EVALUATION KIT AVAILABLE

MAX16974

High-Voltage, 2.2MHz, 2A Automotive Step-Down Converter with Low Operating Current

General Description

The MAX16974 is a 2A, current-mode, step-down converter with an integrated high-side switch. It is designed to operate with 3.5V to 28V input voltages, while using only 35µA quiescent current at no load. The switching frequency is adjustable from 220kHz to 2.2MHz by an external resistor and can be synchronized to an external clock. The output voltage is pin selectable to be 5V fixed or 1V to 10V adjustable. The wide input voltage range makes the device ideal for automotive and industrial applications.

The device operates in skip mode for reduced current consumption in light-load applications. An adjustable reset threshold helps keep microcontrollers alive down to their lowest specified input voltage. Protection features include cycle-by-cycle current limit, overvoltage, and thermal shutdown with automatic recovery. The device also features a power-good monitor to ease power-supply sequencing.

The device operates over the -40°C to +125°C automotive temperature range and is available in a 16-pin TSSOP-EP package.

Applications

Automotive

Industrial

Features

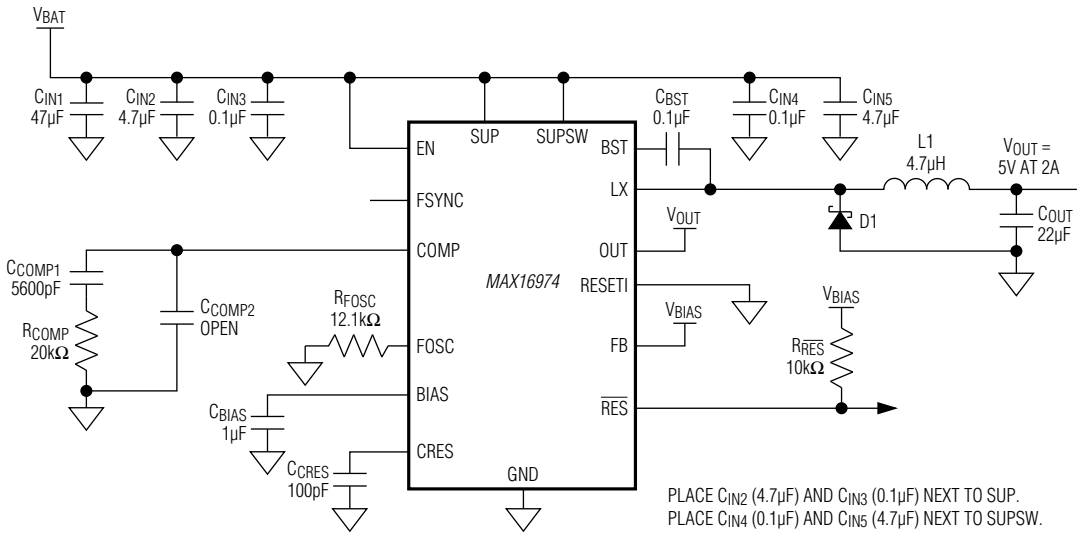
- **Wide 3.5V to 28V Input Voltage Range**
- **42V Input Transient Tolerance**
- **5V Fixed or 1V to 10V Adjustable Output Voltage**
- **Integrated 2A Internal High-Side Switch**
- **Adjustable Switching Frequency (220kHz to 2.2MHz)**
- **Operates Through Cold Crank with High Duty Cycle**
- **Frequency Synchronization Input**
- **Internal Boost Diode**
- **35µA Skip-Mode Operating Current**
- **5µA Typical Shutdown Current**
- **Adjustable Power-Good Output Level and Timing**
- **3.3V Logic Level to 42V Compatible Enable Input**
- **Current-Limit, Thermal-Shutdown, and Overvoltage Protections**
- **Automotive Temperature Range: -40°C to +125°C**
- **AEC-Q100 Qualified**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16974AUE/V+	-40°C to +125°C	16 TSSOP-EP*

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Typical Application Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-5630; Rev 3; 12/16

ABSOLUTE MAXIMUM RATINGS

SUP, SUPSW, EN, LX to GND.....-0.3V to +45V
SUP to SUPSW.....-0.3V to +0.3V
BST to GND .....-0.3V to +47V
BST to LX .....-0.3V to +6V
OUT to GND.....-0.3V to +12V
RESETI, FOSC, COMP, BIAS, FSYNC, CRES, $\overline{RES}$, FB to GND .....-0.3V to +6V
Output Short-Circuit Duration.....Continuous

Continuous Power Dissipation (T_A = +70°C)
TSSOP (derate 26.1mW/°C above +70°C)..... 2088.8mW*
Operating Temperature Range..... -40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

**As per JEDEC 51 standard (multilayer board).*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....38.3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{SUP} = V_{SUPSW} = 14V, L1 = 4.7µH, V_{EN} = 14V, C_{IN} = 10µF, C_{OUT} = 22µF, C_{BIAS} = 1µF, C_{BST} = 0.1µF, C_{CRES} = 1nF, R_{FOSC} = 12.1kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{SUP}	Normal operation	3.5		28	V
Supply Current	I_{SUP}	Normal operation, I_{LOAD} = 1.5A		2	3	mA
		Skip mode, no load, V_{OUT} = 5V		35	50	µA
Shutdown Supply Current		V_{EN} = 0V		5	10	µA
BIAS Regulator Voltage	V_{BIAS}	V_{SUP} = V_{SUPSW} = 6V to 42V, V_{OUT} > 6V	4.9	5.1	5.5	V
BIAS Undervoltage Lockout	V_{UVBIAS}	V_{BIAS} rising	2.85	3.05	3.25	V
BIAS Undervoltage Lockout Hysteresis	V_{UVBIAS_HYS}			350		mV
Thermal-Shutdown Threshold				175		°C
OUTPUT VOLTAGE (OUT)						
Output Voltage	V_{OUT}	Normal operation, V_{FB} = V_{BIAS}, I_{LOAD} = 2A, T_A = +25°C	4.95	5	5.05	V
		Normal operation, V_{FB} = V_{BIAS}, I_{LOAD} = 2A, -40°C < T_A <+125°C	4.9	5	5.1	
Skip-Mode Output Voltage	V_{OUT_SKIP}	No load, V_{FB} = V_{BIAS} (Note 2)	4.95	5.05	5.2	V
Load Regulation		V_{OUT} = 5V, V_{FB} = V_{BIAS}; 400mA < I_{LOAD} < 2A		1		%
Line Regulation		6V < V_{SUP} < 28V		0.02		%/V
BST Input Current	I_{BST}	100% duty cycle, V_{BST} - V_{LX} = 5V		1.5	3	mA
LX Current Limit	I_{LX}		2.5	3	3.5	A
Skip-Mode Current Threshold	I_{SKIP_TH}			240		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{SUP} = V_{SUPSW} = 14V, L1 = 4.7µH, V_{EN} = 14V, C_{IN} = 10µF, C_{OUT} = 22µF, C_{BIAS} = 1µF, C_{BST} = 0.1µF, C_{CRES} = 1nF, R_{FOSC} = 12.1kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Switch On-Resistance	R_{ON}	R_{ON} measured between SUPSW and LX, I_{LX} = 500mA		185	400	mΩ
LX Leakage Current	$I_{LX,LEAK}$	V_{SUP} = 28V, V_{LX} = 0V, T_A = +25°C			1	µA
		V_{SUP} = 28V, V_{LX} = 0V, T_A = +125°C		0.04		
TRANSCONDUCTANCE AMPLIFIER (COMP)						
FB Input Current	I_{FB}			20		nA
FB Regulation Voltage	V_{FB}	FB connected to an external resistive divider, T_A = +25°C	0.99	1.0	1.01	V
		FB connected to an external resistive divider, -40°C < T_A < +125°C	0.985	1.0	1.015	
FB Line Regulation	ΔV_{LINE}	6V < V_{SUP} < 28V		0.02		%/V
Transconductance (from FB to COMP)	$g_{m,EA}$	V_{FB} = 1V, V_{BIAS} = 5V		1000		µS
Minimum On-Time	$t_{MIN,ON}$			120		ns
Cold-Crank Event Duty Cycle	DC_{CC}			92		%
OSCILLATOR FREQUENCY						
Oscillator Frequency		R_{FOSC} = 120kΩ	190	260	310	kHz
		R_{FOSC} = 12.1kΩ	2.00	2.20	2.48	MHz
EXTERNAL CLOCK INPUT (FSYNC)						
External Input Clock Acquisition Time	t_{FSYNC}			4		Cycles
External Input Clock High Threshold	V_{FSYNC_HI}	V_{FSYNC} rising	1.5			V
External Input Clock Low Threshold	V_{FSYNC_LO}	V_{FSYNC} falling			0.5	V
FSYNC Pulldown Resistance	I_{FSYNC}			510		kΩ
Soft-Start Time	t_{SS}	f_{SW} = 220kHz		9.3		ms
		f_{SW} = 2.2MHz		0.93		
ENABLE INPUT (EN)						
Enable-On Threshold Voltage Low	V_{EN_LO}				0.7	V
Enable-On Threshold Voltage High	V_{EN_HI}		2.2			V
Enable Threshold Voltage Hysteresis	$V_{EN,HYS}$			0.35		V
Enable Input Current	I_{EN}			0.5		µA
RESET						
Reset Internal Switching Level	V_{TH_RISING}	V_{FB} rising, V_{RESETI} = 0V	0.88	0.90	0.92	V
	$V_{TH\_FALLING}$	V_{FB} falling, V_{RESETI} = 0V	0.83	0.85	0.87	
RESETI Threshold Voltage	V_{RESETI_LO}	V_{RESETI} falling	1.13	1.2	1.27	V
CRES Threshold Voltage	V_{CRES_HI}	V_{CRES} rising	1.1	1.25	1.45	V
CRES Threshold Hysteresis	V_{CRES_HYS}			0.04		V
RESETI Input Current	I_{RESET}	V_{RESETI} = 0V		0.02		µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{SUP} = V_{SUPSW} = 14V, L1 = 4.7µH, V_{EN} = 14V, C_{IN} = 10µF, C_{OUT} = 22µF, C_{BIAS} = 1µF, C_{BST} = 0.1µF, C_{CRES} = 1nF, R_{FOSC} = 12.1kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

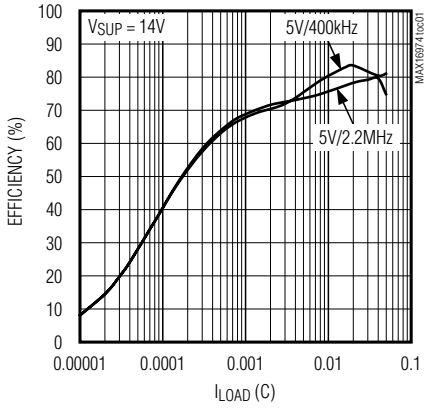
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CRES Source Current	I_{CRES}	V_{OUT} in regulation	9.5	10	10.5	µA
CRES Pulldown Current	I_{CRES_PD}	V_{OUT} out of regulation	1			mA
$\overline{RES}$ Sink Current		$V_{\overline{RES}}$ pulls low, $V_{\overline{RES}}$ > 0.4V	1			mA
$\overline{RES}$ Leakage Current (Open-Drain Output)		V_{OUT} in regulation, T_A = +25°C			1	µA
Reset Debounce Time	t_{RES_DEB}	V_{RESETI} falling		25		µs

Note 2: Guaranteed by design; not production tested.

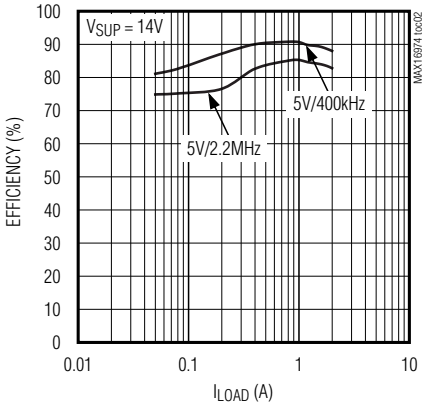
Typical Operating Characteristics

(V_{SUP} = V_{SUPSW} = 14V, V_{OUT} = 5V, FSYNC = GND, f_{OSC} = 400kHz, T_A = +25°C, unless otherwise noted. See Figure 1.)

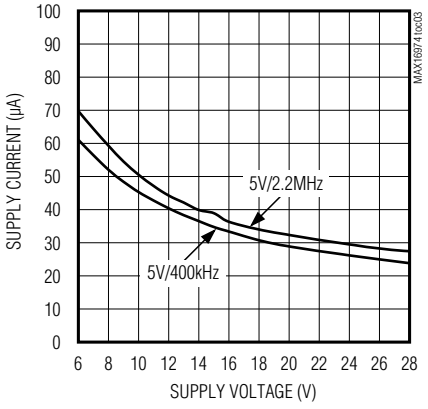
EFFICIENCY vs. I_{LOAD} (SKIP MODE)



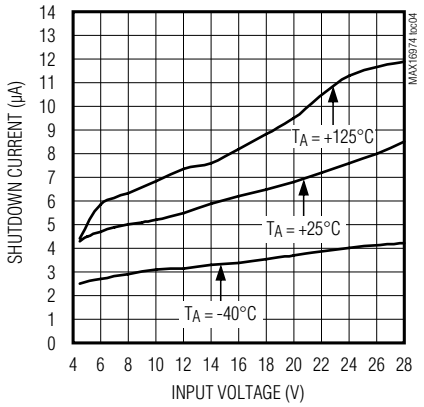
EFFICIENCY vs. I_{LOAD}



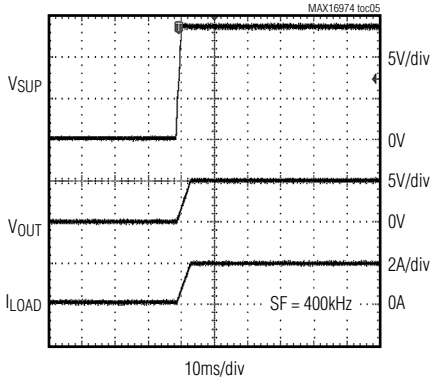
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN CURRENT vs. INPUT VOLTAGE



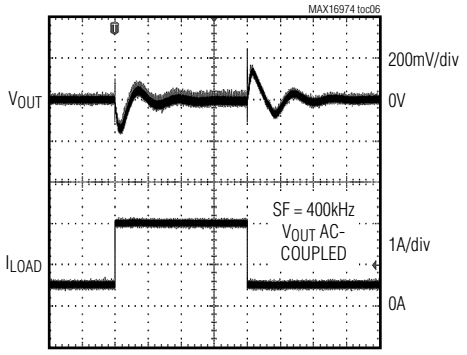
STARTUP INTO HEAVY LOAD



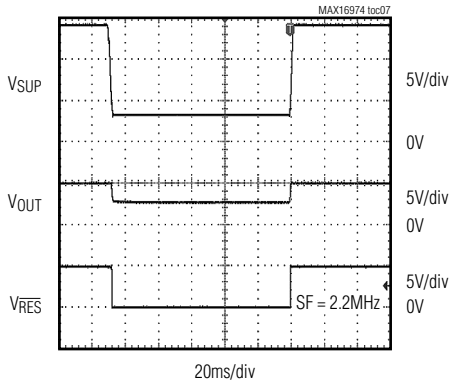
Typical Operating Characteristics (continued)

(V_{SUP} = V_{SUPSW} = 14V, V_{OUT} = 5V, FSYNC = GND, f_{OSC} = 400kHz, T_A = +25°C, unless otherwise noted. See Figure 1.)

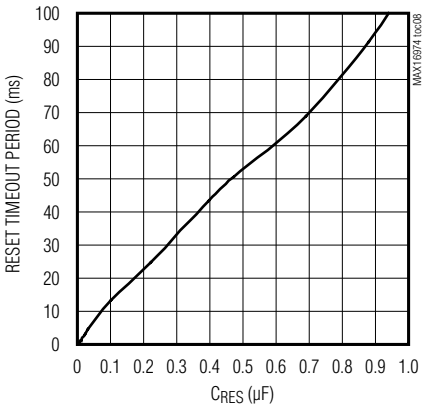
LOAD TRANSIENT



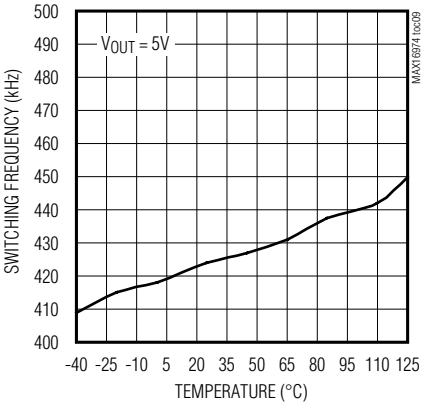
UNDERVOLTAGE PULSE



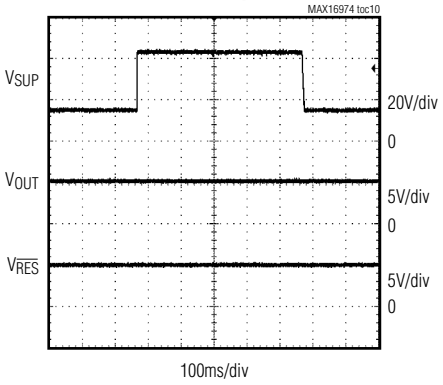
RESET TIMEOUT PERIOD vs. C_{RES}



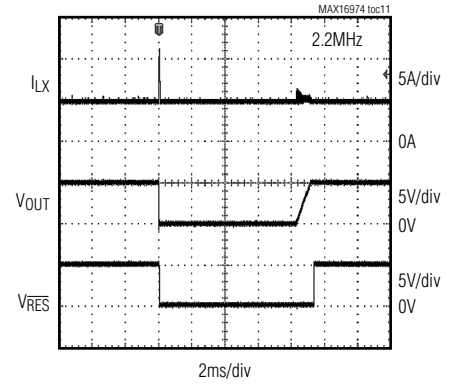
SWITCHING FREQUENCY vs. TEMPERATURE



LOAD DUMP TEST (5V/2.2MHz)



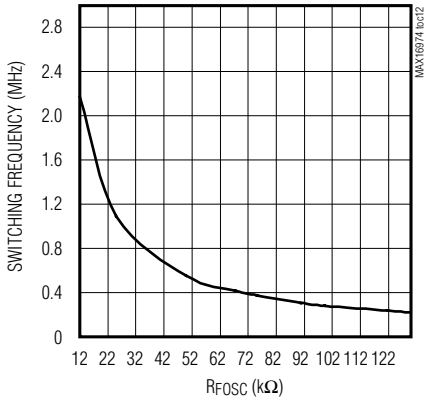
SHORT-CIRCUIT RESPONSE



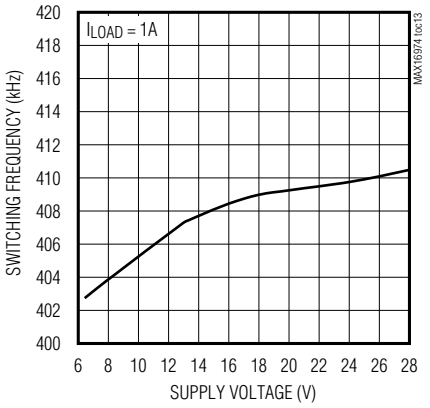
Typical Operating Characteristics (continued)

(V_{SUP} = V_{SUPSW} = 14V, V_{OUT} = 5V, FSYNC = GND, f_{OSC} = 400kHz, T_A = +25°C, unless otherwise noted. See Figure 1.)

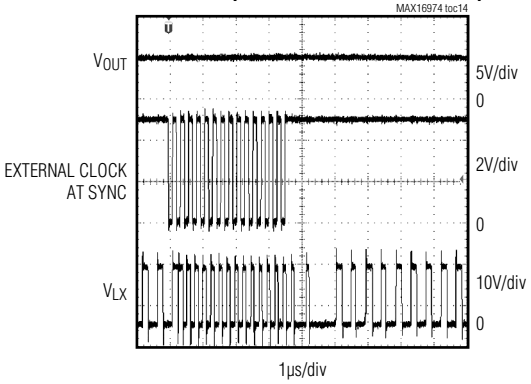
SWITCHING FREQUENCY vs. R_{FOSC}



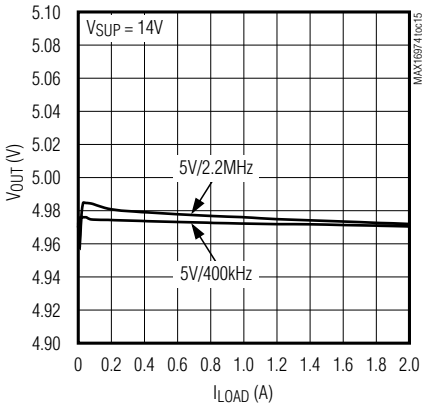
SWITCHING FREQUENCY vs. SUPPLY VOLTAGE



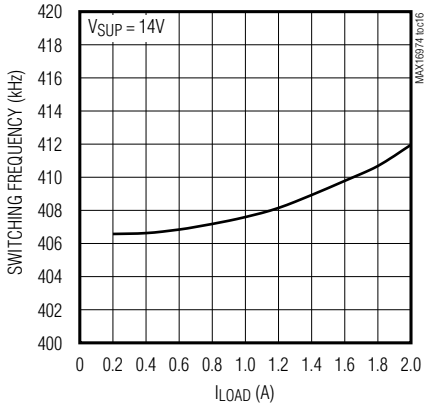
FSYNC TRANSITION FROM INTERNAL TO EXTERNAL FREQUENCY (5V/2.2MHz CONFIGURATION)



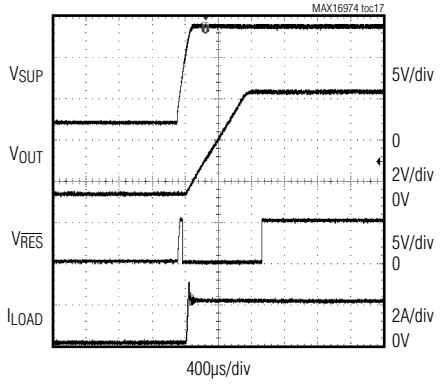
V_{OUT} vs. I_{LOAD}



SWITCHING FREQUENCY vs. I_{LOAD}



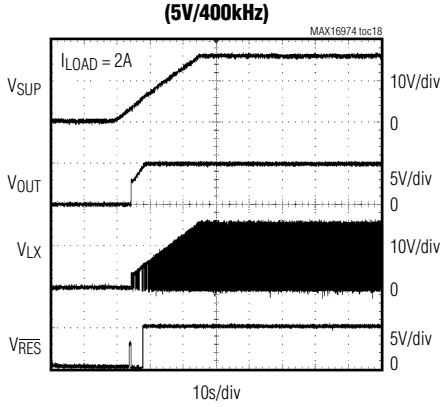
STARTUP INTO HEAVY LOAD (5V/2.2MHz)



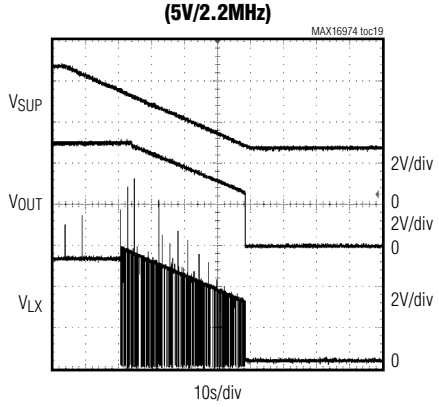
Typical Operating Characteristics (continued)

(V_{SUP} = V_{SUPSW} = 14V, V_{OUT} = 5V, FSYNC = GND, f_{OSC} = 400kHz, T_A = +25°C, unless otherwise noted. See Figure 1.)

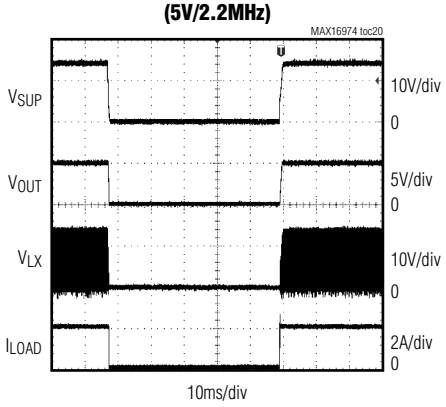
OUTPUT RESPONSE TO SLOW INPUT RAMP UP (5V/400kHz)



OUTPUT RESPONSE TO SLOW INPUT RAMP DOWN (5V/2.2MHz)



DIPS AND DROP TEST (5V/2.2MHz)



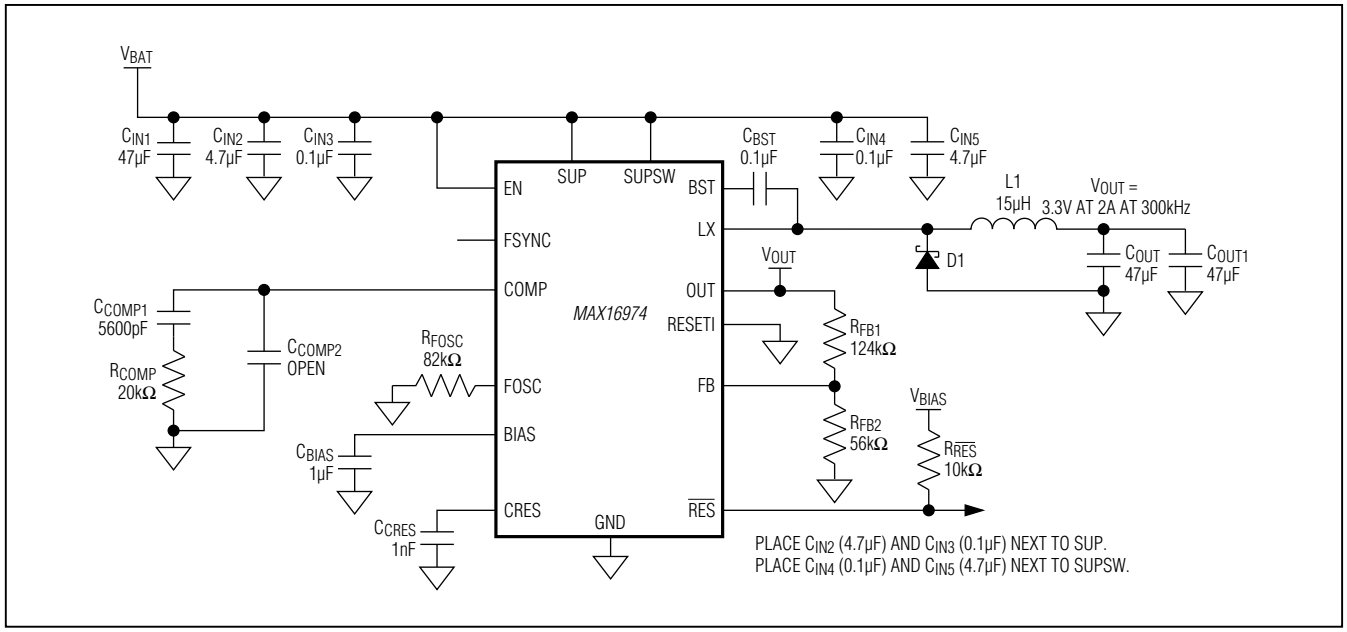
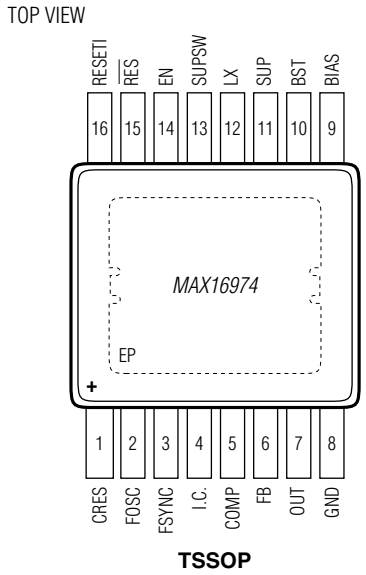


Figure 1. 3.3V Fixed Output Voltage Configuration

Pin Configuration



TSSOP

Pin Description

PIN	NAME	FUNCTION
1	CRES	Analog Reset Timer. CRES sources 10µA (typ) of current into an external capacitor to set the reset timeout period. Reset timeout period is defined as the time between the start of output regulation and $\overline{RES}$ going high impedance. Leave unconnected for minimum delay time.
2	FOSC	Resistor-Programmable Switching-Frequency Setting Control Input. Connect a resistor from FOSC to GND to set the switching frequency.
3	FSYNC	Synchronization Input. The device synchronizes to an external signal applied to FSYNC. The external signal period must be 10% shorter than the internal clock period for proper operation.
4	I.C.	Internally Connected. Connect to GND.
5	COMP	Error Amplifier Output. Connect an RC network from COMP to GND for stable operation. See the *Compensation Network* section for more details.
6	FB	Feedback Input. Connect an external resistive divider from OUT to FB and GND to set the output voltage. Connect to BIAS to set the output voltage to 5V.
7	OUT	Supply Input. OUT provides power to the internal circuitry when the output voltage of the converter is set between 3V and 5V.
8	GND	Ground
9	BIAS	Linear Regulator Output. BIAS powers up the internal circuitry. Bypass with a 1µF capacitor to ground.
10	BST	High-Side Driver Supply. Connect a 0.1µF capacitor between LX and BST for proper operation.
11	SUP	Voltage Supply Input. SUP powers up the internal linear regulator. Connect a minimum of 1µF capacitor from SUP to GND close to the IC. Connect SUP to SUPSW.
12	LX	Inductor Switching Node. Connect a Schottky diode between LX and GND.
13	SUPSW	Internal High-Side Switch Supply Input. SUPSW provides power to the internal switch. For most applications, connect 4.7µF and 0.1µF capacitors between SUPSW and GND close to the IC. See the *Input Capacitor* section for more details.
14	EN	Battery-Compatible Enable Input. Drive EN low to disable the device. Drive EN high to enable the device.
15	$\overline{RES}$	Open-Drain Active-Low Reset Output. $\overline{RES}$ asserts when V_{OUT} is below the reset threshold set by RESETI.
16	RESETI	Reset Threshold Level Input. Connect to a resistive divider to set the reset threshold for $\overline{RES}$. Connect to GND to enable the internal reset threshold.
—	EP	Exposed Pad. Connect EP to a large-area contiguous copper ground plane for effective power dissipation. Do not use as the only IC ground connection. EP must be connected to GND.

Detailed Description

The MAX16974 is a constant-frequency, current-mode, automotive buck converter with an integrated high-side switch. The device operates with 3.5V to 28V input voltages and tolerates input transients up to 42V. During undervoltage events, such as cold-crank conditions, the internal pass device maintains up to 92% duty cycle.

An open-drain, active-low reset output helps monitor the output voltage. The device offers an adjustable reset threshold that helps keep microcontrollers alive down to their lowest specified input voltage. A capacitor programmable reset timeout ensures proper startup.

The switching frequency is resistor programmable from 220kHz to 2.2MHz to allow optimization for efficiency, noise, and board space. A clock input, FSYNC, allows the device to synchronize to an external clock.

During light-load conditions, the device enters skip mode that reduces the quiescent current down to 35µA. The 5V fixed output voltage option eliminates the need for external resistors and reduces the supply current by up to 50µA. See Figure 2 for the internal block diagram.

Supply Voltage Range (SUP)

The device's supply voltage range (V_{SUP}) is compatible with the typical 3.5V to 28V automotive battery voltage range and can tolerate transients up to 42V.

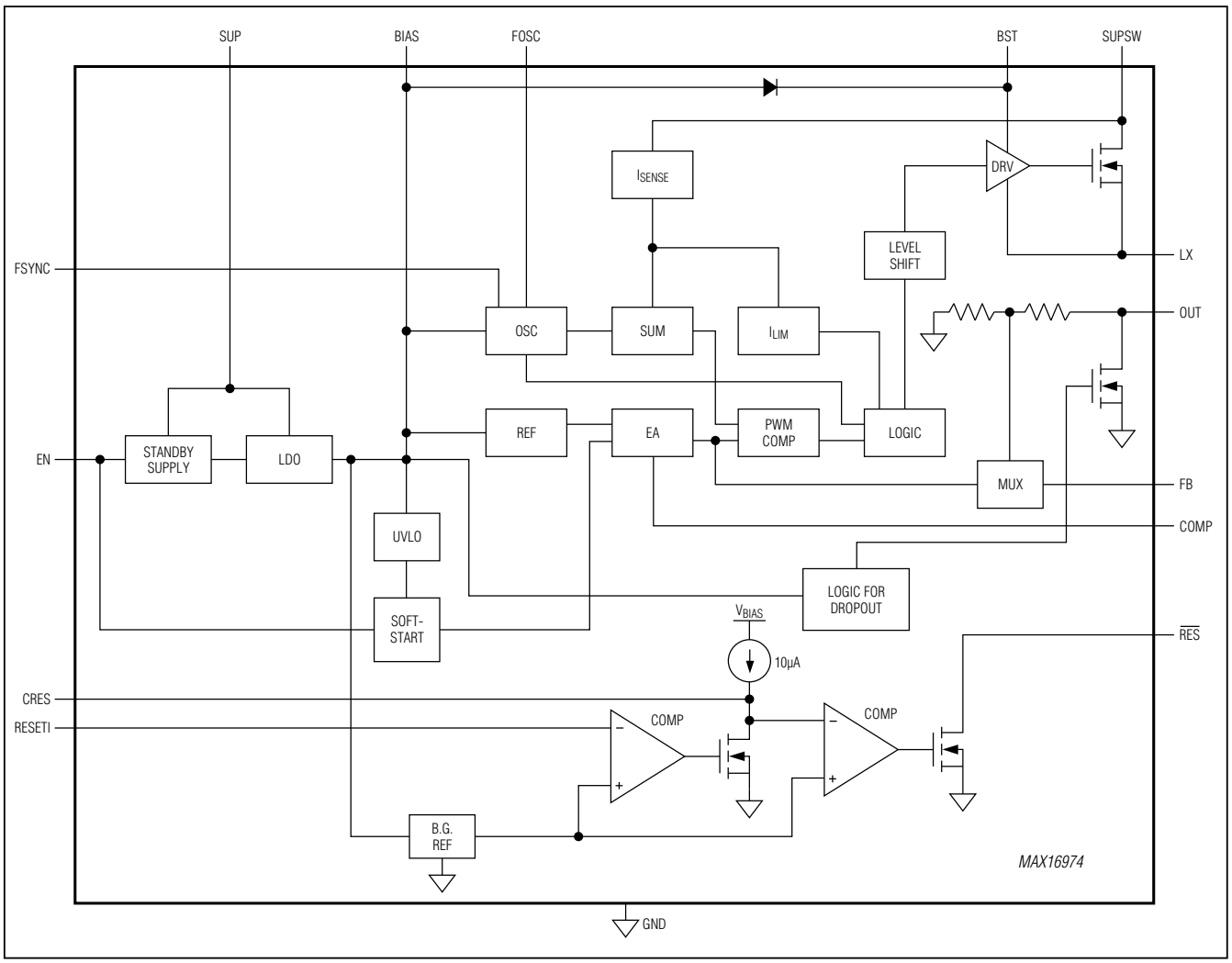


Figure 2. Internal Block Diagram

Linear Regulator Output (BIAS)

The device includes a 5V linear regulator, V_{BIAS}, that provides power to the internal circuitry. Connect a 1µF ceramic capacitor from BIAS to GND. If the output voltage is set between 3.0V and 5.6V, the internal linear regulator only provides power until the output is in regulation. The internal linear regulator turns off once the output is in regulation and load current is below 50mA, allowing the output to provide power to the device.

External Clock Input (FSYNC)

The device synchronizes to an external clock signal applied at FSYNC. The signal at FSYNC must have a 10% shorter period than the internal clock period for proper synchronization. The internal clock signal takes over if the externally applied signal has a frequency lower than the internal clock frequency.

Adjustable Reset Level

The device features a programmable reset threshold using a resistive divider between OUT, RESETI, and GND. Connect RESETI to GND for the internal threshold. $\overline{RES}$ asserts low when the output voltage falls to 85% of its programmed level. $\overline{RES}$ deasserts when the output voltage goes above 90% of its set voltage.

Some microprocessors have a wide input voltage range (5V to 3.3V) and can operate during device dropout. Use a resistive divider at RESETI to adjust the reset activation level ($\overline{RES}$ goes low) to lower levels. The reference voltage at RESETI is 1.2V (typ).

The device also offers a capacitor-programmable reset timeout period. Connect a capacitor from CRES to GND to adjust the reset timeout period. When the output voltage goes out of regulation, $\overline{RES}$ asserts low, and the reset timing capacitor discharges with a 1mA pulldown current. Once the output is back in regulation, the reset timing capacitor recharges with 10µA (typ) current. $\overline{RES}$ stays low until the voltage at CRES reaches 1.25V (typ).

Dropout Operation

The device has an effective maximum duty cycle to help refresh the BST capacitor when continuously operated in dropout. When the high-side switch is on for three consecutive clock cycles, the device forces the high-side switch off during the final 35% of the fourth clock cycle. When the high-side switch is off, the LX node is pulled low by current flowing through the external Schottky diode. This increases the voltage across the BST capacitor. To ensure that the inductor has enough current to pull LX to ground, an internal load sinks current from V_{OUT} when the device is close to dropout and when the external load is small. Once the input voltage is increased above the dropout region, the device continues to regulate without restarting.

If the device has neither external clock nor external load, the effective maximum duty cycle is 92% when operating deep into dropout. This effective maximum duty cycle is influenced by the external load and by the external synchronized clock, if any.

System Enable (EN)

An enable-control input (EN) activates the device from its low-power shutdown mode. EN is compatible with inputs from automotive battery level down to 3.3V. The high-voltage compatibility allows EN to be connected to SUP, KEY/KL30, or the INH pin of a CAN transceiver.

EN turns on the internal regulator. Once V_{BIAS} is above the internal lockout level, V_{UVL} = 3.05V (typ), the controller activates and the output voltage ramps up within 2048 cycles of the switching frequency.

A logic-low at EN shuts down the device. During shutdown, the internal linear regulator and gate drivers turn off. Shutdown is the lowest power state and reduces the quiescent current to 5µA (typ). Drive EN high to bring the device out of shutdown.

Overvoltage Protection

The device includes an overvoltage protection circuit that protects the device when there is an overvoltage condition at the output. If the output voltage increases by more than 10% of its set voltage, the device stops switching. The device resumes regulation once the overvoltage condition is removed.

Overload Protection

The overload protection circuitry is activated when the device is in current limit and V_{OUT} is below the reset threshold. Under these conditions the device enters a soft-start mode. If the overcurrent condition is removed before the soft-start mode is over, the device regulates the output voltage to its set value. Otherwise, the soft-start cycle repeats until the overcurrent condition is removed.

Skip Mode

During light-load operation, $I_{INDUCTOR} \leq 240mA$, the device enters skip-mode operation. Skip mode turns off the internal switch and allows the output to drop below regulation voltage before the switch is turned on again. The lower the load current, the longer it takes for the regulator to initiate a new cycle. Because the converter skips unnecessary cycles, the converter efficiency increases. During skip mode the quiescent current drops to 35µA.

Overtemperature Protection

Thermal-overload protection limits the total power dissipation in the device. When the junction temperature exceeds +175°C (typ), an internal thermal sensor shuts down the internal bias regulator and the step-down controller, allowing the IC to cool. The thermal sensor turns on the device again after the junction temperature cools by +15°C.

Applications Information

Output Voltage/Reset Threshold Resistive Divider Network

Although the device's output voltage and reset threshold can be set individually, Figure 3 shows a combined resistive divider network to set the desired output voltage and the reset threshold using three resistors. Use the following formula to determine the R_{FB3} of the resistive divider network:

$$R_{FB3} \quad \frac{R_{TOTAL} \times V_{REF}}{OUT}$$

where V_{REF} = 1V, R_{TOTAL} = selected total resistance of R_{FB1}, R_{FB2}, and R_{FB3} in ohms, and V_{OUT} is the desired output voltage in volts.

$$R_{FB2} = \frac{R_{TOTAL} \times V_{REF\_RES}}{V_{RES}} - R_{FB3}$$

where V_{REF_RES} is 1.2V (see the *Electrical Characteristics* table), and V_{RES} is the desired reset threshold in volts.

The precision of the reset threshold function is dependent on the tolerance of the resistors used for the divider. Care must be taken to choose the values of the resistors. Too small a resistor value adds to the device's quiescent current, whereas if the resistors are too large, there is some noise susceptibility to the FB pin.

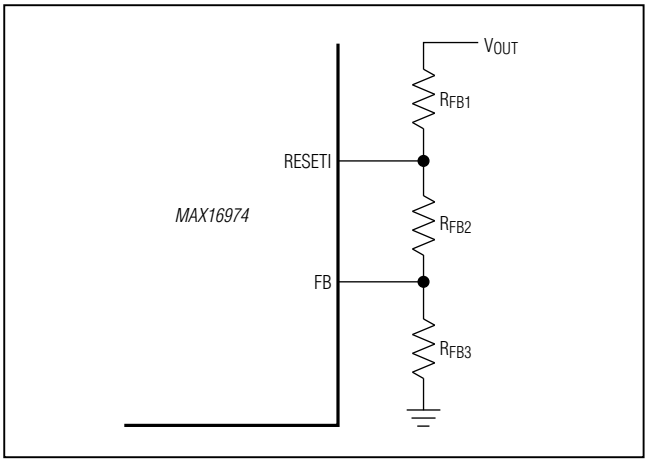


Figure 3. Output Voltage/Reset Threshold Resistive Divider Network

Boost Capacitor for Dropout Operation

The device has an internal boost capacitor refresh algorithm for dropout operation. This is required to ensure proper boost capacitor voltage, which delivers power to the gate drive circuitry. If the high-side MOSFET is on consecutively for 3.65 clock cycles, the internal counter detects this and turns off the high-side MOSFET for 0.35 clock cycles. This is of particular concern when V_{IN} is falling and approaching V_{OUT} and a minimum switching frequency of 220kHz is used.

The worst-case condition for boost capacitor refresh time is with no load on the output. For the boost capacitor to recharge completely, the LX node must be pulled to ground. If there is no current in the inductor, the LX node does not go to ground. To solve this issue, an internal load of approximately 100mA is turned on at the 6th clock cycle, which is determined by a separate counter.

In the worst-case condition with no load, the LX node does not go below ground during the first detect of the 3.65 clock cycles. It must wait for the next 3.65 clock cycles to finish. This means the soonest the LX node can go below ground is 4 + 3.65 = 7.65 clock cycles. This time does not factor in the size of the inductor and the time it takes for the inductor current to build up to 100mA (internal load).

So no-load minimum time before refresh is:

dt (no load) = 7.65 clock cycles = 7.65 x 5µs
(at 220kHz) = 34.77µs

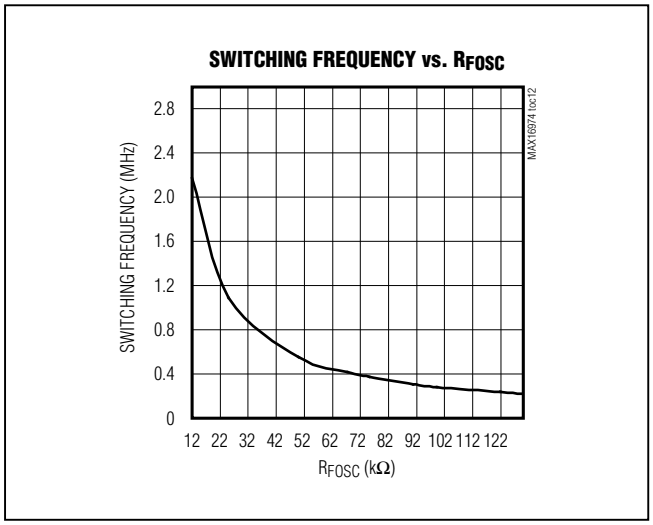


Figure 4. Switching Frequency vs. R_{FOSC}

Assume a full 100mA is needed to refresh the BST capacitor. Depending on the size of the inductor, the time it takes to build up a full 100mA in the inductor is given by:

dt (inductor) = L x di/dV (current buildup starts from the 6th clock cycle)

L = inductor value chosen in the design guide

di is the required current = 100mA

dV = voltage across the inductor (assume this to be 0.5V), which means V_{IN} is greater than V_{OUT} by 0.5V

If dt (inductor) < 7.65 - 6 (clock cycles), the BST capacitor should be sized as follows:

BST_CAP ≥ $I_{BST(DROPOUT)}$ x dt (no load)/dV (BST capacitor)

dt (no load) = 7.65 clock cycles = 34.77µs

dV (BST capacitor) for (3.3V to 5V) output = V_{OUT} - 2.7V (2.7V is the minimum voltage allowed on the bst capacitor)

If dt (inductor) > 7.65 - 6 clock cycles, then wait for the next count of 3.65 clock cycles making dt (no load) = 11.65 clock cycles.

Considering the typical inductor values used for 220kHz operation, the safe way to design the BST capacitor is to assume:

dt (no load) as 16 clock cycles

So the final BST_CAPACITOR equation is:

BST_CAP = $I_{BST(DROPOUT)}$ x dt (no load)/dV (BST capacitor)

where:

$I_{BST(DROPOUT)}$ = 3mA (worst case)

dt (no load) = 16 clock cycles

dV (BST capacitor) = V_{OUT} - 2.7V.

Reset Timeout Period

The device offers a capacitor-adjustable reset timeout period. Connect up to 0.1µF capacitor from CRES to GND to set the timeout period. CRES can source 10µA of current. Use the following formula to set the timeout period:

$$RESET\_TIMEOUT = \frac{1.25V \times C}{10 \times 10^{-6}A} (s),$$

where C is the capacitor from CRES to GND in Farads.

Internal Oscillator

The switching frequency (f_{SW}) is set by a resistor (R_{FOSC}) connected from FOSC to GND. See Figure 4 to select the correct R_{FOSC} value for the desired switching frequency.

For example, a 2.2MHz switching frequency is set with R_{FOSC} = 12.1kΩ. Higher frequencies allow designs with lower inductor values and less output capacitance. Consequently, peak currents and I^2R losses are lower at higher switching frequencies, but core losses, gate-charge currents, and switching losses increase.

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). To select inductance value, the ratio of inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good compromise between size and loss is a 30% peak-to-peak ripple current to average current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{SUP} - V_{OUT})}{V_{SUP} f_{SW} I_{OUT} LIR}$$

where V_{SUP}, V_{OUT}, and I_{OUT} are typical values so that efficiency is optimum for typical conditions. The switching frequency is set by R_{FOSC} (see the *Internal Oscillator* section). The exact inductor value is not critical and can be adjusted to make trade-offs among size, cost, efficiency, and transient response requirements.

Table 1. Inductor Size Comparison

INDUCTOR SIZE	
SMALLER	**LARGER**
Lower price	Smaller ripple
Smaller form factor	Higher efficiency
Faster load response	Larger fixed-frequency range in skip mode

Table 1 shows a comparison between small and large inductor sizes.

The inductor value must be chosen so the maximum inductor current does not reach the minimum current limit of the device. The optimum operating point is usually found between 10% and 30% ripple current. When pulse skipping (light loads), the inductor value also determines the load-current value at which PFM/PWM switchover occurs.

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Most inductor manufacturers provide inductors in standard values, such as 1.0µH, 1.5µH, 2.2µH, 3.3µH, etc. Also look for nonstandard values, which can provide a better compromise in LIR across the input voltage range. If using a swinging inductor (where the no-load inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values. For the selected inductance value, the actual peak-to-peak inductor ripple current ($\Delta I_{INDUCTOR}$) is defined by:

$$\Delta I_{INDUCTOR} = \frac{V_{OUT}(V_{SUP} - V_{OUT})}{V_{SUP} \times f_{SW} \times L}$$

where $\Delta I_{INDUCTOR}$ is in A, L is in H, and f_{SW} is in Hz.

Ferrite cores are often the best choices, although powdered iron is inexpensive and can work well at 220kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}$$

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \frac{\sqrt{V_{OUT}(V_{SUP} - V_{OUT})}}{V_{SUP}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage ($V_{SUP} = 2V_{OUT}$), so $I_{RMS(MAX)} = I_{LOAD(MAX)}/2$.

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input-voltage ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the equivalent series resistance (ESR) of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified input-voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{(V_{SUP} - V_{OUT}) \times V_{OUT}}{V_{SUP} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\Delta V_Q \times f_{SW}} \text{ and } D = \frac{V_{OUT}}{V_{SUPSW}}$$

where I_{OUT} is the maximum output current, and D is the duty cycle.

Output Capacitor

The output filter capacitor must have low enough ESR to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions without tripping the overvoltage fault protection. When using high-capacitance, low-ESR capacitors, the filter capacitor's ESR dominates the output voltage ripple. So the size of the output capacitor depends on the maximum ESR required to meet the output voltage ripple ($V_{RIPPLE(P-P)}$) specifications:

$$V_{RIPPLE(P-P)} = ESR \times I_{LOAD(MAX)} \times LIR$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value.

When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising-load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section). However, low-capacity filter capacitors typically have high-ESR zeros that can affect the overall stability. Other important criteria in the choice of the total output capacitance are the device's soft-start time and maximum current capability (see the *Soft-Start Time and Maximum Allowed Output Capacitance* section).

Soft-Start Time and Maximum Allowed Output Capacitance

The device's soft-start time depends on the selected switching frequency. The soft-start time is fixed to 2048 cycles, regardless of the switching frequency. This means at 2.2MHz the soft-start time is ~0.93ms, and at 220kHz the soft-start time is ~9.3ms.

The device is a 2A-capable switching regulator and the amount of load present at startup determines the total output capacitance allowed for a particular application.

$$C_{OUT(MAX)} \approx 2048/f_{SW} \times 1/\Delta V_{OUT} \times \left[I_{LX(MIN)} - I_{LOAD(MAX)}\right]$$

Keeping the above equation in mind, see the following table to ensure that C_{OUT} is less than maximum allowed values.

FREQUENCY = 400kHz		
V_{OUT} (V)	I_{LOAD} (STARTUP) (A)	C_{OUT} (MAX ALLOWED)
3.3	2	775µF
5	2	512µF
3.3	0	3.9mF
5	0	2.6mF
FREQUENCY = 2.2MHz		
V_{OUT} (V)	I_{LOAD} (STARTUP) (A)	C_{OUT} (MAX ALLOWED)
3.3	2	140µF
5	2	93µF
3.3	0	705µF
5	0	465µF

Transient Response

The inductor ripple current also impacts transient response performance, especially at low V_{SUP} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The total output-voltage sag is the sum of the voltage sag while the inductor is ramping up and the voltage sag before the next pulse can occur:

$$V_{SAG} = \frac{L\left(\Delta I_{LOAD(MAX)}\right)^2}{2C_{OUT}\left(\left(V_{SUP} \times D_{MAX}\right) - V_{OUT}\right)} + \frac{\Delta I_{LOAD(MAX)}\left(t - \Delta t\right)}{C_{OUT}}$$

where D_{MAX} is the maximum duty factor (see the *Electrical Characteristics* table), L is the inductor value in µH, C_{OUT} is the output capacitor value in µF, t is the switching period ($1/f_{SW}$) in µs, and Δt equals (V_{OUT}/V_{SUP} x t when in fixed-frequency PWM mode, or L x 0.2 x $I_{MAX}/(V_{SUP} - V_{OUT})$ when in skip mode. The amount of overshoot (V_{SOAR}) during a full-load to a no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \left(\Delta I_{LOAD(MAX)}\right)^2 \times L/\left(2 \times C_{OUT} \times V_{OUT}\right)$$

Rectifier Selection

The device requires an external Schottky diode rectifier as a freewheeling diode. Connect this rectifier close to the device using short leads and short PCB traces. Choose a rectifier with a continuous current rating greater than the highest output current-limit threshold (3.5A), and with a voltage rating greater than the maximum expected input voltage, V_{SUPSW}. Use a low forward-voltage-drop Schottky rectifier to limit the negative voltage at LX. Avoid higher than necessary reverse-voltage Schottky rectifiers that have higher forward-voltage drops.

Compensation Network

The device uses an internal transconductance error amplifier with its inverting input and output available to the user for external frequency compensation. The output capacitor and compensation network determine the loop stability. The inductor and the output capacitor are chosen based on performance, size, and cost. Additionally, the compensation network optimizes the control-loop stability.

The controller uses a current-mode control scheme that regulates the output voltage by forcing the required current through the external inductor, so the device uses

the voltage drop across the high-side MOSFET. Current-mode control eliminates the double pole in the feedback loop caused by the inductor and output capacitor resulting in a smaller phase shift and requiring less elaborate error-amplifier compensation than voltage-mode control. A simple single-series resistor (R_C) and capacitor (C_C) are all that is required to have a stable, high-bandwidth loop in applications where ceramic capacitors are used for output filtering (Figure 5). For other types of capacitors, due to the higher capacitance and ESR, the frequency of the zero created by the capacitance and ESR is lower than the desired closed-loop crossover frequency. To stabilize a nonceramic output capacitor loop, add another compensation capacitor (C_F) from COMP to GND to cancel this ESR zero.

The basic regulator loop is modeled as a power modulator, output feedback divider, and an error amplifier. The power modulator has a DC gain set by $g_{mc} \times R_{LOAD}$, with a pole and zero pair set by R_{LOAD}, the output capacitor (C_{OUT}), and its ESR. The following equations approximate the value for the gain of the power modulator ($GAIN_{MOD(DC)}$), neglecting the effect of the ramp stabilization. Ramp stabilization is necessary when the duty cycle is above 50% and is internally done for the device.

$$GAIN_{MOD(DC)} = g_{mc} \times R_{LOAD}$$

where $R_{LOAD} = V_{OUT}/I_{LOUT(MAX)}$ in Ω and g_{mc} = 3S.

In a current-mode step-down converter, the output capacitor, its ESR, and the load resistance introduce a pole at the following frequency:

$$f_{pMOD} = \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}}$$

The output capacitor and its ESR also introduce a zero at:

$$f_{zMOD} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

When C_{OUT} is composed of "n" identical capacitors in parallel, the resulting $C_{OUT} = n \times C_{OUT(EACH)}$ and $ESR = ESR_{(EACH)}/n$. Note that the capacitor zero for a parallel combination of alike capacitors is the same as for an individual capacitor.

The feedback voltage-divider has a gain of $GAIN_{FB} = V_{FB}/V_{OUT}$, where V_{FB} is 1V (typ).

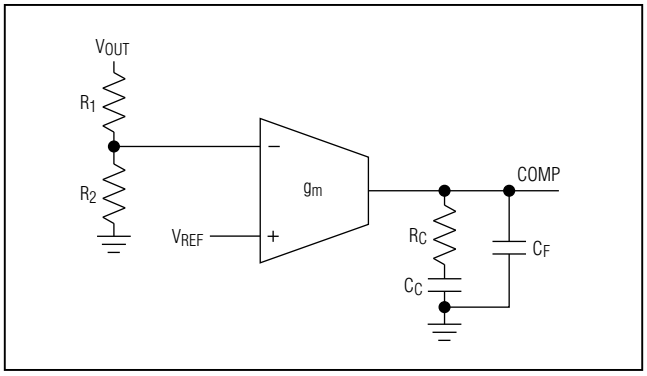


Figure 5. Compensation Network

The transconductance error amplifier has a DC gain of $GAIN_{EA(DC)} = g_{m,EA} \times R_{OUT,EA}$, where $g_{m,EA}$ is the error amplifier transconductance, which is 1000µS (typ), and $R_{OUT,EA}$ is the output resistance of the error amplifier 50MΩ.

A dominant pole (f_{dpEA}) is set by the compensation capacitor (C_C) and the amplifier output resistance ($R_{OUT,EA}$). A zero (f_{ZEA}) is set by the compensation resistor (R_C) and the compensation capacitor (C_C). There is an optional pole (f_{pEA}) set by C_F and R_C to cancel the output capacitor ESR zero if it occurs near the crossover frequency (f_C), where the loop gain equals 1 (0dB)). Thus:

$$f_{pdEA} = \frac{1}{2\pi \times C_C \times (R_{OUT,EA} + R_C)}$$

$$f_{zEA} = \frac{1}{2\pi \times C_C \times R_C}$$

$$f_{pEA} = \frac{1}{2\pi \times C_F \times R_C}$$

The loop-gain crossover frequency (f_C) should be set below 1/5th of the switching frequency and much higher than the power-modulator pole (f_{pMOD}):

$$f_{pMOD} << f_C \le \frac{f_{SW}}{5}$$

The total loop gain as the product of the modulator gain, the feedback voltage-divider gain, and the error amplifier gain at f_C should be equal to 1. So:

$$GAIN_{MOD(fC)} \times \frac{V_{FB}}{V_{OUT}} \times GAIN_{EA(fC)} = 1$$

For the case where f_{zMOD} is greater than f_C:

$$GAIN_{EA(fC)} = g_{m,EA} \times R_C$$

$$GAIN_{MOD(fC)} = GAIN_{MOD(DC)} \times \frac{f_{pMOD}}{f_C}$$

Therefore:

$$GAIN_{MOD(fC)} \times \frac{V_{FB}}{V_{OUT}} \times g_{m,EA} \times R_C = 1$$

Solving for R_C:

$$R_C = \frac{V_{OUT}}{g_{m,EA} \times V_{FB} \times GAIN_{MOD(fC)}}$$

Set the error-amplifier compensation zero formed by R_C and C_C (f_{zEA}) at the f_{pMOD}. Calculate the value of C_C as follows:

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor, C_F, from COMP to GND and set the compensation pole formed by R_C and C_F (f_{pEA}) at the f_{zMOD}. Calculate the value of C_F as follows:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C}$$

As the load current decreases, the modulator pole also decreases; however, the modulator gain increases accordingly and the crossover frequency remains the same.

For the case where f_{zMOD} is less than f_C:

The power-modulator gain at f_C is:

$$GAIN_{MOD(fC)} = GAIN_{MOD(DC)} \times \frac{f_{pMOD}}{f_{zMOD}}$$

The error-amplifier gain at f_C is:

$$GAIN_{EA(fC)} = g_{m,EA} \times R_C \times \frac{f_{zMOD}}{f_C}$$

Therefore:

$$GAIN_{MOD(fC)} \times \frac{V_{FB}}{V_{OUT}} \times g_{m,EA} \times R_C \times \frac{f_{zMOD}}{f_C} = 1$$

Solving for R_C:

$$R_C = \frac{V_{OUT} \times f_C}{g_{m,EA} \times V_{FB} \times GAIN_{MOD(fC)} \times f_{zMOD}}$$

Set the error-amplifier compensation zero formed by R_C and C_C at the f_{pMOD} (f_{zEA} = f_{pMOD}):

$$C_C = \frac{1}{2\pi \times f_{pMOD} \times R_C}$$

If f_{zMOD} is less than 5 x f_C, add a second capacitor, C_F, from COMP to GND. Set f_{pEA} = f_{zMOD} and calculate C_F as follows:

$$C_F = \frac{1}{2\pi \times f_{zMOD} \times R_C}$$

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

1) Use a large contiguous copper plane under the IC package. Ensure that all heat-dissipating components have adequate cooling. The bottom pad of the device must be soldered down to this copper plane for effective heat dissipation and getting the full power out of the IC. Use multiple vias or a single large via in this plane for heat dissipation.
2) Isolate the power components and high-current path from the sensitive analog circuitry. This is essential to prevent any noise coupling into the analog signals.
3) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high-current path composed of input capacitor, high-side FET, inductor, and the output capacitor should be as short as possible.

4) Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs (2oz vs. 1oz) to enhance full-load efficiency.
5) The analog signal lines should be routed away from the high-frequency planes. This ensures integrity of sensitive signals feeding back into the IC.
6) The ground connection for the analog and power section should be close to the IC. This keeps the ground current loops to a minimum. In cases where only one ground is used, enough isolation between analog return signals and high power signals must be maintained.
7) Ensure a high-frequency decoupling capacitor of 0.1µF is placed next to the SUP pin of the IC. This capacitor prevents high-frequency noise from entering the SUP pin. Adding a resistor between the SUPSW and SUP pins along with the decoupling capacitor at the SUP pin is recommended to reduce noise sensitivity.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TSSOP-EP	U16E+3	21-0108	90-0120

High-Voltage, 2.2MHz, 2A Automotive Step-Down Converter with Low Operating Current

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/10	Initial release	—
1	7/11	Corrected the $GAIN_{MOD(DC)}$ and f_{pMOD} equations in the *Compensation Network* section	16
2	3/15	Updated first two lines in *Absolute Maximum Ratings* section	2
3	12/16	Changed BIAS Regulator Voltage max in *Electrical Characteristics* from 5.4 to 5.5	2