![maxim integrated logo]

Keywords: DC-DC converter, switchmode, EMI, circuit board, PCB, layout, noise reduction

APPLICATION NOTE 3645

Correct Board Layout Lowers EMI of Switchmode Converters

Nov 04, 2005

Abstract: Component placement and board layout have a fundamental impact on EMI performance of switching converters. The basic techniques outlined in this article minimize electric and magnetic fields, as well as conducted EMI.

Switching-mode DC-DC converters are found in almost all electronic systems today, and their popularity is primarily due to their high power-conversion efficiency. Unfortunately, they also have the reputation of being noisy and unstable, and are indeed often causes for failed EMI certification. Most of these problems (barring poor component selection) originate in the component placement and the board layout. Board parasitics can ruin a perfectly specified design. A good layout not only helps with EMI certification but is also crucial to get correct functionality. To understand this problem, it is necessary to review the EMI specification and then to identify potential EMI sources in a typical DC-DC converter. We use the step-down converter as an example (which is directly applicable to step-up converters, and easily applied to other topologies). Basic guidelines for laying out DC-DC converters are outlined, followed by a practical example.

The EMI specification prescribes a pass/fail mask in the frequency domain. It is divided into two frequency ranges. In the lower range, 150kHz to 30MHz, the conducted AC current onto the line source is measured. In the higher range, 30MHz to 1GHz, the radiated electric and magnetic fields are measured. Electric fields are generated by a circuit's node voltages, while magnetic fields are generated by currents. The most problematic waveforms have steps (e.g., square waves), which generate harmonics reaching up to very high frequencies.

To identify EMI sources, study the conceptual step-down converter[1] in **Figure 1a**. The idea behind switching supplies is to operate transistors Q1 and Q2 as switches instead of in the linear mode. The currents through and the voltage drops across the transistors are square wave-like but out of phase to minimize power loss.
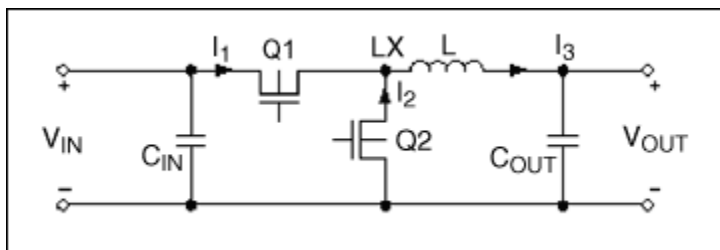

Figure 1a. In this conceptual step-down converter, the switching transistors Q1 and Q2 are controlled by

complementary drive signals, so they operate as switches to achieve high efficiency.

Referring to **Figure 1b**, the switch-node voltage V_{LX} and the transistor currents I_1 and I_2 have square waveforms and contain high-frequency components. The inductor current I_3 has a triangular shape and should be treated as a potential noise source. These waveforms are needed to achieve high efficiency, but pose a major problem from an EMI viewpoint.
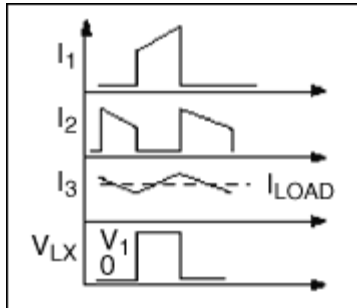

Figure 1b. Current and voltage waveforms in a step-down converter. The switch transistor currents I_1 and I_2, as the switch node voltage V_{LX} are square wave-like and potential EMI sources.

An ideal converter would produce no external magnetic and electric field, and would only draw DC current at its input. All effects of the switching activity should be confined within the converter block. It is the responsibility of the circuit designer *and* layout engineer to ensure this goal is met:

Electric field radiation is generated at the LX node, as all other nodes are at constant voltage. This field is relatively easy to confine by having a reasonably small node area and having a ground plane nearby (the field then terminates on this plane). Do not overdo it, as too much added stray capacitance lowers efficiency and can introduce ringing of the LX voltage. But too small a node will give series impedance, which should be avoided.

Magnetic field radiation is generated by the switching currents I_1 to I_3. The parasitic inductance of the PCB layout in each of the current loops determines the field strength. The nonmetalized board area between the current loops must be minimized and the trace width maximized for lowest magnetic fields. The inductor (L) itself must obviously confine its field, but this has to do with inductor construction and not PCB layout.

Conducted EMI is a major cause of failure. It is generated when input and output capacitors C_{IN} and C_{OUT} fail to provide low impedance for the switching currents I_1 and I_3. These currents are then conducted to upstream and downstream circuitry. The impedance is composed of the capacitor itself (including parasitics) and also the parasitic impedance of the PCB. The PCB parasitic inductance determines the impedance and should be minimized. This also lowers the magnetic field radiation. Via holes must be avoided *inside* the switching converter as their inductance is simply too high. This is done by creating local planes on the top/component layer for the fast currents of the power supply. The SMT components connect directly to these planes. The paths must be wide and short to minimize inductance. Vias are instead used to connect the local planes to the system planes *outside* of the power supply. Their parasitic inductance now helps to confine the fast currents to the top layer. Sometimes vias can be inserted around the inductor where their impedance effect is swamped to some degree. Another cause of conducted EMI is the ground plane where fast switching currents induce voltage spikes. The switching currents must not share any common path with the external circuitry, including the ground plane. The solution is again to create a local power ground plane on the top layer inside the converter boundary and connect it to the system ground plane at one point, usually at the output capacitor.

Other components include the controller IC, bias and feedback/compensation components, treated as low-level signals. To avoid crosstalk, these signals should be located in an area separate from the power components, with the controller IC wedged in between. One approach is to put power components on one side of the controller and low-level signal components on the other side. The controller IC's gate driver outputs source and sink large current spikes at the switching frequency and the distance between the IC and switching transistors should be minimized. High-impedance nodes, such as feedback and compensation pins, should be kept small and far away from the power components, in particular the switch node LX. DC-DC controller ICs often have two ground pins, GND and PGND. The idea is to separate the low-level signal ground from the power ground. Yet another analog ground plane has to be created that is used for low-level signals. It needs not to reside on the top layer, and vias can be used. The analog ground and power ground should be connected at one point only, usually the PGND pin. In extreme cases (high currents), a true single-point ground might be needed, connecting the local ground, power ground, and system ground plane at the output capacitor.

The discussion can be summarized in a layout guide (similar PCB guidelines are often found in good data sheets):

1. Place and route the power components. Start placing switching transistors Q1 and Q2, inductor L, and input and output capacitors C_{IN} and C_{OUT}. Arrange them so as to minimize the distances between them, in particular the ground connections of Q2, C_{IN} and C_{OUT}, and the C_{IN} and Q1 connection. Next, create top-layer shapes for the power ground, input, output, and LX nodes, and route them on the top layer using wide short traces.
2. Place and route the low-level signal components. The controller IC should be placed close to the switching transistors. Low-level signal components are placed on the other side of the controller. High-impedance nodes are kept small and away from the LX node. Create an analog ground shape on a suitable layer and connect it to power ground at one point.

The techniques described above are illustrated below. The MAX1954 is a low-cost, current-mode PWM controller IC suitable for consumer, as well as telecom and industrial applications. **Figure 2** shows the schematic of the MAX1954 evaluation kit with the board layout in **Figure 3**. It is capable of supplying 5A. The kit features input power options from either a low-voltage (V_{IN}) or high-voltage distribution bus (V_{HSD}).
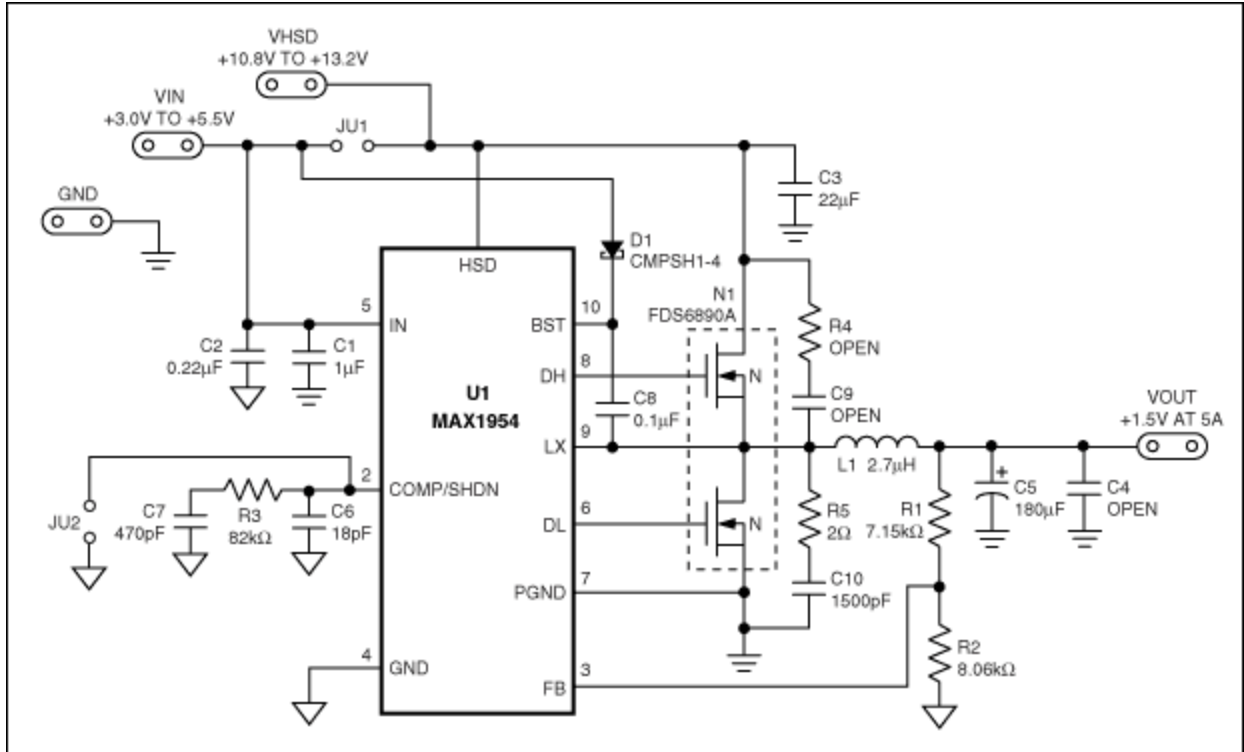
Figure 2. MAX1954 evaluation kit schematics for a high-current step-down converter. Note the different ground symbols.

We start by finding the power components: dual switch transistors N1, inductor L1, input capacitor C3, and output capacitor C5.C3 location is very critical; it should be as close and direct as possible across the high-side MOSFET's drain and the low-side MOSFET's source. This is done to contain the fast switching peak current due to the recovery charge of the low-side MOSFET's body diode when the high-side MOSFET turns on. These are placed in the right side of the layout c.f. Figure 3. All connections are made on the top layer (in red). The LX node in the upper right corner lies directly on top of the system ground plane, and is further shielded from the low area region by top-layer V_{HSD} and P_{GND} nodes.

The low-level signals and related components are placed on the left side of the layout. The pinout of the MAX1954 controller simplifies separation of low-level signals from power currents. Controller U1 is wedged in between low-level signals and the power area. The midpoint of R1 and R2 is the feedback node, and is made small. The compensation node (C7, C8, and R3) is also made small. The analog ground is made invisible in the layout for readability, but is a mid-layer plane with via connections to the components.

The power ground and low-level analog ground planes are separated in the layout, but also in the schematic through different symbols. The top-layer power ground, analog ground plane, and system power plane are joined together in the lower right corner.
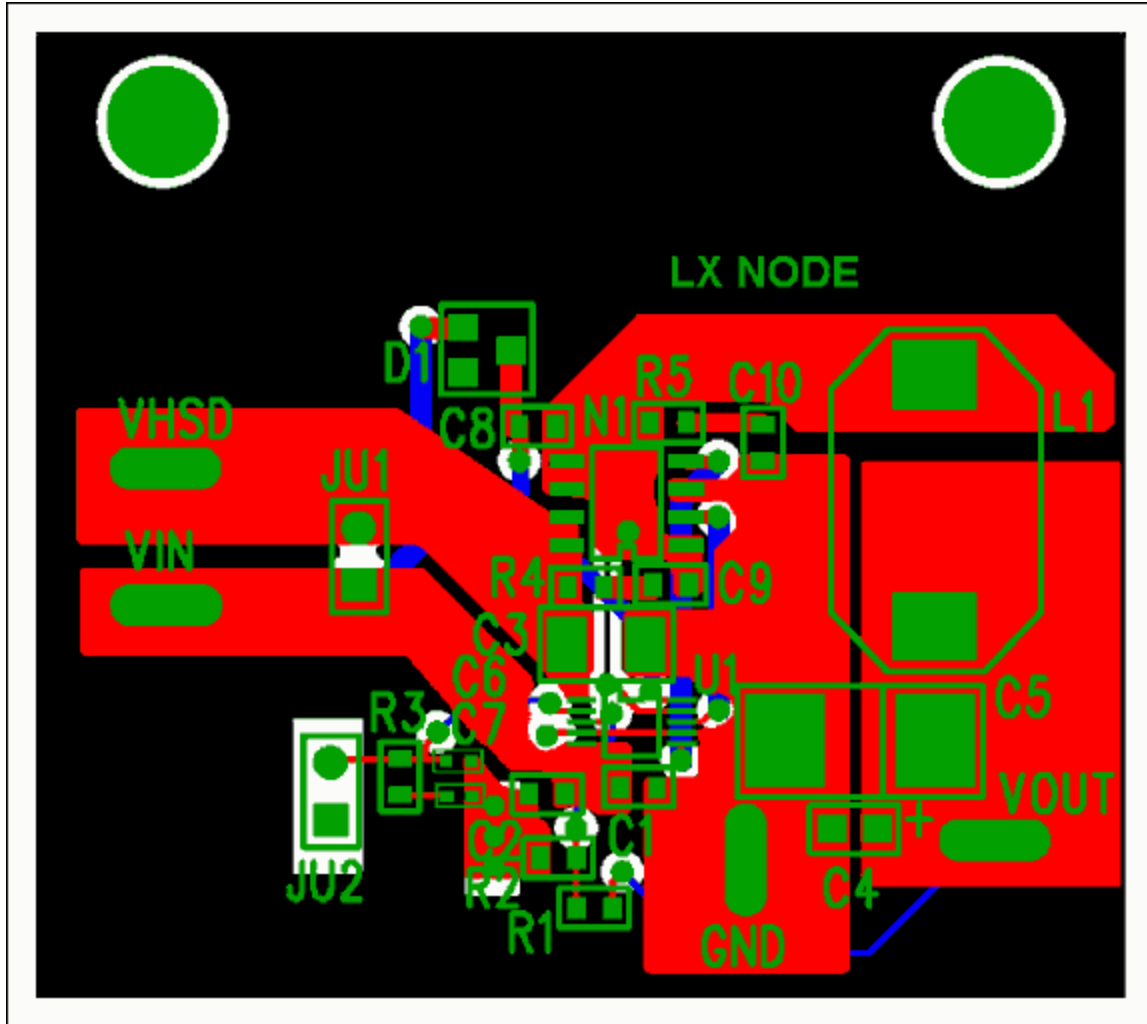
Figure 3. Board layout of the MAX1954 evaluation kit illustrating the outlined principles. The board consists of four layers: red is the top layer; blue is the bottom layer; black is the system ground plane (mid layer); and the analog ground plane (mid layer) is invisible for readability.

The switching node, due to parasitic inductance and capacitance, will have high frequency (40MHz to 100MHz) ringing that could cause EMI. A simple RC snubber circuit can be placed across each MOSFET to dampen the high-frequency ringing. To dampen out the V_{LX} rising-edge ringing, add an RC snubber across the low-side MOSFET. Similarly, to dampen the V_{LX} falling-edge ringing, add an RC snubber across the high-side MOSFET. Because added components add cost, only add the RC snubber if needed. A properly selected RC snubber circuit does not degrade the efficiency much at all, as the energy stored in the parasitic would also be dissipated in the circuit—it just takes longer.

Notes
[1]The guidelines apply directly to step-up converter by swapping Input and Output voltages.

Related Parts		
MAX1954	Low-Cost, High-Frequency, Current-Mode PWM Buck Controllers	Free Samples

More Information

For Technical Support: http://www.maximintegrated.com/support
For Samples: http://www.maximintegrated.com/samples
Other Questions and Comments: http://www.maximintegrated.com/contact

Application Note 3645: http://www.maximintegrated.com/an3645
APPLICATION NOTE 3645, AN3645, AN 3645, APP3645, Appnote3645, Appnote 3645
Copyright © by Maxim Integrated Products
Additional Legal Notices: http://www.maximintegrated.com/legal