# MC14532B

# 8-Bit Priority Encoder

The MC14532B is constructed with complementary MOS (CMOS) enhancement mode devices. The primary function of a priority encoder is to provide a binary address for the active input with the highest priority. Eight data inputs (D0 thru D7) and an enable input ($E_{in}$) are provided. Five outputs are available, three are address outputs (Q0 thru Q2), one group select (GS) and one enable output ($E_{out}$).

**Features**

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load over the Rated Temperature Range
- Pb−Free Packages are Available*

**MAXIMUM RATINGS** (Voltages Referenced to $V_{SS}$)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| DC Supply Voltage Range | $V_{DD}$ | −0.5 to +18.0 | V |
| Input or Output Voltage Range (DC or Transient) | $V_{in}$, $V_{out}$ | −0.5 to $V_{DD}$ + 0.5 | V |
| Input or Output Current (DC or Transient) per Pin | $I_{in}$, $I_{out}$ | ±10 | mA |
| Power Dissipation, per Package (Note 1) | $P_D$ | 500 | mW |
| Ambient Temperature Range | $T_A$ | −55 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Lead Temperature (8 Sec Soldering) | $T_L$ | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.

**TRUTH TABLE**

| Input | | | | | | | | | Output | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $E_{in}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | GS | Q2 | Q1 | Q0 | $E_{out}$ |
| 0 | X | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | X | X | X | X | X | X | X | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | X | X | X | X | X | X | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | X | X | X | X | X | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | X | X | X | X | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | X | X | X | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | X | X | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

X = Don’t Care

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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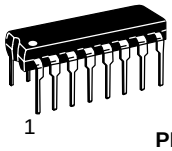
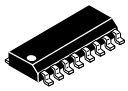
**MARKING DIAGRAMS**





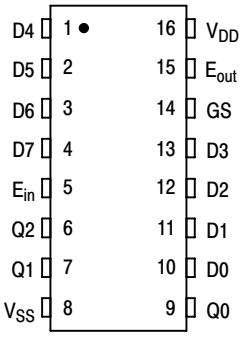
**PDIP−16**
**P SUFFIX**
**CASE 648**




**SOIC−16**
**D SUFFIX**
**CASE 751B**


A = Assembly Location
WL = Wafer Lot
YY, Y = Year
WW = Work Week
G = Pb−Free Package

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC14532BCP | PDIP−16 | 25 Units / Rail |
| MC14532BCPG | PDIP−16 (Pb−Free) | |
| MC14532BD | SOIC−16 | 48 Units / Rail |
| MC14532BDG | SOIC−16 (Pb−Free) | |
| MC14532BDR2 | SOIC−16 | 2500 / Tape & Reel |
| MC14532BDR2G | SOIC−16 (Pb−Free) | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$)

| Characteristic | Symbol | $V_{DD}$ Vdc | − 55°C Min | − 55°C Max | 25°C Min | 25°C Typ (Note 2) | 25°C Max | 125°C Min | 125°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Output Voltage “0” Level $V_{in}$ = $V_{DD}$ or 0 | $V_{OL}$ | 5.0 | − | 0.05 | − | 0 | 0.05 | − | 0.05 | Vdc |
| | | 10 | − | 0.05 | − | 0 | 0.05 | − | 0.05 | |
| | | 15 | − | 0.05 | − | 0 | 0.05 | − | 0.05 | |
| “1” Level $V_{in}$ = 0 or $V_{DD}$ | $V_{OH}$ | 5.0 | 4.95 | − | 4.95 | 5.0 | − | 4.95 | − | Vdc |
| | | 10 | 9.95 | − | 9.95 | 10 | − | 9.95 | − | |
| | | 15 | 14.95 | − | 14.95 | 15 | − | 14.95 | − | |
| Input Voltage “0” Level ($V_O$ = 4.5 or 0.5 Vdc) | $V_{IL}$ | 5.0 | − | 1.5 | − | 2.25 | 1.5 | − | 1.5 | Vdc |
| ($V_O$ = 9.0 or 1.0 Vdc) | | 10 | − | 3.0 | − | 4.50 | 3.0 | − | 3.0 | |
| ($V_O$ = 13.5 or 1.5 Vdc) | | 15 | − | 4.0 | − | 6.75 | 4.0 | − | 4.0 | |
| “1” Level ($V_O$ = 0.5 or 4.5 Vdc) | $V_{IH}$ | 5.0 | 3.5 | − | 3.5 | 2.75 | − | 3.5 | − | Vdc |
| ($V_O$ = 1.0 or 9.0 Vdc) | | 10 | 7.0 | − | 7.0 | 5.50 | − | 7.0 | − | |
| ($V_O$ = 1.5 or 13.5 Vdc) | | 15 | 11 | − | 11 | 8.25 | − | 11 | − | |
| Output Drive Current ($V_{OH}$ = 2.5 Vdc) Source | $I_{OH}$ | 5.0 | –3.0 | − | –2.4 | –4.2 | − | –1.7 | − | mAdc |
| ($V_{OH}$ = 4.6 Vdc) | | 5.0 | – 0.64 | − | – 0.51 | – 0.88 | − | – 0.36 | − | |
| ($V_{OH}$ = 9.5 Vdc) | | 10 | –1.6 | − | –1.3 | – 2.25 | − | –0.9 | − | |
| ($V_{OH}$ = 13.5 Vdc) | | 15 | – 4.2 | − | –3.4 | – 8.8 | − | –2.4 | − | |
| ($V_{OL}$ = 0.4 Vdc) Sink | $I_{OL}$ | 5.0 | 0.64 | − | 0.51 | 0.88 | − | 0.36 | − | mAdc |
| ($V_{OL}$ = 0.5 Vdc) | | 10 | 1.6 | − | 1.3 | 2.25 | − | 0.9 | − | |
| ($V_{OL}$ = 1.5 Vdc) | | 15 | 4.2 | − | 3.4 | 8.8 | − | 2.4 | − | |
| Input Current | $I_{in}$ | 15 | − | ± 0.1 | − | ±0.00001 | ± 0.1 | − | ± 1.0 | μAdc |
| Input Capacitance ($V_{in}$ = 0) | $C_{in}$ | − | − | − | − | 5.0 | 7.5 | − | − | pF |
| Quiescent Current (Per Package) | $I_{DD}$ | 5.0 | − | 5.0 | − | 0.005 | 5.0 | − | 150 | μAdc |
| | | 10 | − | 10 | − | 0.010 | 10 | − | 300 | |
| | | 15 | − | 20 | − | 0.015 | 20 | − | 600 | |
| Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Package) ($C_L$ = 50 pF on all outputs, all buffers switching) | $I_T$ | 5.0 | $I_T$ = (1.74 μA/kHz) f + $I_{DD}$ | | | | | | | μAdc |
| | | 10 | $I_T$ = (3.65 μA/kHz) f + $I_{DD}$ | | | | | | | |
| | | 15 | $I_T$ = (5.73 μA/kHz) f + $I_{DD}$ | | | | | | | |

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

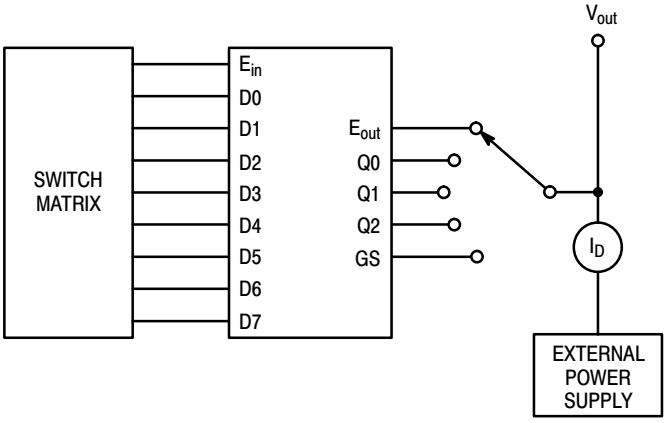
$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: $I_T$ is in μA (per package), $C_L$ in pF, V = ($V_{DD}$ – $V_{SS}$) in volts, f in kHz is input frequency, and k = 0.005.

**SWITCHING CHARACTERISTICS** ($C_L$ = 50 pF, $T_A$ = 25°C) (Note 5)

| Characteristic | Symbol | $V_{DD}$ | Min | Typ (Note 6) | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise and Fall Time | $t_{TLH}$, | | | | | ns |
| $t_{TLH}$, $t_{THL}$ = (1.5 ns/pF) $C_L$ + 25 ns | $t_{THL}$ | 5.0 | – | 100 | 200 | |
| $t_{TLH}$, $t_{THL}$ = (0.75 ns/pF) $C_L$ + 12.5 ns | | 10 | – | 50 | 100 | |
| $t_{TLH}$, $t_{THL}$ = (0.55 ns/pF) $C_L$ + 9.5 ns | | 15 | – | 40 | 80 | |
| Propagation Delay Time — $E_{in}$ to $E_{out}$ | $t_{PLH}$, | | | | | ns |
| $t_{PLH}$, $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 120 ns | $t_{PHL}$ | 5.0 | – | 205 | 410 | |
| $t_{PLH}$, $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 77 ns | | 10 | – | 110 | 220 | |
| $t_{PLH}$, $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 55 ns | | 15 | – | 80 | 160 | |
| Propagation Delay Time — $E_{in}$ to GS | $t_{PLH}$, | | | | | ns |
| $t_{PLH}$, $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 90 ns | $t_{PHL}$ | 5.0 | – | 175 | 350 | |
| $t_{PLH}$, $t_{PHL}$ = (0.66 ns/pF) $C_L$ 57 ns | | 10 | – | 90 | 180 | |
| $t_{PLH}$, $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 40 ns | | 15 | – | 65 | 130 | |
| Propagation Delay Time — $E_{in}$ to $Q_n$ | $t_{PHL}$, | | | | | ns |
| $t_{PLH}$, $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 195 ns | $t_{PLH}$ | 5.0 | – | 280 | 560 | |
| $t_{PLH}$, $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 107 ns | | 10 | – | 140 | 280 | |
| $t_{PLH}$, $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 75 ns | | 15 | – | 100 | 200 | |
| Propagation Delay Time — $D_n$ to $Q_n$ | $t_{PLH}$, | | | | | ns |
| $t_{PLH}$, $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 265 ns | $t_{PHL}$ | 5.0 | – | 300 | 600 | |
| $t_{PLH}$, $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 137 ns | | 10 | – | 170 | 340 | |
| $t_{PLH}$, $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 85 ns | | 15 | – | 110 | 220 | |
| Propagation Delay Time — $D_n$ to GS | $t_{PLH}$, | | | | | ns |
| $t_{PLH}$, $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 195 ns | $t_{PHL}$ | 5.0 | – | 280 | 560 | |
| $t_{PLH}$, $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 107 ns | | 10 | – | 140 | 280 | |
| $t_{PLH}$, $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 75 ns | | 15 | – | 100 | 200 | |

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.




| Output Under Test | $V_{GS} = V_{DD}$ $V_{DS} = V_{out}$ Sink Current | | $V_{GS} = -V_{DD}$ $V_{DS} = V_{out} - V_{DD}$ Source Current | | |
|---|---|---|---|---|---|
| | D0 thru D7 | $E_{in}$ | D0 thru D6 | D7 | $E_{in}$ |
| $E_{out}$ | X | 0 | 0 | 0 | 1 |
| Q0 | X | 0 | 0 | 1 | 1 |
| Q1 | X | 0 | 0 | 1 | 1 |
| Q2 | X | 0 | 0 | 1 | 1 |
| GS | X | 0 | 0 | 1 | 1 |

**Figure 1. Typical Sink and Source Current Characteristics**

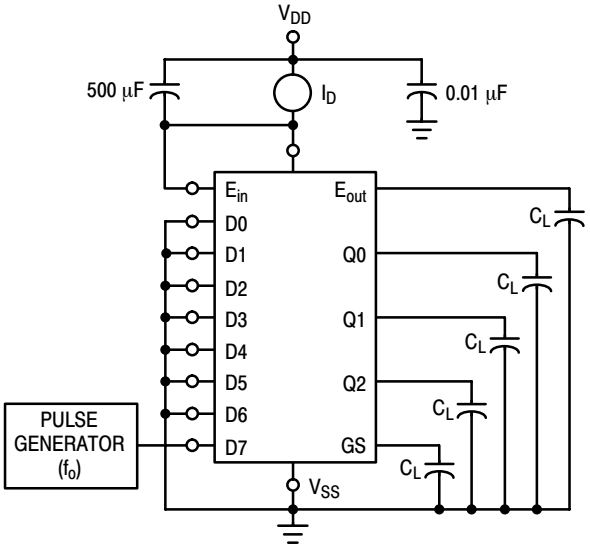



**Figure 2. Typical Power Dissipation Test Circuit**

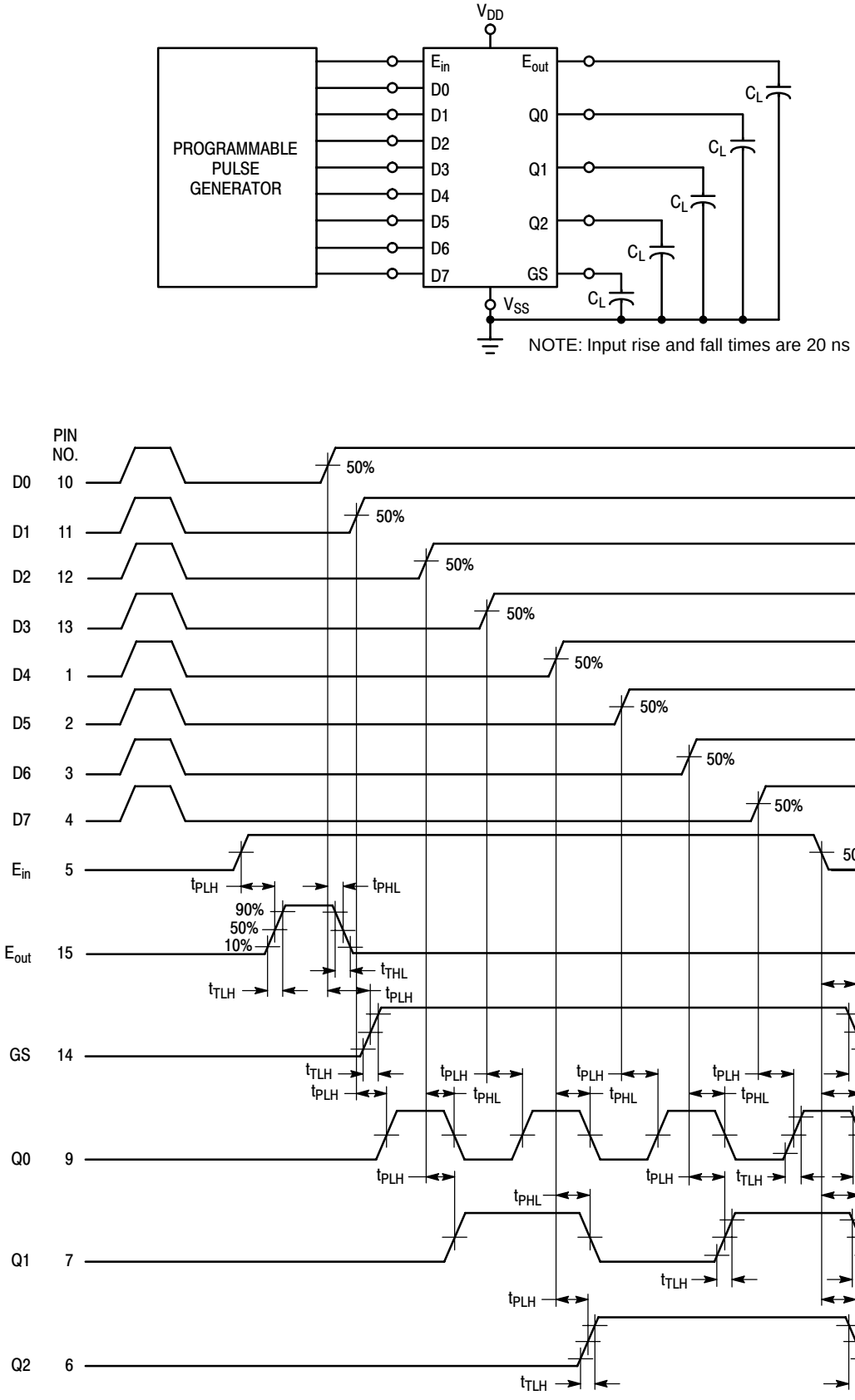



**Figure 3. AC Test Circuit and Waveforms**

**LOGIC EQUATIONS**

$E_{out} = E_{in} \bullet \overline{D0} \bullet \overline{D1} \bullet \overline{D2} \bullet \overline{D3} \bullet \overline{D4} \bullet \overline{D5} \bullet \overline{D6} \bullet \overline{D7}$

$Q0 = E_{in} \bullet (D1 \bullet \overline{D2} \bullet \overline{D4} \bullet \overline{D6} + D3 \bullet \overline{D4} \bullet \overline{D6} + D5 \bullet \overline{D6} + D7)$

$Q1 = E_{in} \bullet (D2 \bullet \overline{D4} \bullet \overline{D5} + D3 \bullet \overline{D4} \bullet \overline{D5} + D6 + D7)$

$Q2 = E_{in} \bullet (D4 + D5 + D6 + D7)$

$GS = E_{in} \bullet (D0 + D1 + D2 + D3 + D4 + 05 + D6 + D7)$

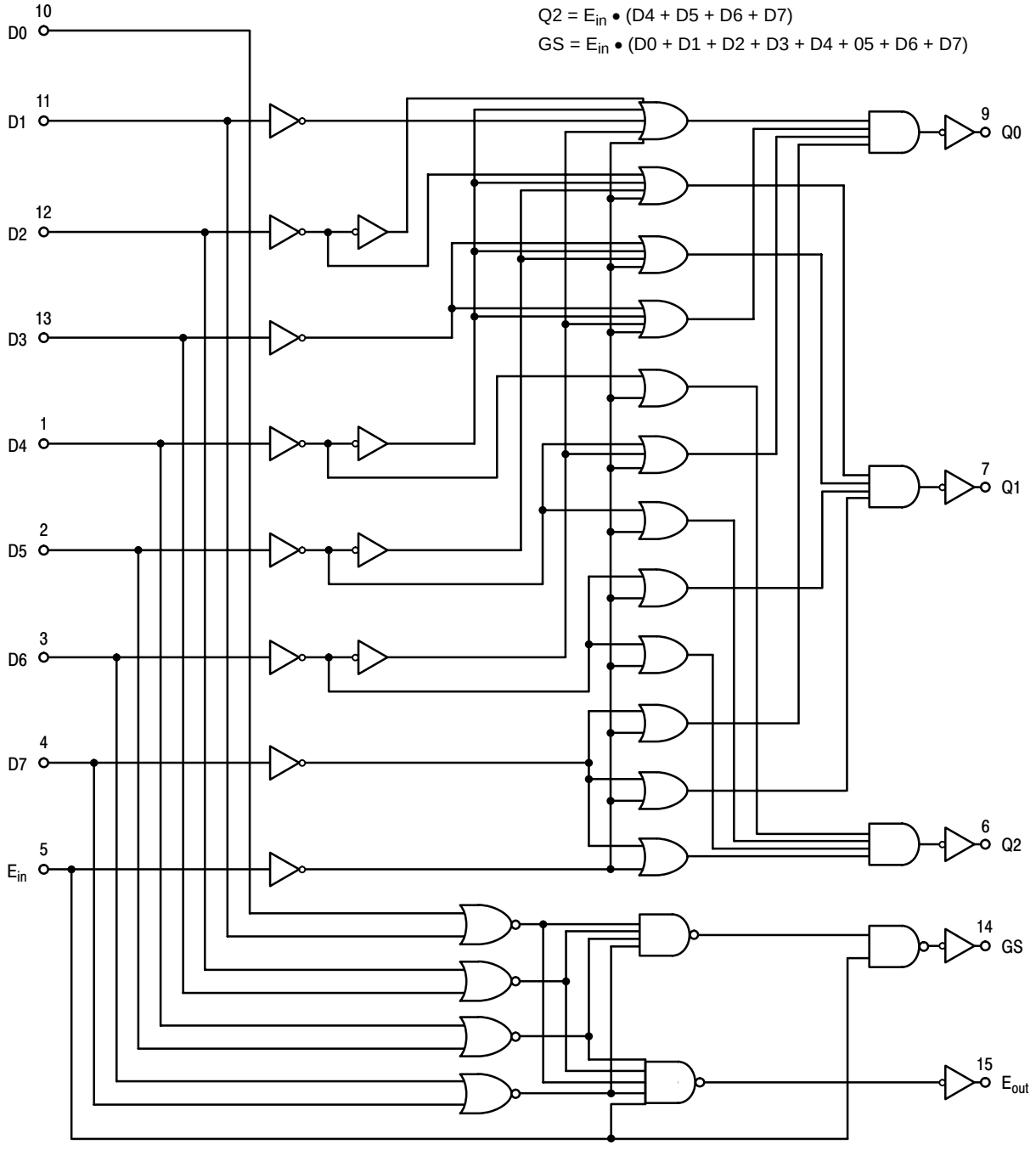



**Figure 4. Logic Diagram**
**(Positive Logic)**

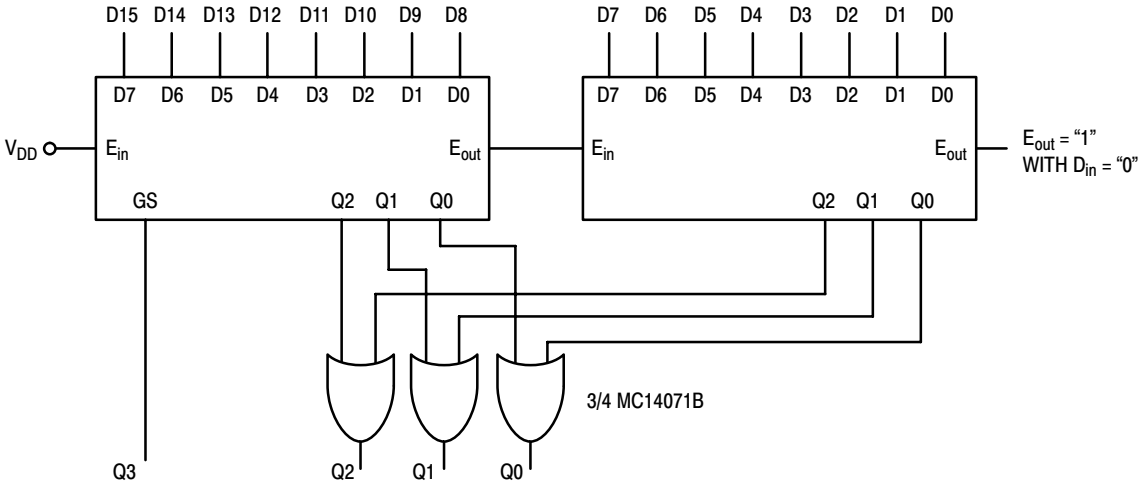



**Figure 5. Two MC14532B's Cascaded for 4−Bit Output**

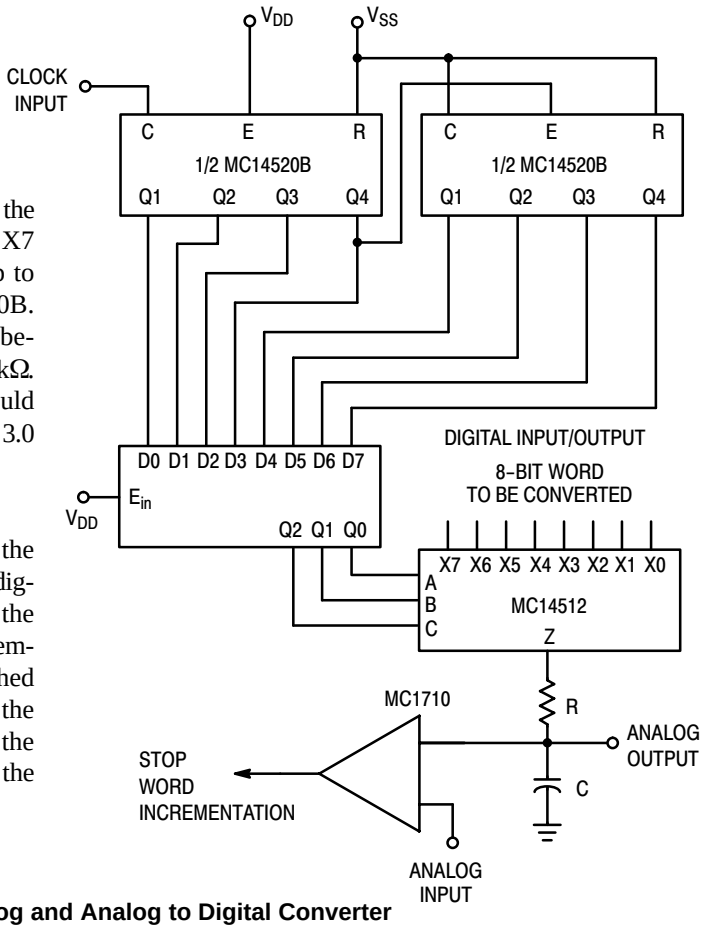



**Figure 6. Digital to Analog and Analog to Digital Converter**

### DIGITAL TO ANALOG CONVERSION

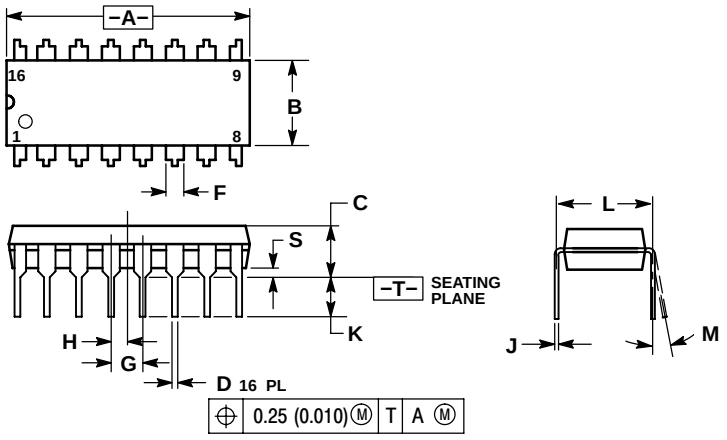
The digital eight−bit word to be converted is applied to the inputs of the MC14512 with the most significant bit at X7 and the least significant bit at X0. A clock input of up to 2.5 MHz (at $V_{DD}$ = 10 V) is applied to the MC14520B. A compromise between $I_{bias}$ for the MC1710 and $\Delta R$ between N and P−channel outputs gives a value of R of 33 kΩ. In order to filter out the switching frequencies, RC should be about 1.0 ms (if R = 33 kΩ, C $\approx$ 0.03 μF). The analog 3.0 dB bandwidth would then be dc to 1.0 kHz.

### ANALOG TO DIGITAL CONVERSION

An analog signal is applied to the analog input of the MC1710. A digital eight−bit word known to represent a digitized level less than the analog input is applied to the MC14512 as in the D to A conversion. The word is incremented at rates sufficient to allow steady state to be reached between incrementations (i.e. 3.0 ms). The output of the MC1710 will change when the digital input represents the first digitized level above the analog input. This word is the digital representation of the analog word.

## PACKAGE DIMENSIONS

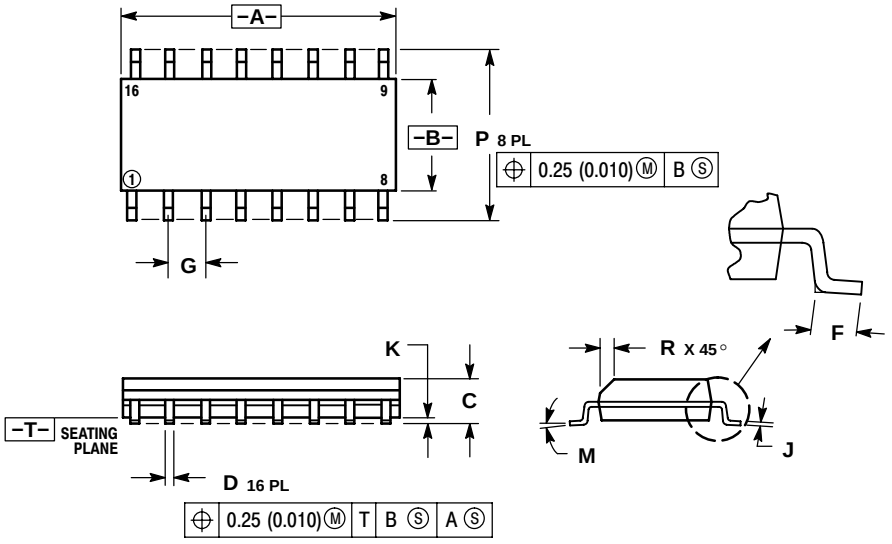
**PDIP−16**
CASE 648−08
ISSUE T




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

**SOIC−16**
CASE 751B−05
ISSUE J




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0 ° | 7 ° | 0 ° | 7 ° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

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