10W Stereo Class-D Audio Power Amplifier With NCPL & SSM

Description

The PAM8106 is a 10W/CH stereo class-D audio amplifier with Spread-Spectrum modulation, which offers high-quality low THD+N, low EMI, and high PSRR.

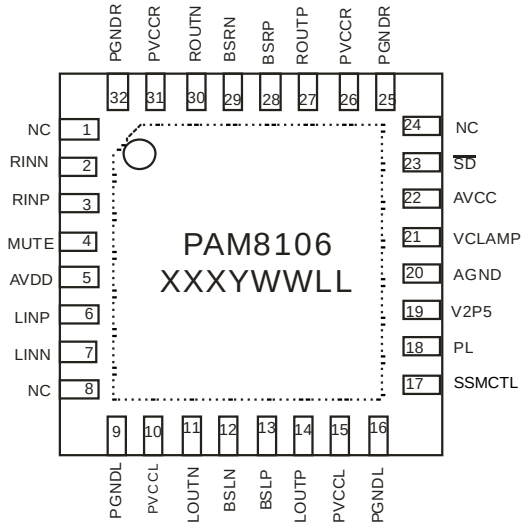
PAM8106 runs off of a 4.5V to 15V supply with high efficiency up to 92% to eliminate the heat-sink. With advanced EMI suppression by Spread-Spectrum Modulation (SSM) technology, PAM8106 requires only inexpensive ferrite bead filters for audio outputs while meeting EMC requirements for overall system cost reduction.

PAM8106 integrates Non-Clipping Power Limit (NCPL) technology which adjusts the gain and eliminate the output signal clip due to the over-level input signal. PAM8106 also offers low THD+N and protects the speaker from damage.

PAM8106 is fully protected against faults with short circuit protection and thermal shutdown as well as undervoltage and DC input protection.

The PAM8106 is available in a W-QFN5050-32 (Standard) package.

Pin Assignments



Features

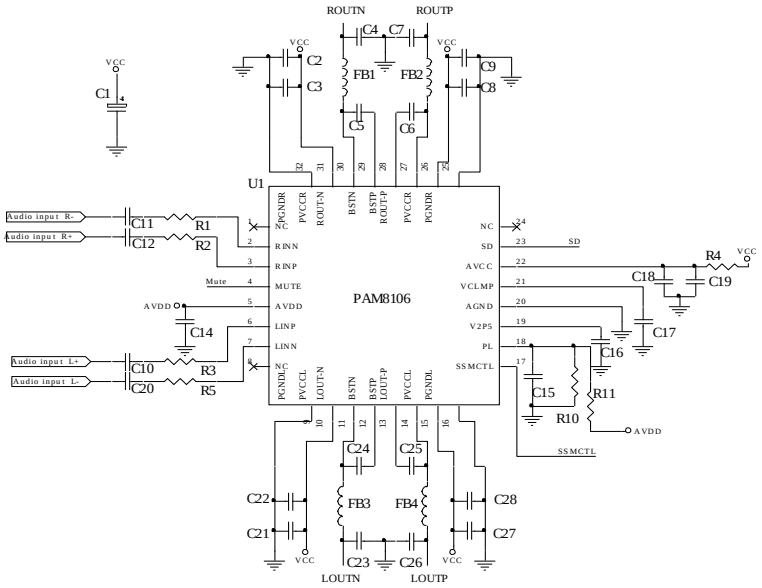
- 4.5V to 15V Operation
- 10Wx2 into a 8Ω speaker with 12V Supply
- 4Ω Impedance Driving Capability
- Built-In Non-Clipping Power Limit (NCPL)
- High SNR, High PSRR,
- Over 92% Efficiency
- Low Noise, Low THD+N
- Low Quiescent Current
- Pop Noise Suppression
- Spread Spectrum Modulation (SSM)
- OCP, OTP, OVP, UVLO, Short-Circuit and DC input Protection
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Applications

- Flat Monitor & LCD TVs
- Multi-Media Speaker System
- DVD Players, Game Machines
- Boom Box & Consumer Electronics Related Application
- Music Instruments

Notes: 1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

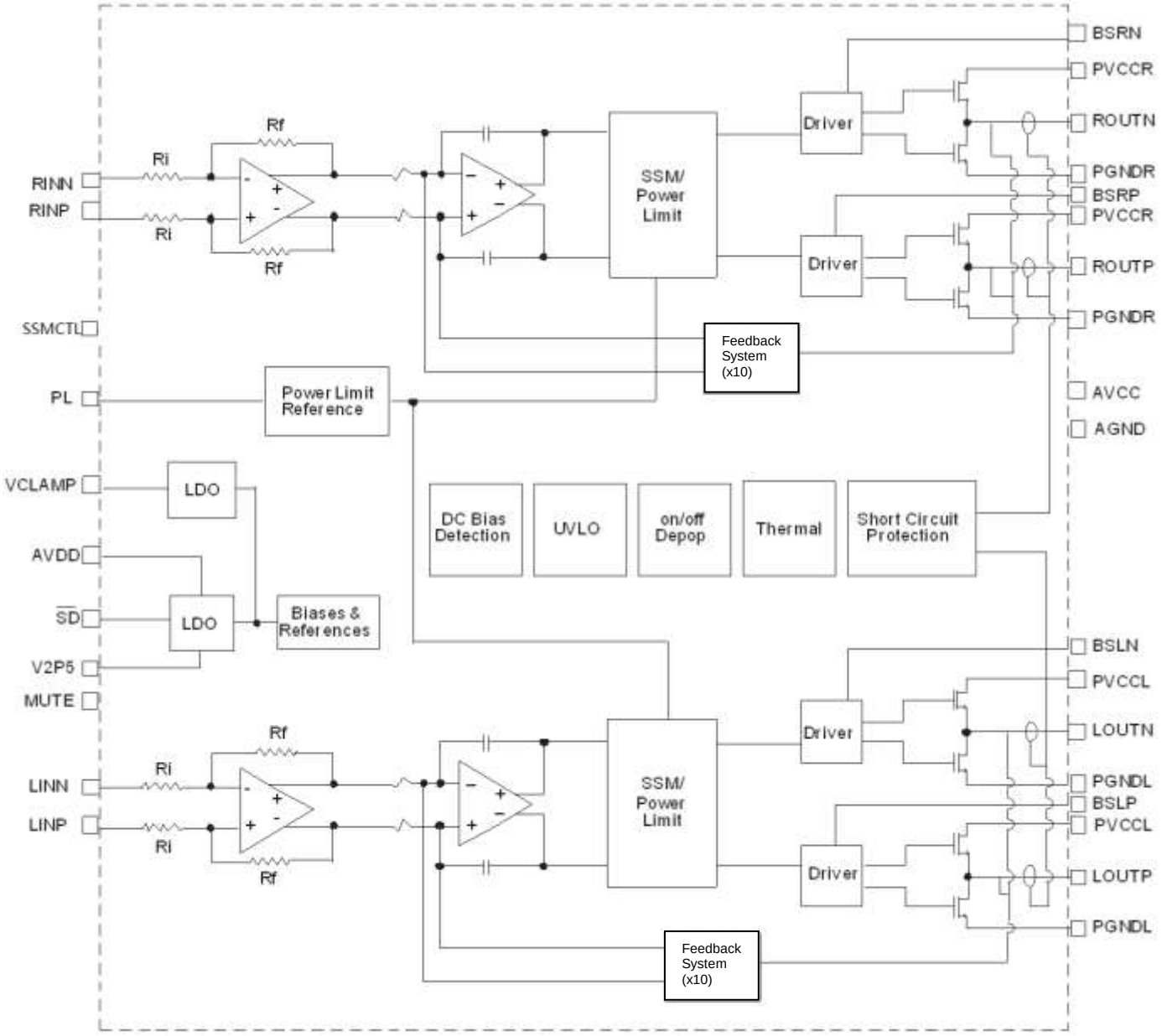
Typical Applications Circuit



Pin Descriptions

Pin Number	Package Name	Function
1, 8, 24	NC	No Connect, floating or connect to GND on PCB
2	RINN	Negative differential audio input for right channel.
3	RINP	Positive differential audio input for right channel.
4	MUTE	A logic-high on this pin disables the outputs and a logic low enables the outputs.
5	AVDD	5V Analog Supply (internally generated)
6	LINP	Positive differential audio input for left channel.
7	LINN	Negative differential audio input for left channel.
9, 16	PGNDL	Power ground for left channel H-bridge.
10, 15	PVCCL	Power supply for left channel H-bridge, not connected to PVCCR or AVCC.
11	LOUTN	Class-D H-bridge negative output for left channel.
12	BSLN	Bootstrap I/O for left channel, negative high-side FET.
13	BSLP	Bootstrap I/O for left channel, positive high-side FET.
14	LOUTP	Class-D H-bridge positive output for left channel.
17	SSMCTL	SSM ON/OFF Control. A Logic-Low enable SSM feature and a Logic-High disable SSM feature. (Logic-High level complies to AVDD). SSM mode will be turned ON if this pin is left floating after power-up, due to pull-up resistor embedded.
18	PL	Reference voltage for power-limit function.
19	V2P5	2.5V Reference for analog cells.
20	AGND	Analog Ground
21	VCLAMP	Internally generated voltage supply for bootstrap capacitors.
22	AVCC	High-voltage analog power supply (4.5V to 15V)
23	$\overline{SD}$	Shutdown signal for IC (low= shutdown, high = operational). Compliance to AVCC.
25, 32	PGNDR	Power ground for right channel H-bridge.
26, 31	PVCCR	Power supply for right channel H-bridge, not connected to PVCCL or AVCC.
27	ROUTP	Class-D H-bridge positive output for right channel.
28	BSRP	Bootstrap I/O for right channel, positive high-side FET.
29	BSRN	Bootstrap I/O for right channel, negative high-side FET.
30	ROUTN	Class-D H-bridge negative output for right channel.
33	Thermal Pad	Connect to ground. Thermal pad should be soldered down on all applications to secure the device properly to the printed wiring board.

Functional Block Diagram



Notes: Gain: R_i = 15k, Rf = 60k; MAX Setting
Power Limit Function: Set by R_I and R_F

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

Symbol	Parameter	Rating	Unit
PVCC/AVCC	Supply Voltage	-0.3 to +18	V
V_I	Input voltages for RINN, RINP, LINN, LINP, MUTE, PL	(GND-0.3) to 5.5	V
$\overline{SD}$	Input voltage for $\overline{SD}$	(GND-0.3) to AVCC	V
T_J	Junction Temperature Range	-40 to +150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{SDR}	Maximum soldering Temperature Range - Lead Temperature 1, 6mm (1/16inch)	260 (5sec)	°C

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
PVCC/AVCC	Supply Voltage	4.5 to 15	V
V_I	Input voltages for RINN, RINP, LINN, LINP	(GND-0.3) to 5.5	V
	Input voltages for RINN-RINP, LINN-LINP	0 to 2	V_{RMS}
$\overline{SD}$	High-Level Input voltage for $\overline{SD}$ Low-Level Input voltage for $\overline{SD}$	3 to AVCC 0 to 0.5	V
MUTE	High-Level Input voltage for MUTE Low-Level Input voltage for MUTE	3 to 5.5 0 to 0.5	V
T_A	Operating Free-Air Temperature range	-40 to +85	°C
T_J	Operating Junction Temperature range	-40 to +150	°C

Thermal Information

Symbol	Parameter	Package	Maximum	Unit
θ_{JC}	Thermal Resistance (Junction to Case)	W-QFN5050-32 (Standard)	5.0	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	W-QFN5050-32 (Standard)	33	°C/W

* The exposed PAD must be soldered to a thermal land on the PCB.

* Measured data by PAM test jig setup condition.

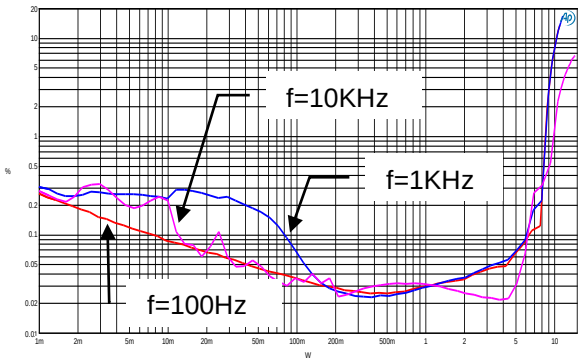
Electrical Characteristics (@T_A = +25°C, V_{CC} = 12V, R_L =8Ω, MAX Gain, unless otherwise specified.)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
AVCC	Supply Voltage	—		4.5	—	15	V
P_O	Continuous Output Power	THD+N = 0.12%, f = 1kHz, R_L = 8Ω		—	6	—	W
		THD+N = 1%, f = 1kHz, R_L = 8Ω		—	8.4	—	
		THD+N = 10%, f = 1kHz, R_L = 8Ω		—	10.4	—	
THD+N	Total Harmonic Distortion plus Noise	P_O = 5W, f = 1kHz, R_L = 8Ω		—	0.05	—	%
I_{DD}	Quiescent Current	(No Load)		—	15	30	mA
I_{SD}	Supply Quiescent Current in Shutdown Mode	Shutdown = 0V		—	15	25	μA
I_{MUTE}	Mute Current	(No Load)		—	11	—	mA
$R_{DS(ON)}$	Drain-Source On-State Resistance	I_O = 0.5A, T_J = +25°C	High Side	—	210	—	mΩ
			Low Side	—	210	—	
			Total	—	420	—	
η	Efficiency	Po=10W		—	92	—	%
PSRR	Power Supply Ripple Rejection Ratio	$1V_{PP}$ Ripple, f = 1kHz, Inputs AC-Coupled to Ground		—	-70	—	dB
T_{ON}	Turn-on Time	$\overline{SD}$ from “L” to “H”		—	25	—	ms
f_{OSC}	Oscillator frequency	—		—	300	—	kHz
V_N	Output Integrated Noise	20Hz to 22kHz, A-Weighting, SSM OFF, Gain = 32dB		—	170	—	μVrms
CS	Crosstalk	P_O = 3W, R_L = 8Ω, f = 1kHz		—	-90	—	dB
SNR	Signal to Noise Ratio	Maximum Output at THD+N < 0.5%, f = 1kHz		—	95	—	dB
G_V	Closed Loop Gain	—		—	32	—	dB
$\|V_{OS}\|$	Output Offset Voltage (measured differentially)	INN and INP Connected Together		—	—	50	mV
V2P5	2.5V Bias Voltage	No Load		—	2.5	—	V
AVDD	Internal Analog Supply Voltage	V_{CC} = 6V to 15V		—	5.2	5.7	V
V_{IH}	Input High Level	—		3	—	—	V
V_{IL}	Input Low Level	—		—	—	0.5	V
OTS	Over-Temperature Shutdown	—		—	160	—	°C
OTH	Thermal Hysteresis	—		—	45	—	°C

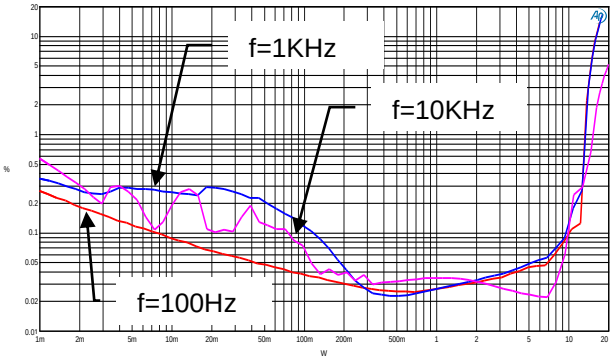
Typical Performance Characteristics

(V_{CC} = 12, R_L = 8Ω, G_V = 32dB, T_A = +25°C, V_{CC} = 15V, R_L =8Ω, unless otherwise specified.)

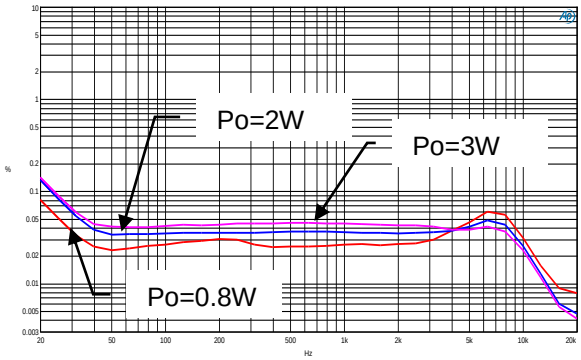
1. THD+N vs Power (Vcc=12V)



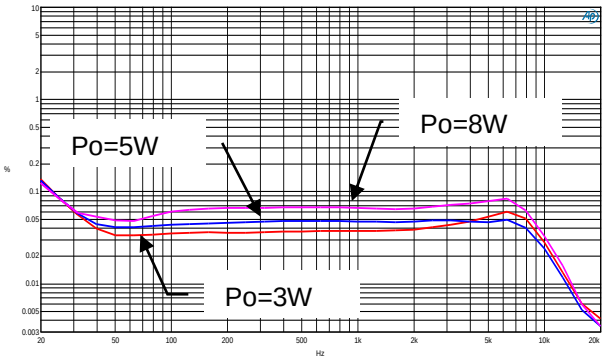
2. THD+N vs Power (Vcc=15V)



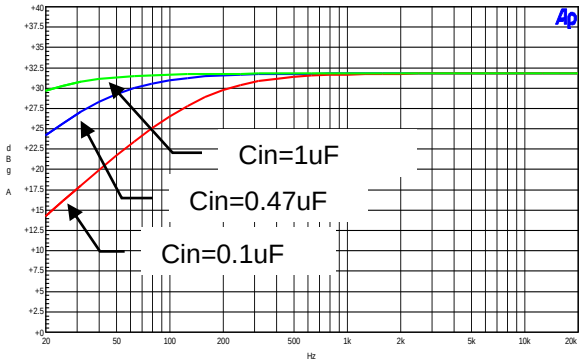
3. THD+N vs Frequency (Vcc=12V)



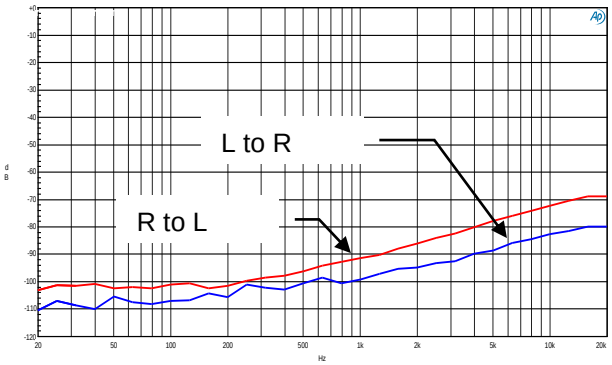
4. THD+N vs Frequency (Vcc=15V)



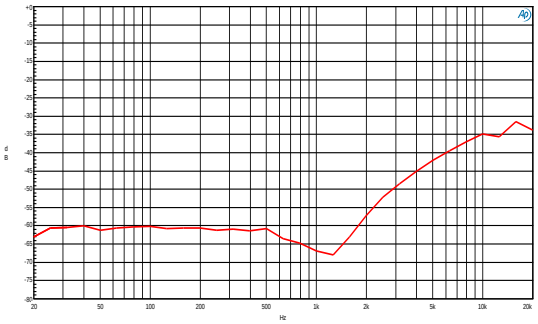
5. Frequency Response(Vcc=12V,Gv=32dB,Rl=8Ω)



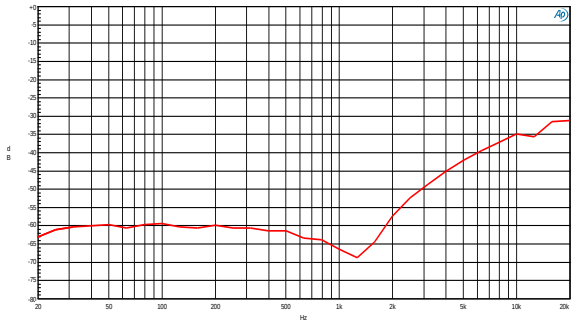
6. Crosstalk(Vcc=12V,Rl=8Ω)



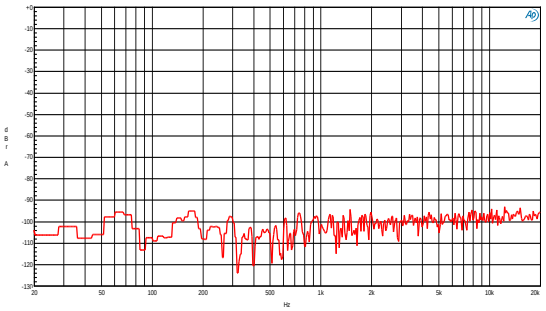
7. PSRR(Vcc=12V,Gv=32dB,Rl=8Ω)



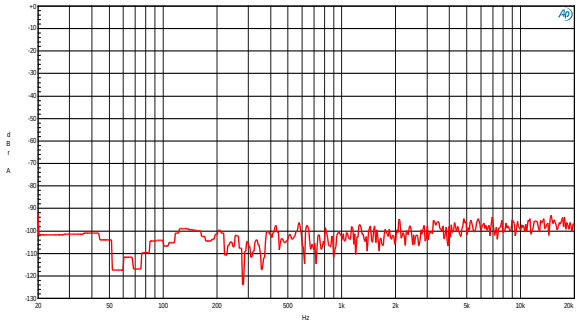
PSRR(Vcc=15V,Gv=32dB,Rl=8Ω)



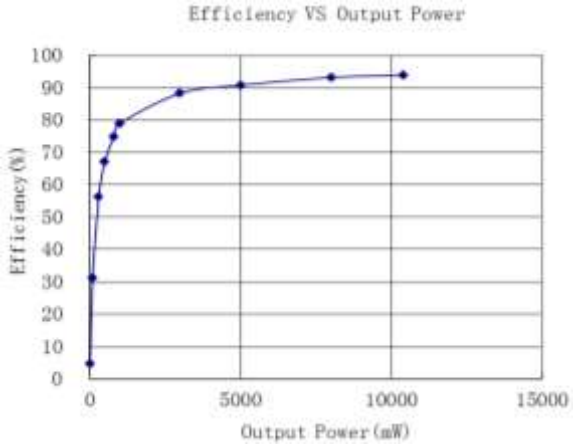
8. Noise Floor(Vcc=12V,Gv=32dB,Rl=8Ω)



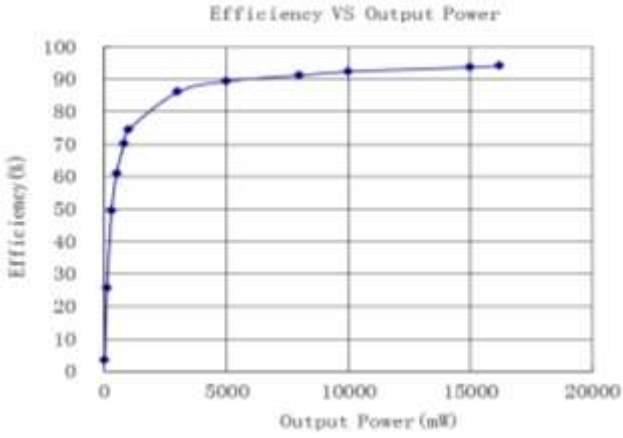
Noise Floor(Vcc=15V,Gv=32dB,Rl=8Ω)



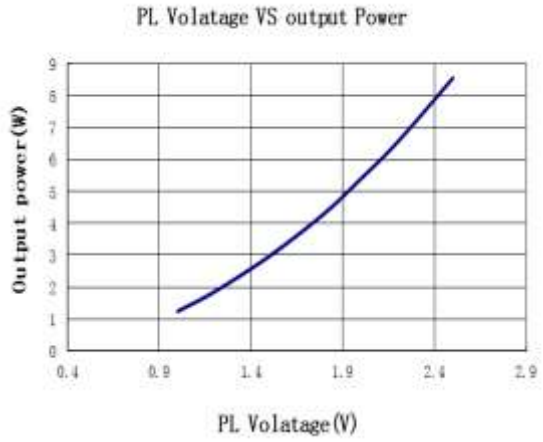
9. Efficiency vs Output Power(Vcc=12V)



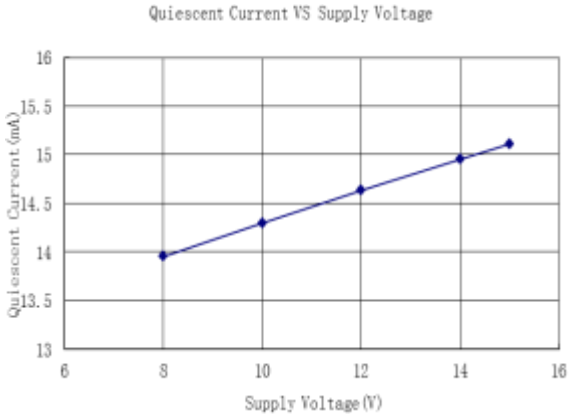
Efficiency vs Output Power(Vcc=15V)



11. PL voltage vs output Power

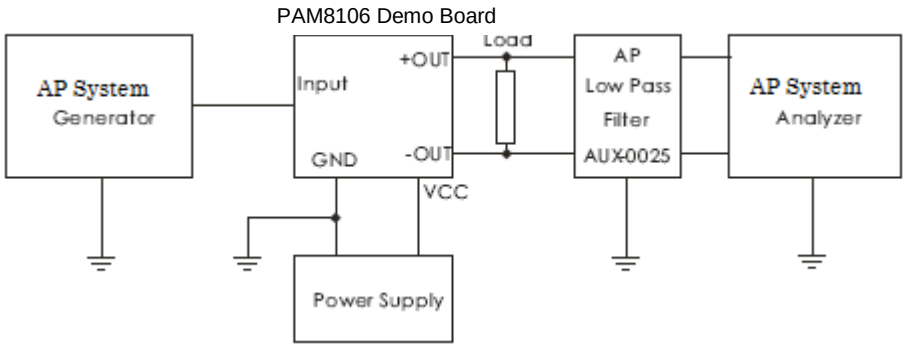


12. Quiescent Current vs Supply Voltage



Application Information

Test Setup for Performance Testing



Notes: 4. The AP AUX-0025 low pass filter is necessary for class-D amplifier measurement with AP analyzer.
5. Two 22μH inductors are used in series with load resistor to emulate the small speaker for efficiency measurement.

MUTE Operation

The MUTE pin is an input for controlling the output state of the PAM8106. A Logic-High on this pin disables the outputs and Logic-Low enables the outputs. This pin may be used as a quick disable or enable of the outputs without a volume fade.

Shutdown Operation

The PAM8106 employs a shutdown operation mode to reduce supply current to the absolute minimum level during periods of non-use to save power. The $\overline{SD}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{SD}$ low causes the outputs to mute and the amplifier to enter a low-current state. $\overline{SD}$ should never be left unconnected to prevent the amplifier from unpredictable operation.

For the best power-off pop performance, the amplifier should be set in shutdown mode prior to removing the power supply voltage.

Internal 2.5V Bias Generator Capacitor Selection

The internal 2.5V bias generator (V2P5) provides the internal bias for the preamplifier stage. The external input capacitors and this internal reference allow the inputs to be biased within the optimal common-mode range of the input preamplifiers.

The selection of the capacitor value on the V2P5 terminal is critical for achieving the best device performance. During startup or recovery from shutdown state, the V2P5 capacitor determines the rate at which the amplifier starts up. When the voltage on the V2P5 capacitor equals 0.75 x V2P5, or 75% of its final value, the device turns on and the Class-D outputs start switching. The startup time is not critical for the best de-pop performance since any heard pop sound is the result of the Class-D output switching-on other than that of the startup time. However, at least a 0.47μF capacitor is recommended for the V2P5 capacitor.

Another function of the V2P5 capacitor is to filter high frequency noise on the internal 2.5V bias generator.

Power Supply Decoupling, C_S

The PAM8106 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) as low as possible. Power supply decoupling also prevents ringing oscillations caused by long lead between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series resistance (ESR) ceramic capacitor, typically X7R type 1μF, is recommended, placing as close as possible to the device's V_{CC} lead. To filter lower frequency noises, a large aluminum electrolytic capacitor of 10μF or greater is recommended, placing near the audio power amplifier. The 10μF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs.

BSN and BSP Capacitors

The full H-bridge output stages use NMOS transistors only. They therefore require bootstrap capacitors for the high side of each output to turn on correctly. An at least 220nF ceramic capacitor, rated for at least 25V, must be connected from each output to its corresponding bootstrap input. Specifically, one 220nF capacitor must be connected from xOUTP to xBSP, and another 220nF capacitor from xOUTN to xBSN. It is recommended to use 1μF BST capacitor to replace 220nF or lower than 100Hz applications.

Application Information (Continued)

VCLAMP Capacitors

To ensure that the maximum gate-to-source voltage for the NMOS output transistors not exceeded, an internal regulators are used to clamp the gate voltage. A 1µF capacitors must be connected from VCLAMP to ground and must be rated for at least 25V. The voltages at the VCLAMP terminals vary with V_{CC} and may not be used to power any other circuitry.

Internal Regulated 5-V Supply (AVDD)

The AVDD terminal is the output of an internally generated 5V supply, used for the oscillator, amplifier, power limit circuitry and logic control circuitry. It requires a 0.1µF to 1µF capacitor, placed very close to the pin to ground to keep the regulator stable. The regulator may not be used to power any external circuitry.

Differential Input Power Limit

The differential input stage of the amplifier eliminates noises that appear on the two input lines of the channel. To use the PAM8106 with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the PAM8106 with a single-ended source, AC ground the INP input through a capacitor equal in value to the input capacitor on INN and apply the audio source to the INN input. In a single-ended input application, the INP input should be AC grounded at the audio source other than at the device input for best noise performance.

Using Low-ESR Capacitors

Low-ESR capacitors are recommended throughout this application section. A real (with respect to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves as an ideal capacitor.

Short-Circuit Protection

The PAM8106 has short circuit protection circuitry on the outputs to prevent damage to the device when output-to-output shorts, output-to-GND shorts, or output-to-VCC shorts occur. Once a short-circuit is detected on the outputs, the output drive is immediately disabled. This is a latched fault and must be reset by cycling the voltage on the $\overline{SD}$ pin to a logic low and back to the logic high state for normal operation. This will clear the short-circuit flag and allow for normal operation if the short was removed. If the short was not removed, the protection circuitry will again activate.

Thermal Protection

Thermal protection on the PAM8106 prevents damage to the device when the internal die temperature exceeds 160°C. There is a ±15 degree tolerance on this trip point from device to device. Once the die temperature exceeds the set thermal point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 50°C. The device begins normal operation at this point without external system intervention.

Spread Spectrum Modulation

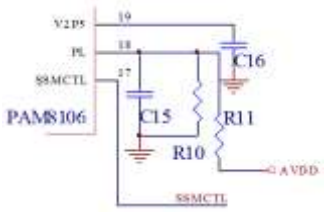
The PAM8106 has built in Spread spectrum modulation control of the oscillator frequency to improve EMI performance, while removing the need to use expensive inductance in the audio output path. The spread spectrum feature can be enabled by setting a Logic-Low to SSMCTL pin, or disabled by setting a Logic-High to SSMCTL pin.

Power Limit

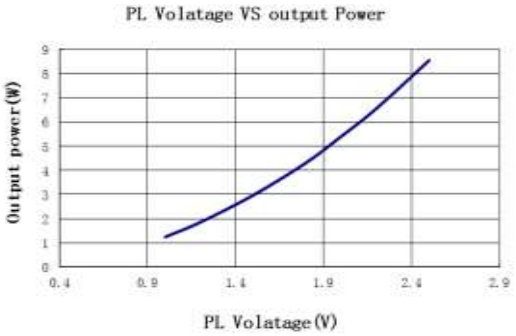
The voltage at PL pin can used to limit the power to levels below that which is possible based on the supply rail. Add a resistor from PL to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Also add a 1µF capacitor from PL pin to ground. The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The gain of Class-D amplifier will automatic reduced if the output power higher than setting value to make output power less than limited value and also provide good sound quality.

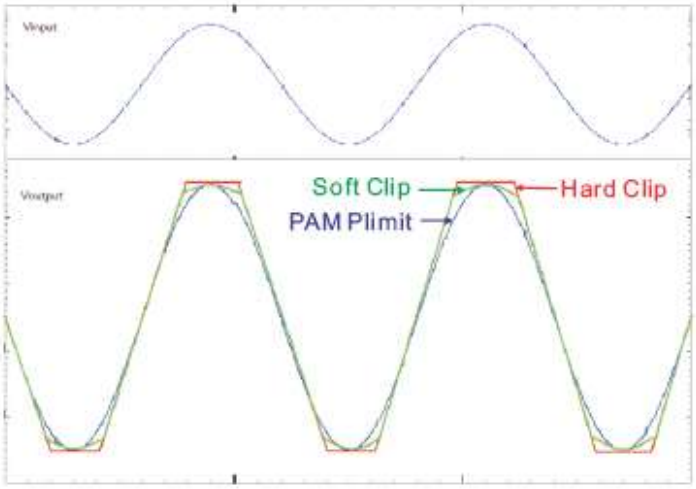
The output power setting by the resistor value (R10, R11) of PL pin is described as below.

System test set up: V_{CC} = 12V, R_{LOAD} = 8Ω, sine wave 1Khz, AVdd=5.2V



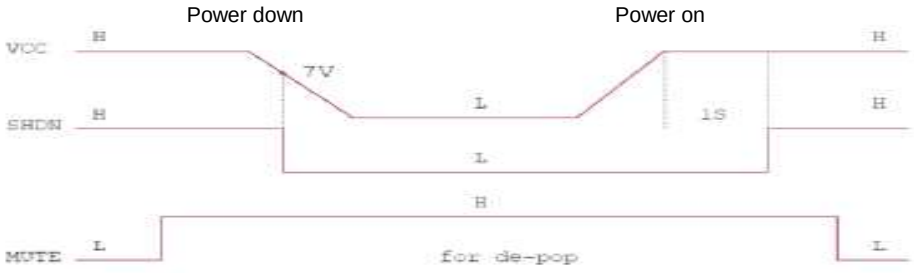
R11 (Ω)	R10 (Ω)	PL (V)	PL (W)
10K	3K	1.2026	1.873
10K	3.6K	1.3819	2.515
10K	4.3K	1.5704	3.281
10K	5.6K	1.877	4.738
10K	6.8K	2.1087	6.07
10K	8.2K	2.3453	7.554
10K	9.1K	2.4884	8.562





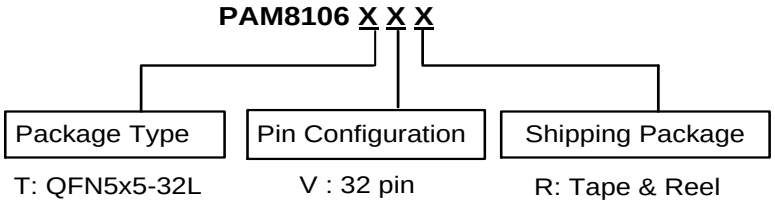
Power Up/Down Sequence

The PAM8106 employs a shutdown operation mode to reduce supply current to the absolute minimum level during periods of non-use to save power. The $\overline{SD}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{SD}$ low causes the outputs to mute and the amplifier to enter a low-current state. $\overline{SD}$ should never be left unconnected to prevent the amplifier from unpredictable operation. Suggest PL starting voltage is greater than 4.5V.



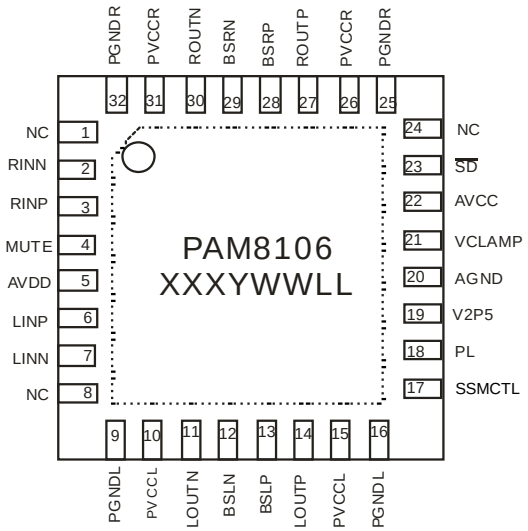
Power-down and Start-up sequences as recommended.

Ordering Information



Part Number	Part Marking	Package Type	Standard Package
PAM8106TVR	PAM8106 XXXYWWLL	W-QFN5050-32 (Standard)	3,000 Units/Tape & Reel

Marking Information

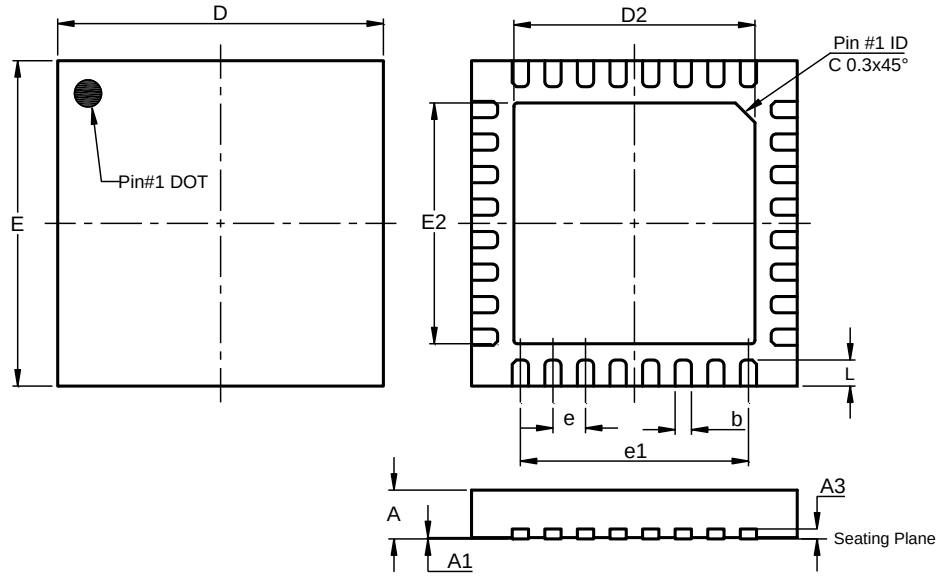


XXX : Internal Code
Y : Year (0 ~9)
WW : Week (01 ~53)
LL : Internal Code

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN5050-32 (Standard)



W-QFN5050-32 (Standard)			
Dim	**Min**	**Max**	**Typ**
A	0.55	0.80	0.75
A1	0.00	0.05	--
A3	0.203 REF		
b	0.20	0.30	0.25
D	4.95	5.05	5.00
D2	3.65	3.75	3.70
E	4.95	5.05	5.00
E2	3.65	3.75	3.70
e	0.50 BSC		
e1	3.50 REF		
L	0.35	0.45	0.40
All Dimensions in mm			

Suggested Pad Layout

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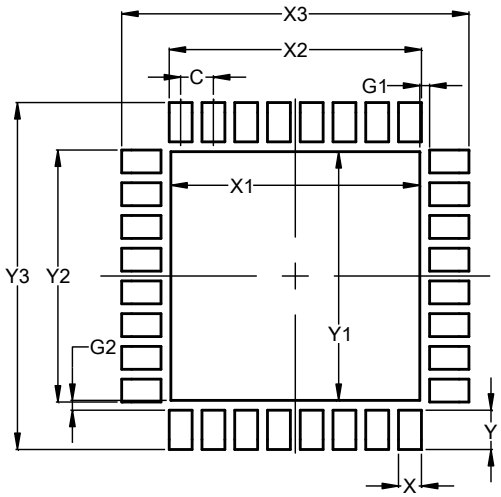
W-QFN5050-32 (Standard)



Dimensions	Value (in mm)
C	0.500
G1	0.150
G2	0.150
X	0.350
X1	3.800
X2	3.850
X3	5.300
Y	0.600
Y1	3.800
Y2	3.850
Y3	5.300

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