PCN Number:	20190521001	PCN Date:	June 24, 2019
Title:	Datasheet for DS90UB948-Q1 and DS90UH948-Q1		
Customer Contact:	PCN Manager	Dept:	Quality Services

Change Type:

☐	Assembly Site	☐	Design	☐	Wafer Bump Site
☐	Assembly Process	☒	Data Sheet	☐	Wafer Bump Material
☐	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

TEXAS INSTRUMENTS

DS90UB948-Q1

SNLS477B – OCTOBER 2014 – REVISED NOVEMBER 2018

Changes from Revision A (January 2016) to Revision B **Page**

- Changed PCLK frequency to support higher speed 192 MHz. 1
- Changed "1.2 V" to "1.25 V" at top of DS90Ux940 Deserializer in Typ App 1
- Simplified the typical application by removing the power supplies nodes. 1
- Removed bolded pin description name for power supplies. 5
- Added new pin description content to the *Pin Functions* table 5
- Changed the description from VDDIO to V(I2C). 6
- Specified in current instead of resistor for all pulldown resistor 6
- Removed 200-µA minimum ramp time for PDB pin description. 7
- Added the description to clarify the INTB_IN that this pin can be an output driver. 7
- Changed pin names from CAP_PLL0 and CAP_PLL1 to RES0 and RES1 respectively. 9
- Removed tablenote from the *Absolute Maximum Ratings* table: For soldering specifications, see product folder at www.ti.com and SNOA549 11
- Added Military/Aerospace tablenote to the *Absolute Maximum Ratings* table 11
- Changed supply voltage maximum for the VDD33 from: 4 V to: 3.96 V 11
- Changed VDD12 abs max from 1.8V to 1.44V. 11
- Changed supply voltage for the VDDIO from: 4 V to: 3.96 V 11
- Added the Added the open-drain voltage, CML output voltage, and FPD-Link III input voltage parameters to the Absolute Maximum Ratings table , open-drain voltage, CML output voltage, and FPD-Link III input voltage parameters to the *Absolute Maximum Ratings* table 11
- Added test conditions to the LVCMOS I/O voltage parameter 11
- Spelled out all GPIOs pin name. 11
- Combined the ESD ratings into one *ESD Ratings* table 11
- Removed VDD18 test condition from the supply voltage parameter 11

- Added the open-drain voltage parameter to the *Recommended Operating Conditions* table 11
- Changed open LDI clock frequency (dual link) maximum from: 170 MHz to: 192 MHz 11
- Added the local I2C frequency parameter to the *Recommended Operating Conditions* table 11
- Added test conditions to the supply noise parameter 12
- Changed the total power consumption, normal operation test conditions 12
- Changed "VDD12 = 1.2 V" to "VDD12 = 1.2 V" 12
- Removed the checkerboard vs. PRBS pattern condition and combined typical and worst case together. 12
- Added current specs for PCLK 192 MHz. 12
- Deleted typical value for Vih and Vil in 3.3V LVCMOS I/O. 12
- Split out the test conditions in the 3.3-V and 1.8-V LVCMOS I/O parameters 12
- Added strap pin input current parameter to the *DC Electrical Characteristics* table 13
- Deleted typical value for Vih and Vil in 1.8V LVCMOS I/O. 13
- Deleted typical value for Vih and Vil in serial control bus 13
- Added test conditions to the input high level and input low level parameters 13
- Changed "complimentary" to "complementary" 14
- Removed tablenote from the *AC Electrical Characteristics* table: This parameter is specified by characterization and is not tested in production. 15
- Changed differential output eye height from: >300 mV to: 300 mV 15
- Removed tablenote from the *Timing Requirements* table: Parameter is specified by bench characterization and is not tested in production. 16
- Changed C_b fast mode plus maximum value from: 550 pF to: 200 pF 16
- Removed tablenote from the *Switching Characteristics* table: Parameter is specified by bench characterization and is not tested in production. 17
- Changed *Deserializer Eye Diagram* graph in the *Typical Characteristics* section 21
- Added paragraph explains HSCC mode. 25
- Changed transmission distance section and insertion loss table. 31
- Changed PCLK frequncy from 96 MHz to 192 MHz in the diagram "2-lane FPD-link Input, Link OpenLDI Output" in the *Data-Path Configurations* graphic 41
- Changed the resistor ratio value for both the *Configuration Select (MODE_SEL0)* and *Configuration Select (MODE_SEL1)* tables. 42
- Deleted repeated first paragraph LUT contents. 48
- Changed pullup power supply node from "VDDIO" to "V(I2C). 51

- Updated register table format to the latest TI standards in the *Register Maps* section 54
- Changed input value from 1.2 V to 1.2 V in typical application drawings 85
- Updated STP diagram. 86
- Updated Coax diagram 87
- Simplified the diagram by removing power supplies node. 88
- Added new design parameters to the *Design Requirements* section 88
- Changed VDD12 in Design Parameters 1.2 to 1.2 88
- Changed *CML Interconnect Guidelines* section title to *FPD-Link III Interconnect Guidelines* 89
- Added *AV Mute Prevention* section 89
- Added *Prevention of I2C Errors During Abrupt System Faults* section 90
- Moved the *Power Sequence* graphic to the *Power Supply Recommendations* 91
- Removed power supplies columns and changed the parameters in the *Power-Up Sequencing Constraints* table according to the diagram. 91
- Moved the *PCB Layout and Power System Considerations* content to the *Layout Guidelines* section 93
- Added *Ground* and *Routing FPD-Link III Signal Traces* sections to the *Layout* section 93

- Added Added FPD-Link training videos to the *Related Documentation* section. 97

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The datasheet number will be changing.

Device Family	Change From:	Change To:
DS90UB948-Q1	SNLS477A	SNLS477B
DS90UH948-Q1	SNLS473A	SNLS473B

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/DS90UB948-Q1

http://www.ti.com/product/DS90UH948-Q1

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this PCN:

None.

Product Affected:

DS90UB948TNKDTQ1	DS90UB948TNKDRQ1	DS90UH948TNKDTQ1	DS90UH948TNKDRQ1

For questions regarding this notice, e-mails can be sent to the contacts shown below or your local Field Sales Representative.

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