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August 2016

# FAN48617
# Fixed-Output Synchronous TinyBoost® Regulator

## Features

- Input Voltage Range: 2.7 V to 4.5 V
- Output Voltage: 5.0 V
- 1000 mA Max. Load Capability
- PWM Only
- Up to 97% Efficient
- Forced Pass-Through Operation via EN Pin
- Internal Synchronous Rectification
- True Load Disconnect
- Short-Circuit Protection
- External Components: 2016 (Metric) 1 µH Inductor, 0402 Case Size Input / Output Capacitors

## Applications

- Class-D Audio Amplifier
- Boost for Low-Voltage Li-Ion Batteries
- Smart Phones, Tablets, Portable Devices
- RF Applications
- NFC Applications

## Description

The FAN48617 is a low-power PWM only boost regulator designed to provide a minimum voltage-regulated rail from a standard single-cell Li-Ion battery and advanced battery chemistries. Even below the minimum system battery voltage, the device maintains the output voltage regulation for an output load current of 1000 mA. The combination of built-in power transistors, synchronous rectification, and low supply current suit the FAN48617 for battery-powered applications.

The FAN48617 is available in a 9-bump, 0.4 mm pitch, (1.215 x 1.215 mm) Wafer-Level Chip-Scale Package (WLCSP).

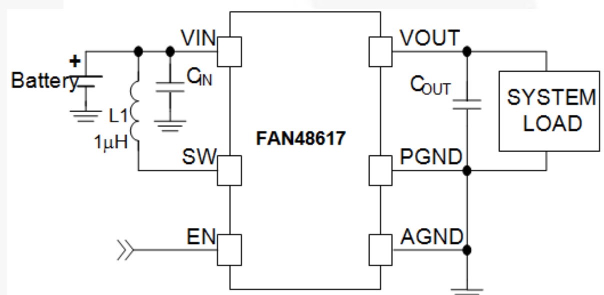



**Figure 1. Typical Application**

## Ordering Information

| Part Number | $V_{OUT}$ | Operating Temperature | Package | Packing | Device Marking |
|---|---|---|---|---|---|
| FAN48617UC50X | 5.0 V | -40°C to 85°C | 9-Bump, 0.4 mm Pitch, WLCSP Package | Tape and Reel | K2 |

## Block Diagram

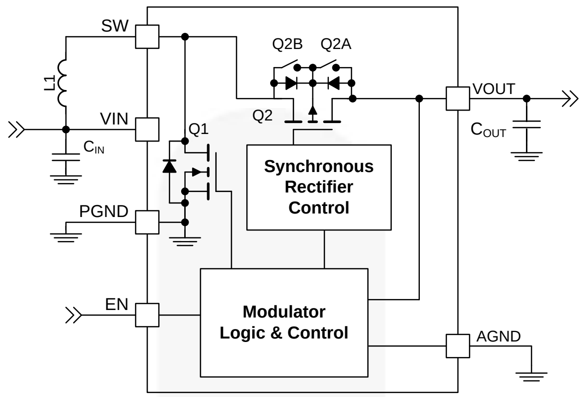



**Figure 2. IC Block Diagram**

**Table 1. Recommended Components**

| Component | Description | Vendor | Parameter | Typ. | Unit |
|---|---|---|---|---|---|
| L1 | 20%, 3.9 A, 2016, 1.0 mm Height | DFE201610E-1R0M TOKO | Inductance | 1 | µH |
| | | | DCR (Series R) | 48 | mΩ |
| $C_{IN}$ | 20%, 6.3 V, X5R, 0402 (1005) | C1005X5R0J106M050BC TDK | Capacitance | 10 | µF |
| $C_{OUT}$ 1[(1)] | 20%, 6.3 V, X5R, 0402 (1005) | C1005X5R0J106M050BC TDK | Capacitance | 2 x 10 | |
| $C_{OUT}$ 2[(2)] | 20%, 6.3 V, X5R, 0402 (1005) | C1005X5R0J106M050BC TDK | Capacitance | 3 x 10 | |

**Notes:**

1. For applications with $I_{OUT}$ < 500 mA use $C_{OUT}$ 1.
2. For applications with 500 mA ≤ $I_{OUT}$ < 1000 mA use $C_{OUT}$ 2.

## Pin Configuration

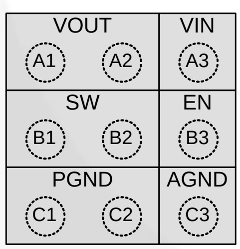



**Figure 3. Top View**

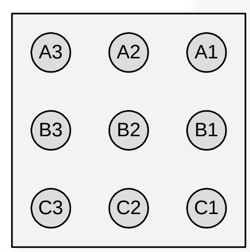



**Figure 4. Bottom View**

## Pin Definitions

| Pin # | Name | Description |
|---|---|---|
| A1, A2 | VOUT | **Output Voltage**. This pin is the output voltage terminal; connect directly to $C_{OUT}$. |
| A3 | VIN | **Input Voltage**. Connect to Li-Ion battery input power source and $C_{IN}$. |
| B1, B2 | SW | **Switching Node**. Connect to inductor. |
| B3 | EN | **Enable**. When this pin is HIGH, the circuit is enabled. After part is engaged, pin forces part into Forced-Pass-Through Mode when EN pin is pulled LOW. |
| C1, C2 | PGND | **Power Ground**. This is the power return for the IC. $C_{OUT}$ capacitor should be returned with the shortest path possible to these pins. |
| C3 | AGND | **Analog Ground**. This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin – connect to PGND at a single point. |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IN}$ | Voltage on VIN Pin | | -0.3 | 6.0 | V |
| $V_{OUT}$ | Voltage on VOUT Pin | | | 6.0 | V |
| $V_{SW}$ | SW Node | DC | -0.3 | 6.0 | V |
| | | Transient: 10 ns, 3 MHz | -1.0 | 8.0 | |
| $V_{CC}$ | Voltage on Other Pins | | -0.3 | 6.0[(3)] | V |
| ESD | Electrostatic Discharge Protection Level | Human Body Model, ANSI/ESDA/JEDEC JS-001-2012 | 2.0 | | kV |
| | | Charged Device Model per JESD22-C101 | 1.0 | | |
| $T_J$ | Junction Temperature | | -40 | +150 | °C |
| $T_{STG}$ | Storage Temperature | | -65 | +150 | °C |
| $T_L$ | Lead Soldering Temperature, 10 Seconds | | | +260 | °C |

**Note:**

3. Lesser of 6.0 V or $V_{IN}$ + 0.3 V.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{IN}$ | Supply Voltage | 2.7 | 4.5 | V |
| $I_{OUT}$ | Maximum Output Current | 1000 | | mA |
| $T_A$ | Ambient Temperature | -40 | +85 | °C |
| $T_J$ | Junction Temperature | -40 | +125 | °C |

## Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards with vias in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature, $T_{J(max)}$, at a given ambient temperature, $T_A$.

| Symbol | Parameter | Typical | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | Junction-to-Ambient Thermal Resistance | 50 | °C/W |

## Electrical Specifications

Recommended operating conditions, unless otherwise noted, circuit per Figure 1, $V_{OUT}$ = 5.0 V. Typical, minimum and maximum values are given at $V_{IN}$ = 3.6 V, $T_A$ = 25˚C, -40°C, and +85°C.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| $I_Q$ | $V_{IN}$ Quiescent Current | $I_{OUT}$ = 0 mA, EN = 1.8 V, No Switching | | 95 | | µA |
| | | Forced Pass-Through EN = 0 V, $V_{OUT} = V_{IN}$ | | 3.5 | | |
| $V_{UVLO}$ | Under-Voltage Lockout | $V_{IN}$ Rising | | 2.20 | | V |
| $V_{UVLO\_HYS}$ | Under-Voltage Lockout Hysteresis | | | 150 | | mV |
| **Inputs** | | | | | | |
| $V_{IH}$ | Enable HIGH Voltage | | 1.05 | | | V |
| $V_{IL}$ | Enable LOW Voltage | | | | 0.4 | V |
| **Outputs** | | | | | | |
| $V_{REG}$ | Output Voltage Accuracy DC[4] | 2.7 V ≤ $V_{IN}$ ≤ 4.5 V | -2 | | +2 | % |
| **Timing** | | | | | | |
| $f_{SW}$ | Switching Frequency | $I_{OUT}$ = 300 mA | 1.8 | 2.3 | 2.8 | MHz |
| $t_{SS}$[5] | EN HIGH to 95% of Regulation | $I_{OUT}$ = 150 mA | | 425 | | µs |
| $t_{RST}$[5] | FAULT Restart Timer | | | 20 | | ms |
| **Power Stage** | | | | | | |
| $R_{DS(ON)N}$ | N-Channel Boost Switch $R_{DS(ON)}$ | | | 63 | | mΩ |
| $R_{DS(ON)P}$ | P-Channel Sync. Rectifier $R_{DS(ON)}$ | | | 52 | | mΩ |

**Notes:**

4. DC $I_{LOAD}$ from 0 to 1000 mA. $V_{OUT}$ measured from mid-point of output voltage ripple. Effective capacitance of $C_{OUT} \geq$ 6.3 µF.
5. Guaranteed by design and characterization; not tested in production.

## Typical Performance Characteristics

Unless otherwise specified; $V_{IN}$ = 3.6 V, $V_{OUT}$ = 5.0 V, $T_A$ = 25°C, and circuit according to Figure 1.
Components: $C_{IN}$ = 10 µF, $C_{OUT}$ = 3 x 10 µF (0402, X5R, 6.3 V, C1005X5R0J106M050BC), L1 = 1 µH (2016, 48 mΩ, DFE201610E-1R0M).

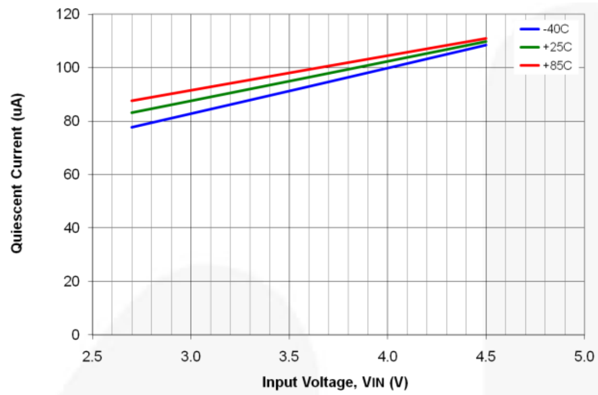



**Figure 5. Quiescent Current (No Switching) vs. Input Voltage and Temperature**

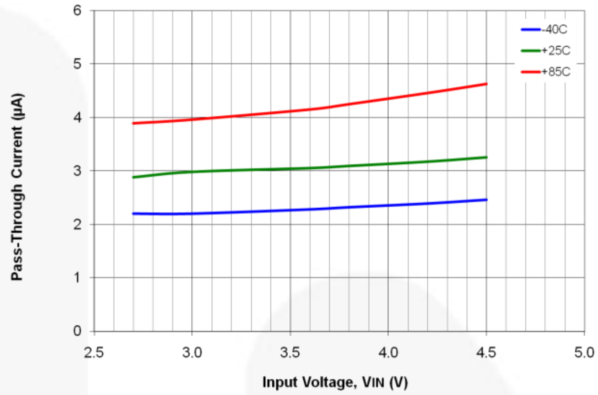



**Figure 6. Pass-Through Current vs. Input Voltage and Temperature**

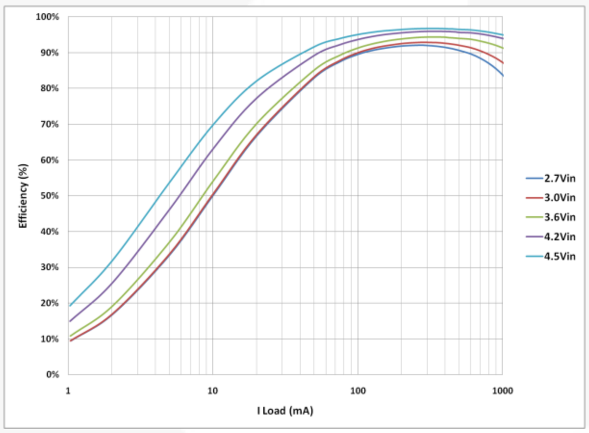



**Figure 7. Efficiency vs. Load Current and Input Voltage**

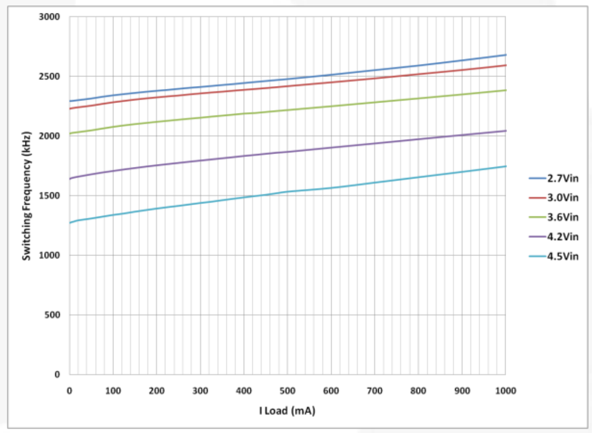



**Figure 8. Switching Frequency vs. Load Current and Input Voltage**

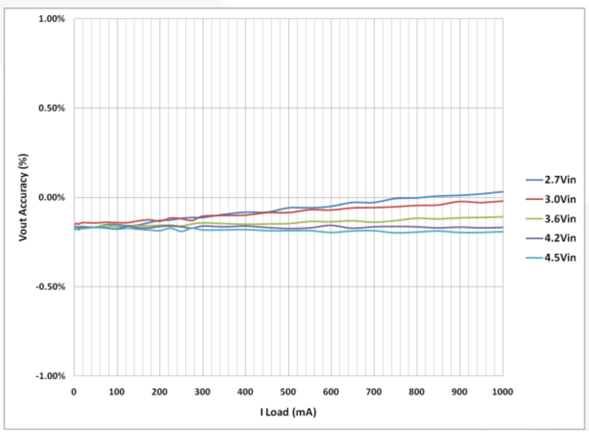



**Figure 9. Output Regulation vs. Load Current and Input Voltage**

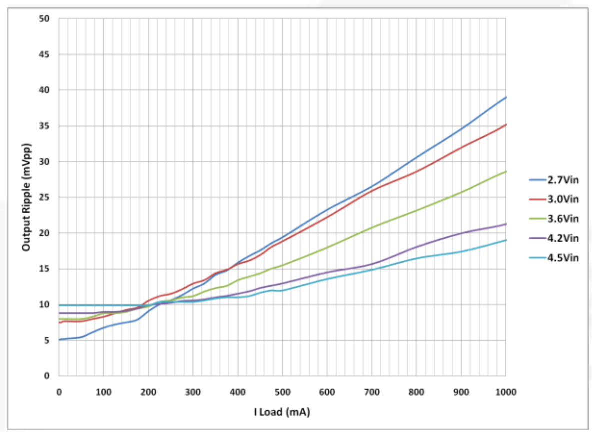



**Figure 10. Output Ripple vs. Load Current and Input Voltage**

## Typical Performance Characteristics

Unless otherwise specified; $V_{IN}$ = 3.6 V, $V_{OUT}$ = 5.0 V, $T_A$ = 25°C, and circuit and components according to Figure 1. Components: $C_{IN}$ = 10 µF, $C_{OUT}$ = 3 x 10 µF (0402, X5R, 6.3 V, C1005X5R0J106M050BC), L1 = 1 µH (2016, 48 mΩ, DFE201610E-1R0M).

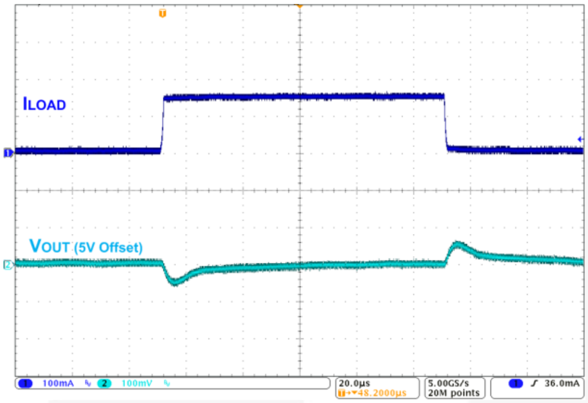



**Figure 11. Load Transient, 10 <-->150 mA, 1 µs Edge**

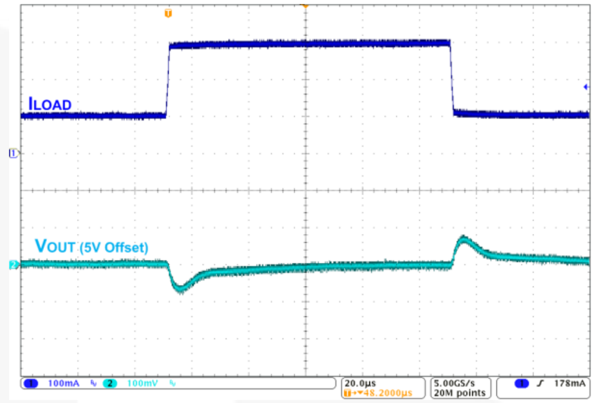



**Figure 12. Load Transient, 100 <--> 300 mA, 1 µs Edge**

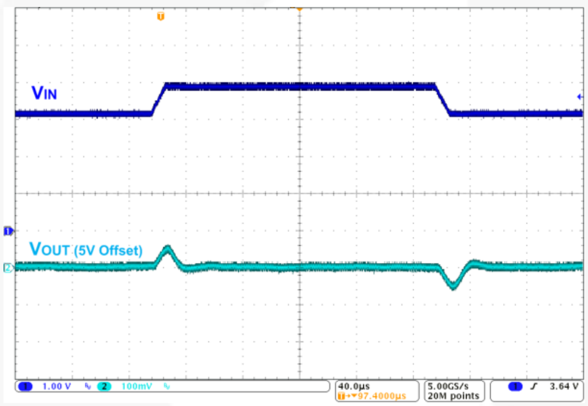



**Figure 13. Line Transient, 3.2 V <-->3.9 V, 10 µs Edge, 150 mA Load**

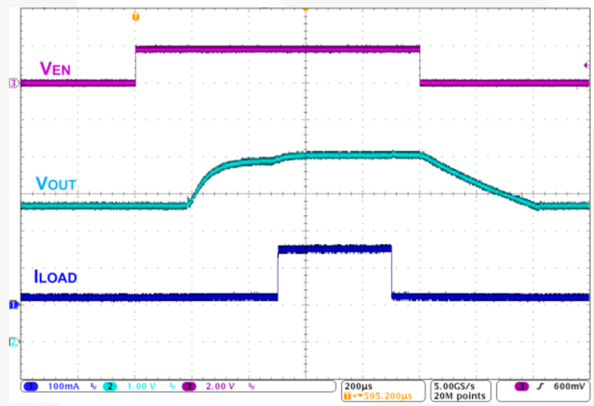



**Figure 14. Pass-Through Mode <--> Boost Mode with Load Transient, 20 <-->150 mA, 1 µs Edge**

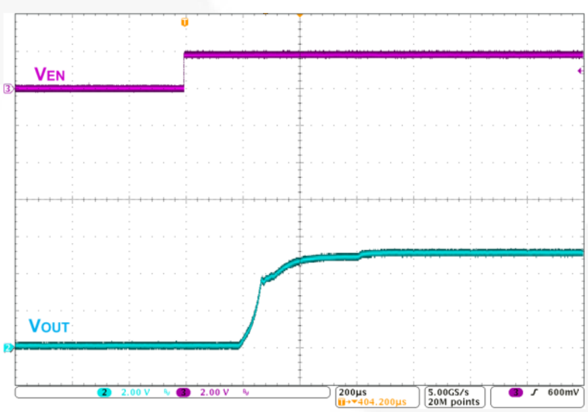



**Figure 15. Startup, 150 mA Load**

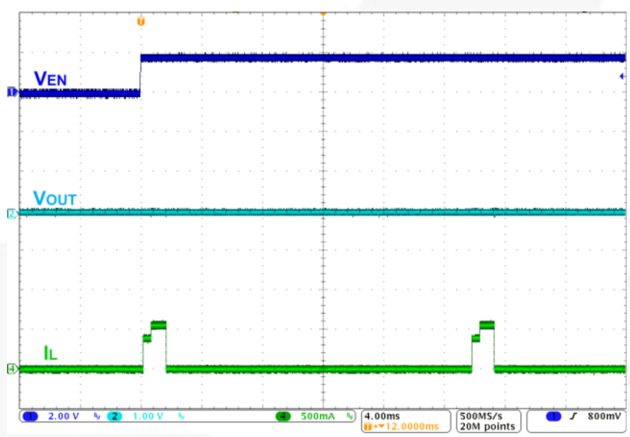



**Figure 16. Fault Restart**

## Circuit Description

FAN48617 is a synchronous PWM Only boost regulator. The regulator's Pass-Through Mode automatically activates when $V_{IN}$ is above the boost regulator's set point.

### Table 2. Operating Modes

| Mode | Description | Invoked When: |
|---|---|---|
| LIN | Linear Startup | $V_{IN} > V_{OUT}$ |
| SS | Boost Soft-Start | $V_{IN} < V_{OUT} < V_{OUT(TARGET)}$ |
| BST | Boost Operating Mode | $V_{OUT} = V_{OUT(TARGET)}$ |
| PT | Pass-Through Mode | $V_{IN} > V_{OUT(TARGET)}$ or when EN is pulled LOW after initial startup |

### Boost Mode Regulation

The FAN48617 uses a current-mode modulator to achieve excellent transient response.

### Table 3. Boost Startup Sequence

| Start Mode | Entry | Exit | End Mode | Timeout (µs) |
|---|---|---|---|---|
| LIN1 | $V_{IN} > V_{UVLO}$, EN=1 | $V_{OUT} > V_{IN}$-300 mV | SS | |
| | | Timeout | LIN2 | 512 |
| LIN2 | LIN1 Exit | $V_{OUT} > V_{IN}$-300 mV | SS | |
| | | Timeout | FAULT | 1024 |
| SS | LIN1 or LIN2 Exit | $V_{OUT}=V_{OUT(TARGET)}$ | BST | |
| | | Overload Timeout | FAULT | 64 |

### LIN Mode

When EN is HIGH and $V_{IN} > V_{UVLO}$, the regulator first attempts to bring $V_{OUT}$ within 300 mV of $V_{IN}$ by using the internal fixed-current source from VIN (Q2). The current is limited to the LIN1 set point.

If $V_{OUT}$ reaches $V_{IN}$-300 mV during LIN1 Mode, the SS Mode is initiated. Otherwise, LIN1 times out after 512 µs and LIN2 Mode is entered.

In LIN2 Mode, the current source is incremented. If $V_{OUT}$ fails to reach $V_{IN}$-300 mV after 1024 µs, a fault condition is declared and the device waits 20 ms to attempt an automatic restart.

### Soft-Start (SS) Mode

Upon the successful completion of LIN Mode ($V_{OUT} \geq V_{IN}$-300 mV), the regulator begins switching with boost pulses current limited to 50% of nominal level.

During SS Mode, if $V_{OUT}$ fails to reach regulation during the SS ramp sequence for more than 64 µs, a fault is declared. If large $C_{OUT}$ is used, the reference is automatically stepped slower to avoid excessive input current draw.

### Boost (BST) Mode

This is a normal operating mode of the regulator.

### Pass-Through (PT) Mode

The device allows the user to force the device in Forced Pass-Through Mode through the EN pin. If the EN pin is pulled HIGH, the device starts operating in Boost Mode. Once the EN pin is pulled LOW, the device is forced into Pass-Through Mode. To disable the device, the input supply voltage must be removed. The device cannot startup in Forced Pass-Through Mode *(see Figure 17)*. During startup, keep the EN pulled HIGH for at least 350 µs before pulling it LOW in order to make sure that the device enters Pass-Through Mode realiably

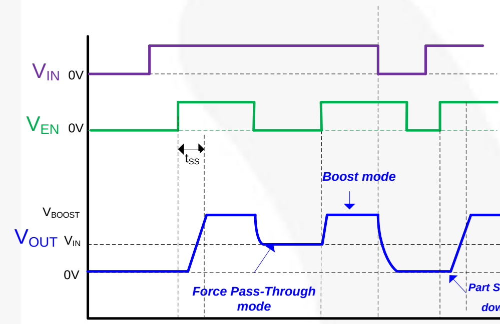



**Figure 17. Pass-Through Profile**

### Current Limit Protection

The FAN48617 has valley current limit protection in case of overload situations. The valley current limit will prevent high current from causing damage to the IC and the inductor. The current limit is halved during soft-start.

When starting into a fault condition, the input current will be limited by LIN1 and LIN2 current threshold.

### Fault State

The regulator enters Fault State under any of the following conditions:

- $V_{OUT}$ fails to achieve the voltage required to advance from LIN Mode to SS Mode.
- $V_{OUT}$ fails to achieve the voltage required to advance from SS Mode to BST Mode.
- Boost current limit triggers for 2 ms during BST Mode.
- $V_{IN} – V_{OUT} > 300$ mV; this fault can occur only after successful completion of the soft-start sequence.
- $V_{IN} < V_{UVLO}$.

Once a fault is triggered, the regulator stops switching and presents a high-impedance path between VIN and VOUT. After waiting 20 ms, an automatic restart is attempted.

### Over-Temperature

The regulator shuts down if the die temperature exceeds 150°C and restarts when the IC cools by ~20°C.

# Application Information

## Output Capacitance ($C_{OUT}$)

The effective capacitance ($C_{EFF}$[6]) of small, high-value ceramic capacitors decreases as their bias voltage increases, as illustrated in the graph below:

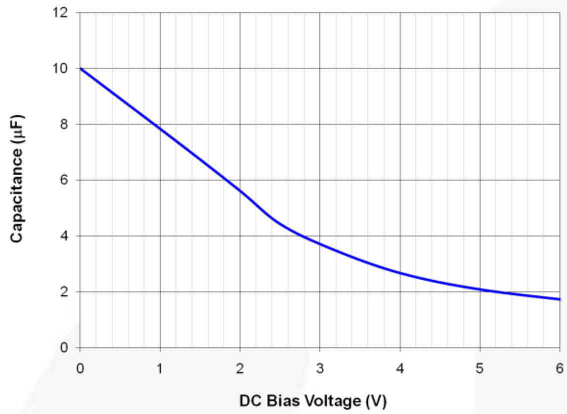



**Figure 18. $C_{EFF}$ for 10 µF, 0402, X5R, 6.3 V-Rated Capacitor (TDK C1005X5R0J106M050BC)**

FAN48617 is guaranteed for stable operation with the minimum value of $C_{EFF}$ ($C_{EFF(MIN)}$) outlined in Table 4.

**Table 4. Minimum $C_{EFF}$ Required for Stability**

| Operating Conditions | | | $C_{EFF(MIN)}$ (µF) |
|---|---|---|---|
| $V_{OUT}$ (V) | $V_{IN}$ (V) | $I_{LOAD}$ (mA) | |
| 5.0 | 2.7 to 4.5 | 0 to 500 | 4.2 |
| 5.0 | 2.7 to 4.5 | 0 to 1000 | 6.3 |

**Note:**

6. $C_{EFF}$ varies by manufacturer, capacitor material, and case size.

## Layout Recommendations

The layout recommendations below highlight various top-copper pours by using different colors.

To minimize spikes at VOUT, $C_{OUT}$ must be placed as close as possible to PGND and VOUT, as shown in Figure 19.

For best thermal performance, maximize the pour area for all planes other than SW. The ground pour, especially, should fill all available PCB surface area and be tied to internal layers with a cluster of thermal vias.

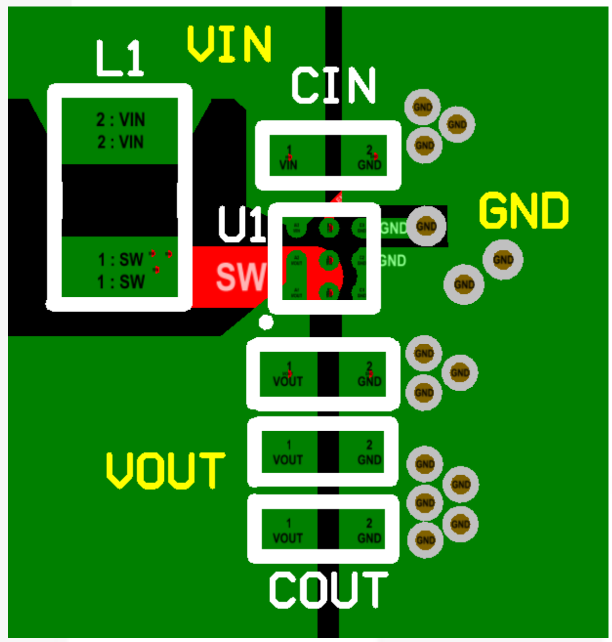
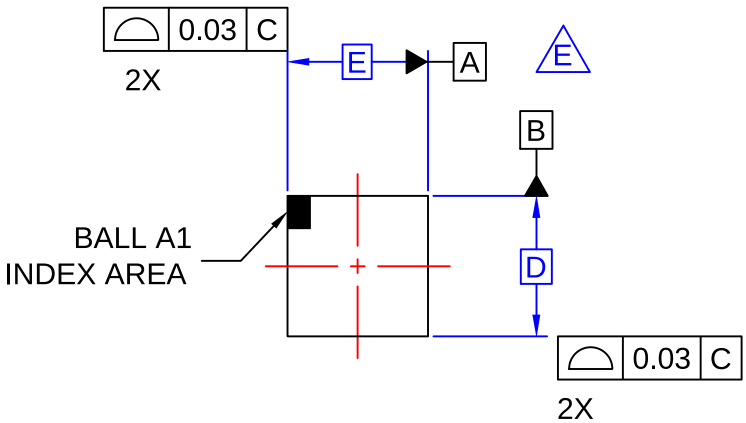



**Figure 19. Layout Recommendation**

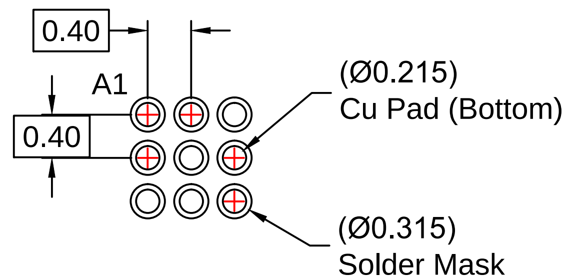
The table below pertains to MOD drawing on the following page.

## Product-Specific Package Dimensions

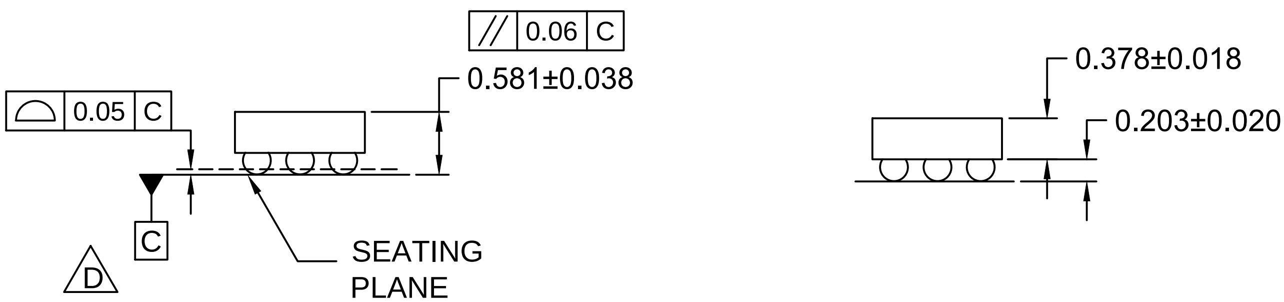
| Product | D | E | X | Y |
|---|---|---|---|---|
| FAN48617UC50X | 1.215 ±0.030 mm | 1.215 ±0.030 mm | 0.2075 mm | 0.2075 mm |




TOP VIEW




RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)




SIDE VIEWS

NOTES

A. NO JEDEC REGISTRATION APPLIES.

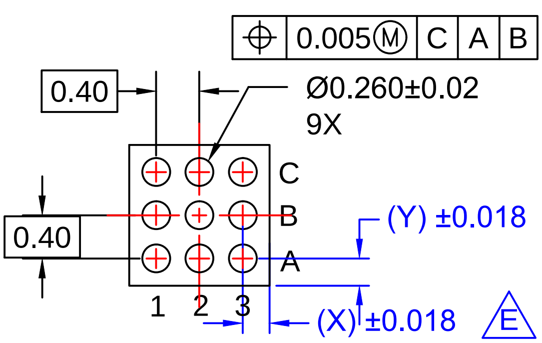
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 2009.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. FOR DIMENSIONS D,E,X, AND Y SEE PRODUCT DATASHEET.

F. DRAWING FILNAME: MKT-UC009Ak rev3




BOTTOM VIEW

ON Semiconductor

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