Audio Codec with Embedded SigmaDSP Processor

ADAV400

FEATURES

- Fully programmable audio digital signal processing (DSP) for enhanced sound processing
- Scalable digital audio delay line
  - Pool of 400 ms @ 48 kHz (200 ms for stereo channel)
- High performance, integrated analog-to-digital converters (ADCs) and digital-to-analog converters (DACs)
  - 1 stereo analog input (ADC)
  - 4 stereo analog inputs with mux-to-stereo ADC
  - 4 stereo (8-channel) analog outputs (DACs)
  - Dedicated headphone output with integrated amplifier
- Multichannel digital I/O
  - 8-channel I²S input and output modes
  - 8- and 16-channel TDM input and output modes
  - 2-channel (1 stereo) asynchronous I²S input with integrated sample rate converter (SRC), supporting sample rates from 5 kHz to 50 kHz
- Features SigmaStudio™, a proprietary graphical programming tool for fast development of custom signal flows
  - Includes various third-party audio algorithms
- I²C control interface
- Operates from 3.3 V (analog), 1.8 V (digital core), 3.3 V (digital interface)
- Features on-chip regulator for single 3.3 V operation
- 80-lead LQFP (14 mm × 14 mm)
- Temperature range: 0°C to 70°C

APPLICATIONS

- ATV and AV audio applications
  - TV audio processing
  - Set-top box (STB)
  - HTiB
- General audio enhancement

FUNCTIONAL BLOCK DIAGRAM

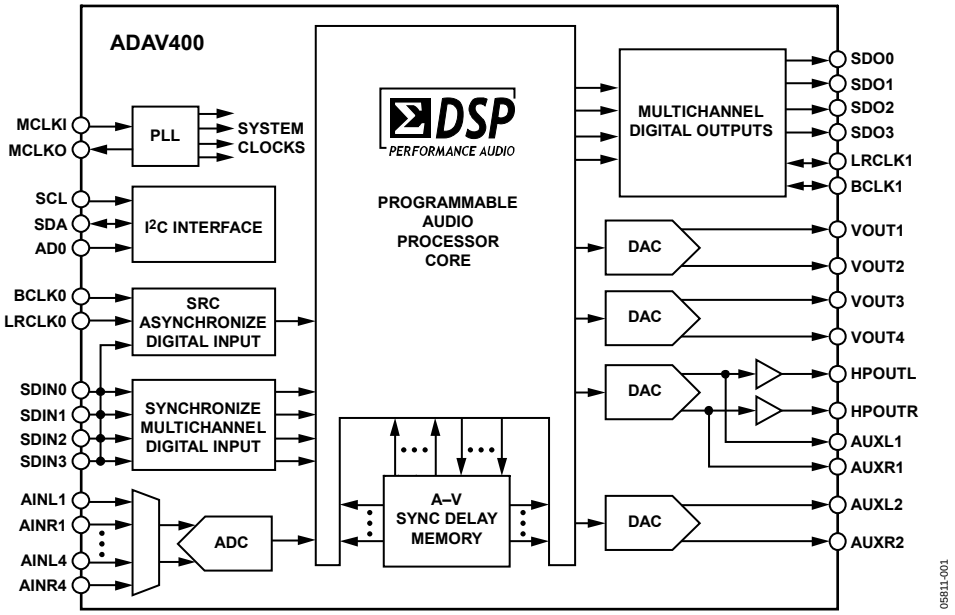

Figure 1.

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TABLE OF CONTENTS

REVISION HISTORY

7/07—Rev. 0 to Rev. A

Change to ADC Section, Total Harmonic Distortion + Noise ... 4
Change to DAC Outputs (Single-Ended),
Total Harmonic Distortion + Noise ... 4
Changes to Ordering Guide ... 35

1/06—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADAV400 is an enhanced audio processor. Integrating high performance analog and digital I/Os with a powerful, audio-specific, programmable core enables designers to differentiate their products through audio performance.

The audio processing core is based on Analog Devices SigmaDSP® technology featuring full 28-bit processing (56-bit in double precision mode); a sophisticated, fully programmable dynamics processor; and delay memory.

This technology allows the system designer to compensate for real-world limitations of speakers, amplifiers, and listening environments. This compensation results in a dramatic improvement of the perceived audio quality through speaker equalization, multiband compression and limiting, and third-party-branded algorithms.

The analog I/O integrates Analog Devices proprietary continuous time, multibit, sigma-delta (Σ-Δ) architecture. This integration brings a higher level of performance to systems that are required to meet system branding certification by third-party algorithm providers. The analog inputs feature a 95 dB dynamic range stereo ADC fed from a four-stereo input mux. The four stereo analog outputs are each driven by a 95 dB dynamic range DAC. A dedicated headphone channel is included with integrated amplifiers.

The ADAV400 supports multichannel digital inputs and outputs. An integrated SRC on one channel provides the capability to support any input sample rate in the range of 5 kHz to 50 kHz, synchronizing this input to the internal DSP engine.

The ADAV400 is supported by a powerful graphical programming tool that includes blocks such as general filters, EQ filters, dynamics processing, mixers, volume, and third-party algorithms for fast development of custom signal flows.

SPECIFICATIONS

AVDDn[1] = 3.3 V, ODVDD = 3.3 V, DVDD = internal voltage regulator, temperature = 0°C to 70°C, master clock = 12.288 MHz, measurement bandwidth = 20 Hz to 20 kHz, ADC input signal = 1 kHz, DAC output signal = 1 kHz, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE SECTION					
Absolute Voltage (V_{REF})		1.5		V	
V_{REF} Temperature Coefficient		130		ppm/°C	
ANALOG INPUTS (SINGLE ENDED)					
Number of Channels		8			Four stereo input channels
Full-Scale Analog Input		100		µA rms	2 V rms input with 20 kΩ series resistor
DC Offset		±10		mV	Relative to V_{REF}
ADC SECTION					Stereo ADC
Resolution		24		Bits	
Dynamic Range					
A-Weighted	90	95		dB	−60 dB with respect to full-scale analog input
Total Harmonic Distortion + Noise		−90		dB	−3 dB with respect to full-scale analog input
Interchannel Gain Mismatch		0.1		dB	Left and right channel gain mismatch
Crosstalk		−78		dB	Analog channel crosstalk (AINYm[2] to AINYm[2]) One channel = −3 dB, other channel = 0 V
Gain Error		−6		%	
Power Supply Rejection		−83		dB	1 kHz, 300 mV p-p signal at AVDDn[1]
ADC DIGITAL DECIMATOR FILTER CHARACTERISTICS @ 48 kHz[3]					
Pass Band		22.5		kHz	
Pass-Band Ripple		±0.0002		dB	
Transition Band		24		kHz	
Stop Band		26.5		kHz	
Stop-Band Attenuation		100		dB	
Group Delay		1040		µs	
DAC OUTPUTS (SINGLE-ENDED)					DAC amplifier register contents = 0x0010
Number of Channels		8			Four stereo output channels
Resolution		24		Bits	
Full-Scale Analog Output		1		V rms	
Dynamic Range					
A-Weighted	90	95		dB	−60 dB with respect to full-scale code input
Total Harmonic Distortion + Noise[4]		−93		dB	−3 dB with respect to full-scale code input
Crosstalk		−100		dB	Analog channel crosstalk (VOUTm[2] to VOUTm[2]) One channel = −3 dB, other channels = 0 V
Gain Error		5		%	
Interchannel Gain Mismatch		0.1		dB	Left and right channel gain mismatch
DC Offset		1		mV	Relative to V_{REF}
Power Supply Rejection		−87		dB	1 kHz, 300 mV p-p signal at AVDDn[1]
DAC DIGITAL INTERPOLATION FILTER CHARACTERISTICS @ 48 kHz[3]					
Pass Band		21.769		kHz	
Pass-Band Ripple		±0.01		dB	
Transition Band		23.95		kHz	
Stop Band		26.122		kHz	
Stop-Band Attenuation		75		dB	
Group Delay		580		µs	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HEADPHONE OUTPUT (SINGLE ENDED)					Measured at headphone output with 32 Ω load, headphone amplifier register contents = 0x0001
Number of Channels		2			One stereo channel
Resolution		24		Bits	
Full-Scale Analog Output		1		V rms	
Dynamic Range					
A-Weighted		92		dB	−60 dBFS with respect to full-scale code input
Total Harmonic Distortion + Noise		−84		dB	−3 dBFS with respect to full-scale code input
Gain Error		4		%	
Interchannel Gain Mismatch		0.5		dB	
DC Offset		−30		mV	Relative to V_{REF}
Power Supply Rejection		−84		dB	1 kHz, 300 mV p-p signal at AVDDn[1]
PLL SECTION[3]					
Master Clock Input (MCLKI)	64 × f_S		512 × f_S	MHz	
SRC[3]					
Dynamic Range					
A-Weighted		115		dB	−60 dBFS input (worst-case input, f_S = 50 kHz)
Total Harmonic Distortion + Noise		−113		dB	0 dBFS input (worst-case input, f_S = 50 kHz)
Sample Rate	5		50	kHz	
DIGITAL INPUT/OUTPUT					
Input Voltage High (V_{IH})	2.0		ODVDD	V	
Input Voltage Low (V_{IL})			0.8	V	
Input Leakage (I_{IH} @ V_{IH} = ODVDD)			10	µA	
Input Leakage (I_{IL} @ V_{IL} = 0 V)	−60			µA	
Output Voltage High (V_{OH} @ I_{OH} = 0.4 mA)	2.4			V	
Output Voltage Low (V_{OL} @ I_{OL} = −3.2 mA)			0.4	V	
Input Capacitance		10		pF	
SUPPLIES					
Analog Supplies (AVDDn)[1]	3.15	3.30	3.45	V	
Digital Supplies (DVDD)	1.6	1.8	2.0	V	
Interface Supply (ODVDD)	3.15	3.30	3.45	V	
Supply Current, Normal Mode					MCLK = 12.288 MHz, ADCs and DACs active, headphone outputs active and driving a 32 Ω load, Power control register = 0xFFFF
Analog Current (AVDD1)		90	110	mA	
Digital and Interface Current		120	135	mA	
PLL Current		5	6	mA	
Supply Current, Power-Down Mode					$\overline{\text{RESET}}$ low, MCLK = 3.074 MHz, AINx = AGND, DAC and headphone outputs floating
Analog Current		6	8.5	mA	
Digital and Interface Current		1.5	6	mA	
PLL Current		5	50	µA	

[1] The n refers to supply number.
[2] The m refers to channel number, and the Y refers to stereo channel identifier: L for left channel or R for right channel.
[3] Guaranteed by design.
[4] Measured on one DAC with other DACs and ADCs off.

DIGITAL TIMING

Table 2.

Parameter	Min	Max	Unit	Comments
MASTER CLOCK AND RESET				
f_{MCLKI} (MCLKI Frequency)	3.024	24.576	MHz	
t_{MCH} (MCLKI High)	10		ns	
t_{MCL} (MCLKI Low)	10		ns	
t_{RLPW} ($\overline{\text{RESET}}$ Low Pulse Width)	20		ns	
I²C® PORT				
f_{SCL} (SCL Clock Frequency)		400	kHz	
t_{SCLH} (SCL High)	0.6		µs	
t_{SCLL} (SCL Low)	1.3		µs	
Start Condition				
t_{SCS} (Setup Time)	0.6		µs	Relevant for repeated start condition
t_{SCH} (Hold Time)	0.6		µs	The first clock is generated after this period
t_{DS} (Data Setup Time)	100		ns	
t_{SCR} (SCL Rise Time)		300	ns	
t_{SCF} (SCL Fall Time)		300	ns	
t_{SDR} (SDA Rise Time)		300	ns	
t_{SDF} (SDA Fall Time)		300	ns	
Stop Condition				
t_{SCSH} (Setup Time)	0.6		µs	
SERIAL PORTS				
Slave Mode				
t_{SBH} (BCLKx High)	40		ns	
t_{SBL} (BCLKx Low)	40		ns	
f_{SBF} (BCLKx Frequency)	$64 \times f_S$			
t_{SLS} (LRCLKx Setup)	10		ns	To BCLK rising edge
t_{SLH} (LRCLKx Hold)	10		ns	From BCLK rising edge
t_{SDS} (SDINx Setup)	10		ns	To BCLK rising edge
t_{SDH} (SDINx Hold)	10		ns	From BCLK rising edge
t_{SDD} (SDOx Delay)		40	ns	From BCLK falling edge
Master Mode				
t_{MLD} (LRCLKx Delay)		5	ns	From BCLK falling edge
t_{MDD} (SDOx Delay)		40	ns	From BCLK falling edge
t_{MDS} (SDINx Setup)	10		ns	From BCLK rising edge
t_{MDH} (SDINx Hold)	10		ns	From BCLK rising edge

Digital Timing Diagrams

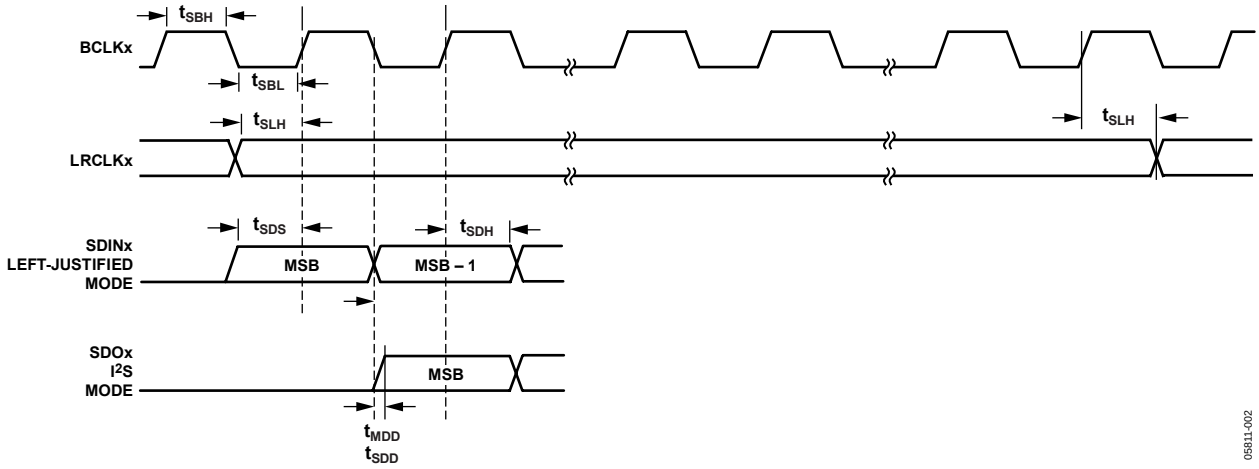

Figure 2. Serial Port Timing

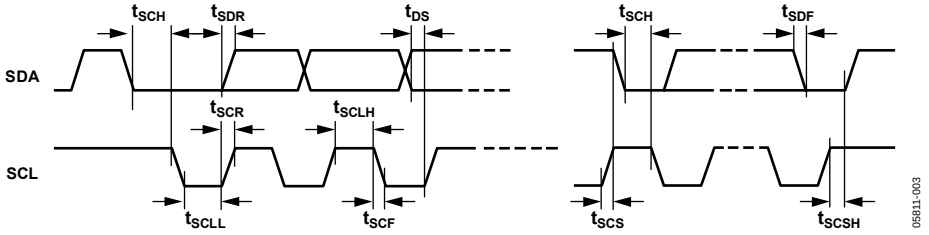

Figure 3. I²C Port Timing

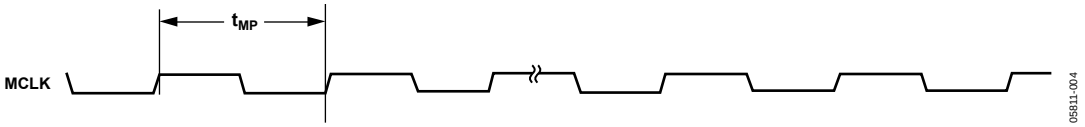

Figure 4. Master Clock Timing

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
DVDD to DGND	0 V to 2.2 V
ODVDD to DGND	0 V to 4.0 V
AVDD to AGND	0 V to 4.0 V
AGND to DGND	−0.3 V to +0.3 V
Digital Inputs	DGND − 0.3 V to ODVDD + 0.3 V
Analog Inputs	AGND − 0.3 V to ADVDD + 0.3 V
Reference Voltage	Indefinite short circuit to ground
Soldering (10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

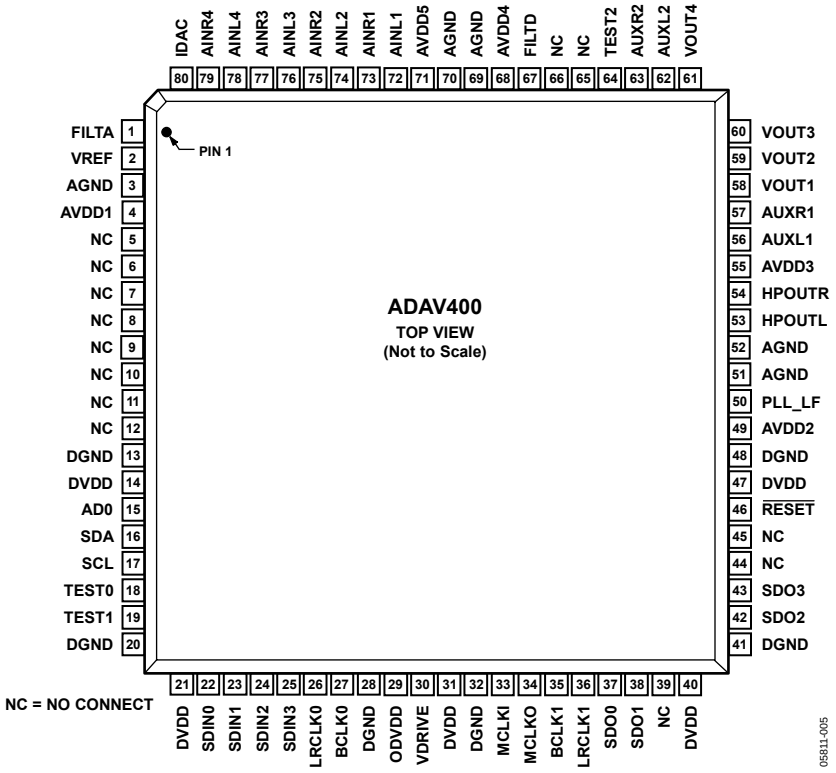

Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	I/O	Description
1	FILTA	O	ADC Filter Decoupling Node for the ADC. Decouple this pin to AGND (Pin 3).
2	VREF		Voltage Reference. This pin is driven by an internal 1.5 V reference voltage. Decouple this pin to AGND (Pin 3).
3	AGND		ADC Ground. Connect this pin to the analog ground plane.
4	AVDD1		Analog Power Supply Pin for the ADC. Connect this pin to 3.3 V and decouple to AGND (Pin 3).
5 to 12, 65, 66	NC		Not Connected Internally.
13, 20, 28, 32, 41, 48	DGND		Digital Ground. Connect this pin to the digital ground plane.
14, 21, 31, 40, 47	DVDD		Digital Power Supply Pins. Connect these pins to 1.8 V, either directly or by using the on-chip regulator. Decouple to DGND.
15	AD0	I	I^2C Address Select. Tie to ODVDD for Address 0x28 (write) and Address 0x29 (read) or to DGND for Address 0x2A (write) and Address 0x2B (read).
16	SDA	I/O	Serial Data Input/Output for the I^2C Control Port.
17	SCL	I	Serial Clock for the I^2C Control Port.
18	TEST0		Test Pin. Connect to ODVDD.
19	TEST1		Test Pin. Connect to ODVDD.
22 to 25	SDIN [0:3]	I	Serial Data Inputs. BCLK1 and LRCLK1 are used as the timing signals for SDIN0 to SDIN3.
26	LRCLK0	I	Left/Right Clock for Sample Rate Converter (SRC). This input frame synchronization signal is associated with SDIN0 to SDIN3 when one of these input channels is redirected to the SRC.
27	BCLK0	I	Bit Clock for Sample Rate Converter (SRC). This input clock is associated with SDIN0 to SDIN3 when one of these input channels is redirected to the SRC.
29	ODVDD		Digital Interface Supply (3.3 V) Pin. Connect this pin to a 3.3 V digital supply. Decouple to DGND.
30	VDRIVE		Drive for External PNP Transistor. This is used with the on-chip 1.8 V regulator circuit.

Pin No.	Mnemonic	I/O	Description
33	MCLKI	I	Master Clock Input. The ADAV400 uses a phase-locked loop (PLL) to generate the appropriate internal clock for the DSP core.
34	MCLKO	O	Audio Clock Output. The MCLKO pin can be programmed to output the internal audio clock.
35	BCLK1	I/O	Bit Clock for Serial Data Input/Output. This clock and the LRCLK1 are used as clock and frame sync signals for the SDINx and SDOx pins. These clocks are inputs to the ADAV400 when the port is configured as a slave, and outputs when the port is configured as a master. On power up, these pins are set to slave mode to avoid conflicts with external master mode devices.
36	LRCLK1	I/O	Left/Right Clock for Serial Data Input/Output. This clock and the BCLK1 are used as clock and frame sync signals for the SDINx and SDOx pins.
37, 38, 42, 43	SDO [0:3]	0	Serial Data Outputs.
39, 44, 45	NC		These pins should be left unconnected.
46	$\overline{\text{RESET}}$	I	Active Low Reset Signal. After $\overline{\text{RESET}}$ the ADAV400 is powered down.
49	AVDD2		Analog Power Supply Pin for the PLL. Connect this pin to 3.3 V and decouple to AGND (Pin 51).
50	PLL_LF		PLL Loop Filter. External components are required to allow the PLL to function correctly. See the PLL Block section for details of these components.
51	AGND		PLL Ground. Connect this pin to the analog ground plane.
52	AGND		Headphone Driver Ground. Connect this pin to the analog ground plane.
53	HPOUTL	O	Left Headphone Output. Analog output from the headphone amplifiers.
54	HPOUTR	O	Right Headphone Output. Analog output from the headphone amplifiers.
55	AVDD3		Analog Power Supply Pin for the Headphone Amplifier. Connect this pin to 3.3 V and decouple to AGND (Pin 52).
56	AUXL1	O	Auxiliary Analog Output Left 1.
57	AUXR1	O	Auxiliary Analog Output Right 1.
58 to 61	VOUT [1:4]	O	Main Analog Output 1 to Output 4.
62	AUXL2	O	Auxiliary Analog Output Left 2.
63	AUXR2	O	Auxiliary Analog Output Right 2.
64	TEST2		Test Pin. This pin should be left unconnected.
67	FILTD		DAC Filter Decoupling Node. Decouple this pin to AGND (Pin 69).
68	AVDD4		Analog Power Supply Pin for the DAC. Connect this pin to 3.3 V and decouple to AGND (Pin 69).
69, 70	AGND		DAC Ground. Connect this pin to the analog ground plane.
71	AVDD5		Analog Power Supply Pin for the DAC. Connect this pin to 3.3 V and decouple to AGND (Pin 70).
72, 74, 76, 78	AINL [1:4]	I	Left Analog Input 1 to Input 4. The analog inputs are current inputs typically driven via a 20 kΩ resistor for 2 V rms input, as shown in Figure 17.
73, 75, 77, 79	AINR [1:4]	I	Right Analog Input 1 to Input 4. The analog inputs are current inputs typically driven via a 20 kΩ resistor for 2 V rms input, as shown in Figure 17.
80	IDAC		DAC External Bias Resistor. This is an external bias pin for the DAC circuitry. Connect a 20 kΩ resistor between this pin and AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

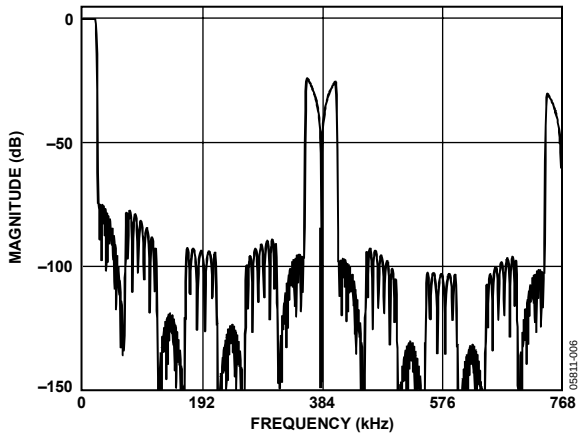

Figure 6. DAC Composite Filter Response (48 kHz)

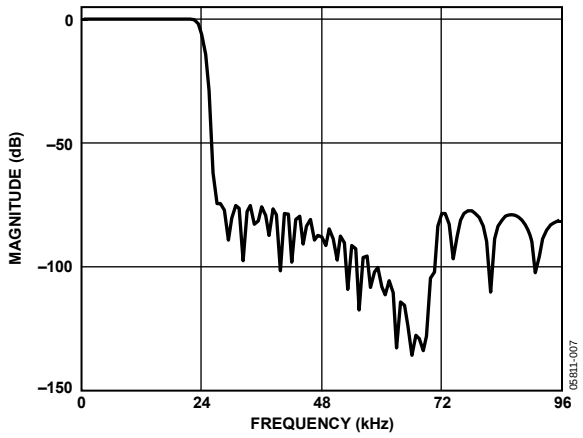

Figure 7. DAC Pass-Band Filter Response (48 kHz)

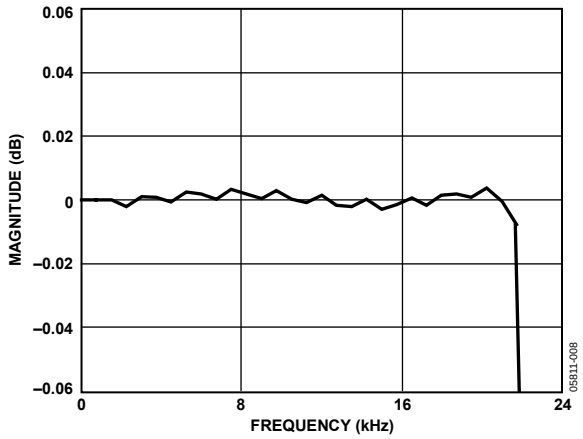

Figure 8. DAC Pass-Band Ripple (48 kHz)

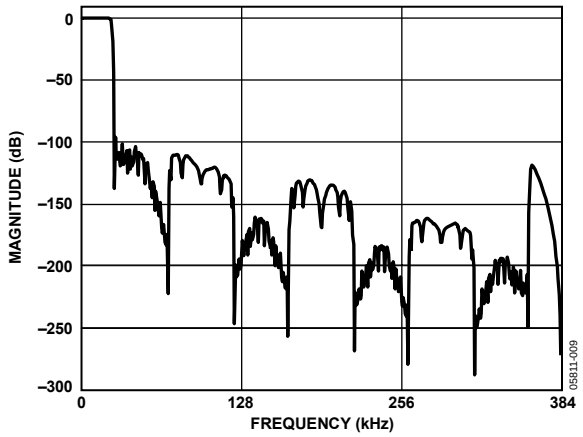

Figure 9. ADC Composite Filter Response (48 kHz)

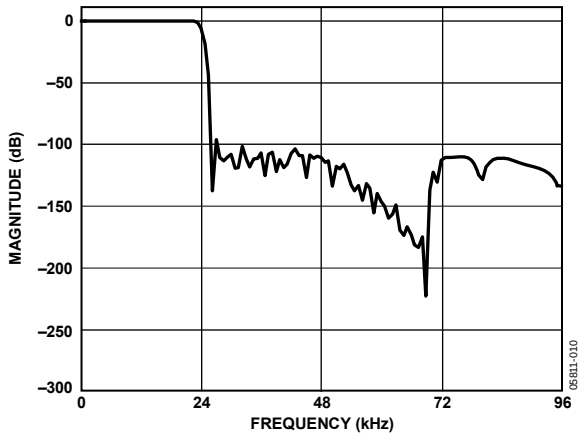

Figure 10. ADC Pass-Band Filter Response (48 kHz)

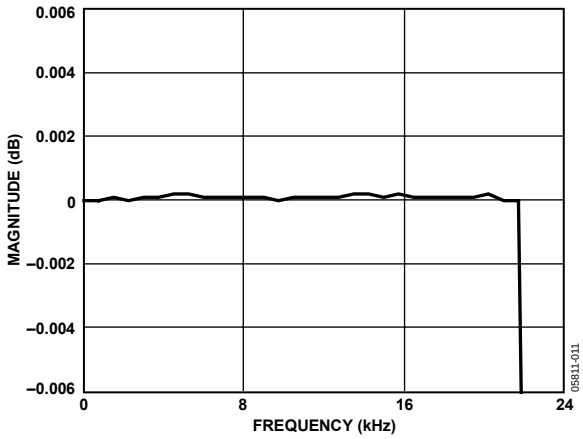

Figure 11. ADC Pass-Band Ripple (48 kHz)

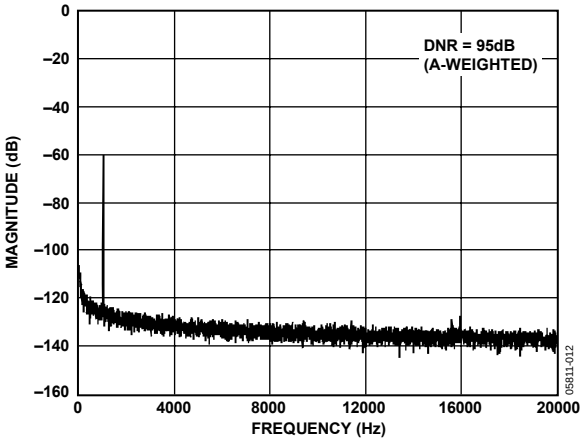

Figure 12. DAC Dynamic Range

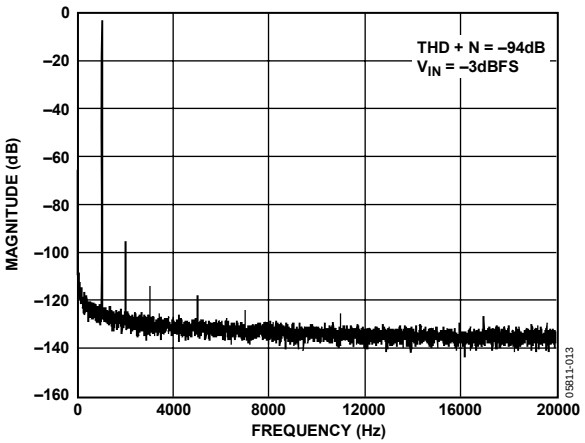

Figure 13. DAC Total Harmonic Distortion + Noise

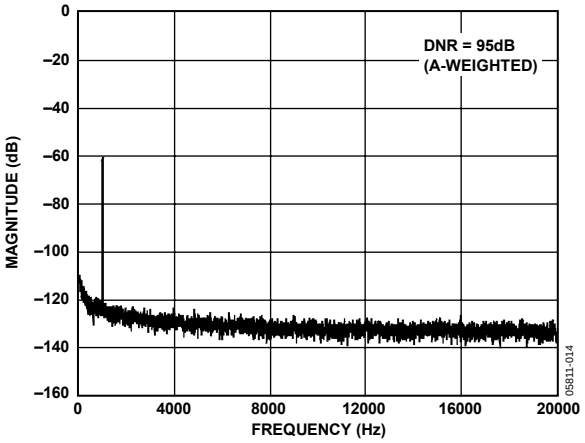

Figure 14. ADC Dynamic Range

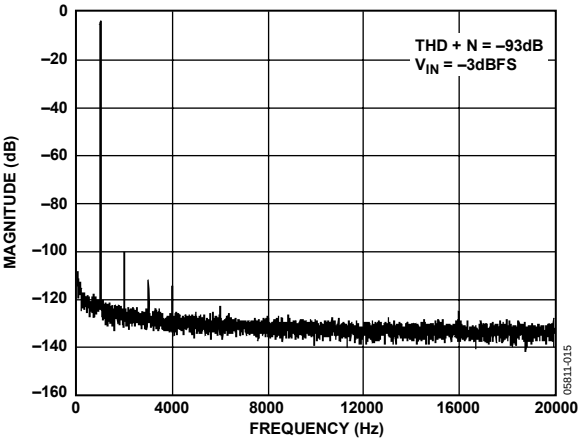

Figure 15. ADC Total Harmonic Distortion + Noise

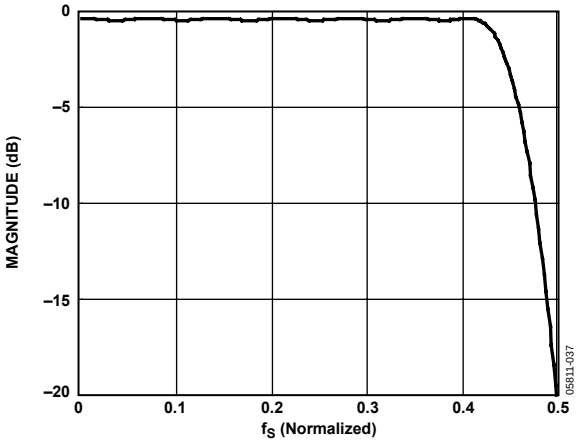

Figure 16. Sample Rate Converter Transfer Function

THEORY OF OPERATION

The ADAV400 is an enhanced audio processor containing an Analog Devices SigmaDSP digital processing core. The core can accept up to four digital stereo channels, typically at 48 kHz, or three channels, typically at 48 kHz, and one channel at any sample rate between 5 kHz and 50 kHz. In addition, up to four stereo analog inputs can be used as the source for the DSP core using the stereo ADC and a four-stereo input mux.

Outputs from the DSP core are available as four stereo digital outputs and four stereo analog outputs.

The core of the ADAV400 is a 28-bit DSP (56-bit with double precision) optimized for audio processing. Signal processing parameters are stored in a 1024-location parameter RAM. The program RAM can be loaded with a custom program after power-up. New values are written to the program and parameter RAM using the I²C control port. The values stored in the parameter RAM control individual signal processing blocks, such as IIR equalization filters, dynamics processors, audio delays, and mixer levels. A safe load feature allows transparent updating of these parameters, eliminating the risk of unwanted pops or clicks in the outputs.

The ADAV400 has a sophisticated control port that supports complete read/write capability of all memory locations except the target/slew RAM and data RAM, which are only accessible by the DSP core.

The ADAV400 has a very flexible serial data input and output port that allows for glueless interconnection to a variety of ADCs, DACs, general-purpose DSPs, S/PDIF receivers, and sample rate converters. The digital inputs and outputs of the ADAV400 can be configured in I²S, left-justified, right-justified, or TDM serial port–compatible mode. They can support 16, 20, or 24 bits in all modes. The ADAV400 accepts serial audio data in MSB-first and twos complement formats.

The digital core of the ADAV400 operates at 1.8 V, and the other circuit blocks operate from a 3.3 V power supply. An on-board regulator allows a single 3.3 V supply for both digital supplies using the configuration shown in Figure 19.

The ADAV400 is fabricated on a single monolithic integrated circuit and is housed in an 80-lead LQFP for operation over the 0°C to 70°C consumer temperature range.

ANALOG INPUTS

The ADAV400 has four stereo analog inputs. An input multiplexer is included that enables any of these four stereo analog inputs to be connected to the ADC. The analog inputs are current inputs; see Figure 17 for the suggested input configuration when the required input level is 2 V rms.

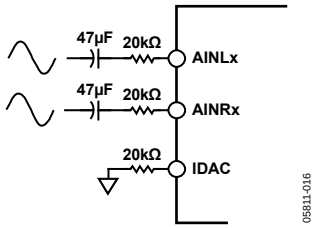

Figure 17. Analog Input Configuration

SAMPLE RATE CONVERTER BLOCK

The ADAV400 contains a stereo SRC that accepts input sample rates in the range of 5 kHz to 50 kHz. Any one of the digital inputs can be selected as the source for the SRC.

Note that the SRC has a filter cutoff frequency of 20 kHz for a 48 kHz sample rate. If a different input sample rate is used, the cutoff frequency scales accordingly.

PLL BLOCK

The ADAV400 contains a phase-locked loop (PLL) that generates all of the internal clocks required by the ADAV400. The master clock frequency can be 64 × f_S, 128 × f_S, 256 × f_S, or 512 × f_S.

The PLL requires some external components to operate correctly, as shown in Figure 18. These components form a loop filter that integrates pulses from a charge pump and produces a voltage to tune the VCO. Internally, the PLL can generate clocks of up to 200 MHz, so it is recommended that a suitable capacitor be selected.

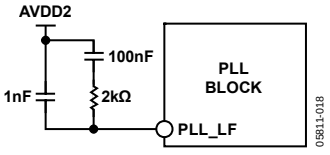

Figure 18. PLL Loop Filter Components

A 3.3 V analog supply connected to AVDD2 is required to operate the PLL. Where the supply for AVDD1 is also used for the PLL, additional filtering is recommended to prevent digital noise created by the PLL block being coupled to the analog circuitry powered by the AVDD1 supply.

ANALOG OUTPUTS

The ADAV400 contains four stereo analog outputs typically at 1 V rms. One stereo pair of DACs is connected to integrated headphone amplifiers HPOUTL and HPOUTR, but is also available on the AUXL1 and AUXR1 pins.

Note that the outputs of all the DACs are inverted with the exception of the headphone channel. If required, this can be changed using the invert library block of the DSP.

HEADPHONE AMPLIFIER

The ADAV400 has an integrated stereo headphone amplifier capable of driving 32 mW into a 32 Ω load.

VOLTAGE REGULATOR

The ADAV400 includes an on-chip voltage regulator that enables the chip to be used in systems where a 1.8 V supply is not available. The only external components needed are a PNP transistor (such as FZT953), a single capacitor, and a single resistor. The recommended design for the voltage regulator is shown in Figure 19.

As shown in this figure, VDD is the main system voltage (3.3 V). A voltage of 1.8 V is generated at the transistor's collector and is connected to the DVDD pins. VDRIVE is an output from the internal regulator circuit on the ADAV400 and is connected to the base of the PNP transistor.

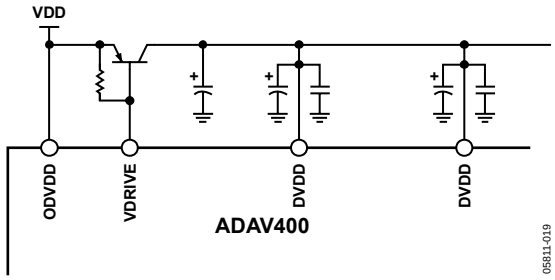

Figure 19. Voltage Regulator Design

There are two specifications to take into consideration when choosing the regulator's transistor. First, h_{FE} should be at least 100. Second, the collector power dissipation, P_C, must be greater than

$$P_C = (3.3\ \text{V} - 1.8\ \text{V}) \times 135\ \text{mA} = 202.5\ \text{mW}$$

CONTROL PORT

The ADAV400 control port has full read and write capability to all registers and RAMs with the exception of the data RAM, which is only accessible by the DSP core. Single or burst mode reads and writes are supported. A typical word consists of the chip address, the register or RAM subaddress, and the data to be written. The number of bytes per data-word depends on the address of the location being written to or read from.

The first byte of a control word (Byte 0) contains the 7-bit chip address plus the R/$\overline{W}$ bit. The next two bytes (Byte 1 and Byte 2) together form the subaddress of the memory or register location within the ADAV400. All subsequent bytes contain data that can be writes to the control register or updates to the program and parameter memories. Table 16 to Table 25 provide more details on the I²C write and read formats.

The ADAV400 has several mechanisms for updating signal processing parameters in real time without causing pops or clicks. In cases where large blocks of data need to be transferred, it is recommended to mute the output of the DSP core by setting Bit 9 of the audio core control register to 0, and then load the new data and set Bit 9 back to 1. This is typically done during the booting sequence at startup or when loading a new program into RAM.

In cases where only a few parameters need to be changed—for example, updating a biquad—the new parameters can be loaded without halting the program. To avoid unwanted pops or clicks in the output during the loading sequence, the DSP core uses an internal safe load mechanism that buffers the data and only updates the parameter memory at the end of the sample period and before the start of the next sample period.

I²C PORT

The ADAV400 supports a 2-wire serial (I²C-compatible) microprocessor bus driving multiple peripherals. Two pins, serial data (SDA) and serial clock (SCL), carry information between the ADAV400 and the system I²C master controller. The ADAV400 is always a slave on the I²C bus, which means that it never initiates a data transfer. Each slave device is recognized by a unique address.

The ADAV400 has four possible slave addresses, two for writing operations and two for reading operations. These are unique addresses for the device and are illustrated in Table 5. The LSB of the byte sets either a read or a write operation; Logic Level 1 corresponds to a read operation, and Logic Level 0 corresponds to a write operation. The seventh bit of the address is set by tying the AD0 pin of the ADAV400 to Logic Level 0 or Logic Level 1.

Table 5. I²C Addresses

AD0	R/$\overline{W}$	Slave Address
0	0	0x28
0	1	0x29
1	0	0x2A
1	1	0x2B

Addressing

Initially, all devices on the I²C bus are in an idle state, wherein the devices monitor the SDA and SCL lines for a start condition and the proper address. The I²C master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream follows. All devices on the bus respond to the start condition and read the next byte (7-bit address + R/$\overline{W}$ bit) MSB first. The device that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This ninth bit is known as an acknowledge bit. All other devices on the bus revert to an idle condition. The R/$\overline{W}$ bit determines the direction of the data. A Logic Level 0 on the LSB of the first byte means the master writes information to the peripheral. A Logic Level 1 on the LSB of the first byte means the master reads information from the peripheral. A data transfer takes place until a stop condition is encountered. A stop condition occurs when SDA transitions from low to high while SCL is held high. Figure 20 shows the timing of an I²C write.

Burst mode addressing, where the subaddresses are automatically incremented at word boundaries, can be used for writing large amounts of data to contiguous memory locations. This increment happens automatically if a stop condition is not encountered after a single word write. A data transfer is always terminated by a stop condition.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, it causes an immediate jump to the idle condition. During a given SCL high period, the user should only issue one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADAV400 does not issue an acknowledge and reverts to an idle state. If the user exceeds the highest subaddress while in auto-increment mode, one of two actions is taken. In read mode, the ADAV400 outputs the highest subaddress register contents until the master device issues a no acknowledge, indicating the end of a read. A no acknowledge condition is where the SDA line is not pulled low on the ninth clock pulse on SCL. If the highest subaddress location is reached while in write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the ADAV400, and the part returns to the idle condition.

I²C Read and Write Operations

Table 6 shows the timing of a single word write operation. Every ninth clock, the ADAV400 issues an acknowledge by pulling SDA low.

Table 7 shows the timing of a burst mode write sequence. This table shows an example where the target destination registers are two bytes. The ADAV400 auto-increments its subaddress register counter every two bytes until a stop condition occurs.

The timing of a single word read operation is shown in Table 8. Note that the first R/$\overline{W}$ bit is still a 0, indicating a write operation. This is because the subaddress must be written to set up the internal address. After the ADAV400 acknowledges the receipt of the subaddress, the master must issue a repeated start command followed by the chip address byte with the R/$\overline{W}$ set to 1 (read). The ADAV400 responds with the read result on SDA. The master then responds every ninth clock with an acknowledge pulse to the ADAV400.

Table 9 shows the timing of a burst mode read sequence. This table shows an example where the target read registers are two bytes. The ADAV400 increments its subaddress register every two bytes because the requested subaddress corresponds to a register or memory area with word lengths of two bytes. Other address ranges may have a variety of word lengths ranging from one to six bytes; the ADAV400 always decodes the subaddress and sets the auto-increment circuit so that the address increments after the appropriate number of bytes.

Key for Table 6 to Table 9

S = start bit
P = stop bit
AM = acknowledge by master
AS = acknowledge by slave

Table 6. Single Word I²C Write

S	Chip address, R/$\overline{W}$ = 0	AS	Subaddress high	AS	Subaddress low	AS	Data Byte 1	AS	Data Byte 2	…	AS	Data Byte N	P

Table 7. Burst Mode I²C Write

S	Chip address, R/$\overline{W}$ = 0	AS	Subaddress high	AS	Subaddress low	AS	Data-Word 1, Byte 1	AS	Data-Word 1, Byte 2	AS	Data-Word 2, Byte 1	AS	Data-Word 2, Byte 2	AS	…	P

Table 8. Single Word I²C Read

S	Chip address, R/$\overline{W}$ = 0	AS	Subaddress high	AS	Subaddress low	AS	S	Chip address, R/$\overline{W}$ = 1	AS	Data Byte 1	AM	Data Byte 2	…	AM	Data Byte N	P

Table 9. Burst Mode I²C Read

S	Chip address, R/$\overline{W}$ = 0	AS	Subaddress high	AS	Subaddress low	AS	S	Chip address, R/$\overline{W}$ = 1	AS	Data-Word 1 Byte 1	AM	Data-Word 1 Byte 2	AM	…	P

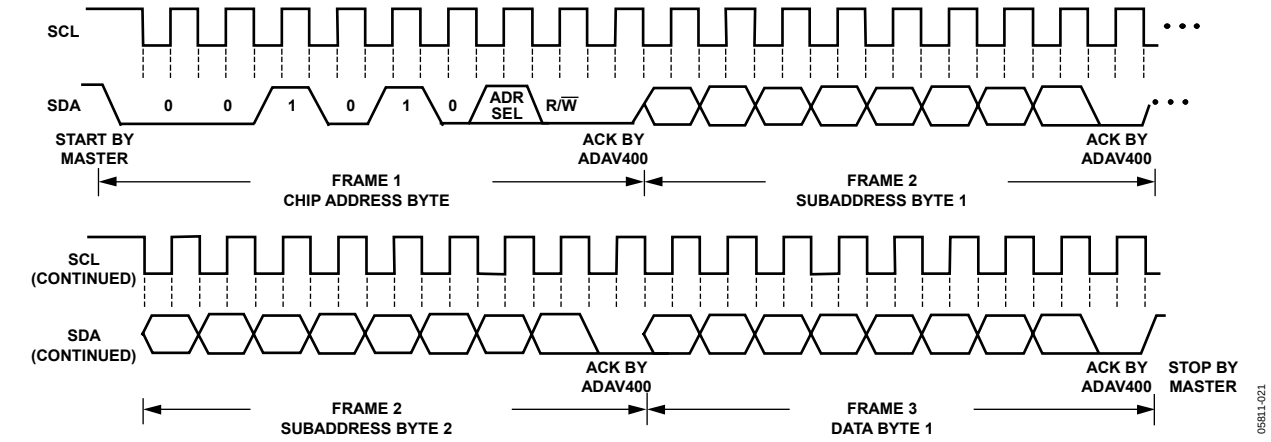

Figure 20. I²C Write Format

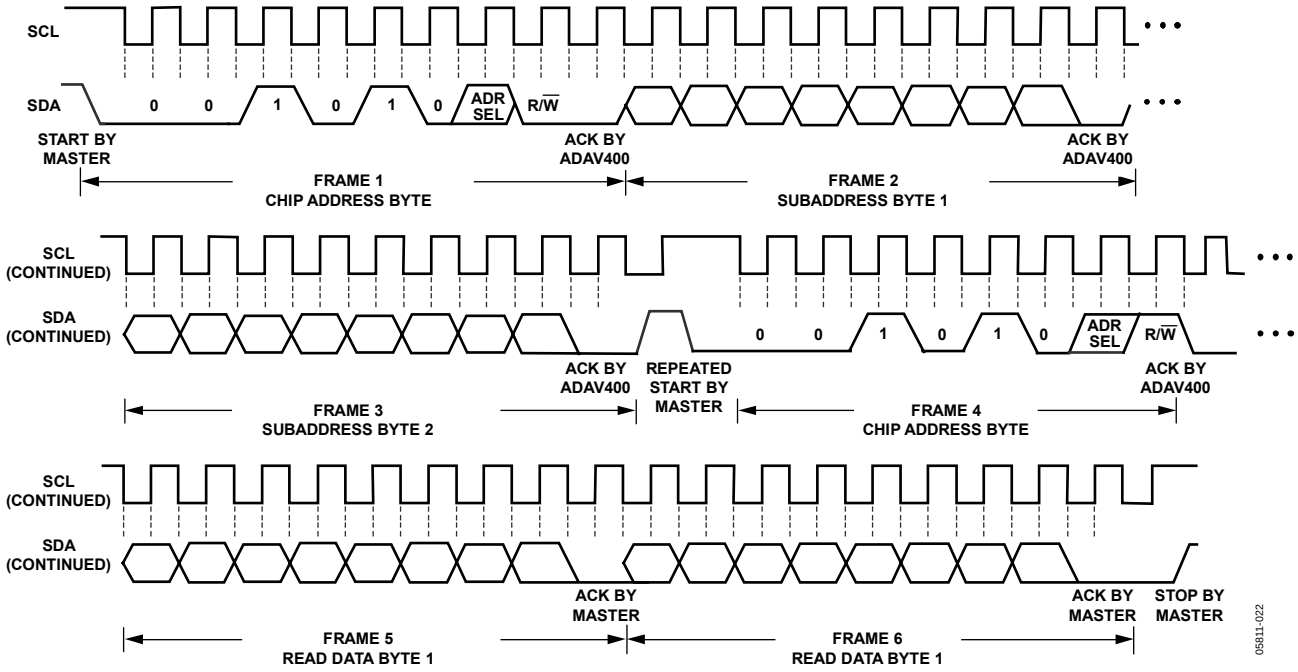

Figure 21. I²C Read Format

SIGNAL PROCESSING

The ADAV400 is designed to provide all the signal processing functions commonly used in stereo or multichannel playback systems. The signal processing flow is created using a graphical development tool supplied by Analog Devices, which allows fast development of even complex audio flows and real-time control of all signal processing functions.

The input and output word lengths are 24 bits. Four extra headroom bits are used in the processor to allow internal gains of up to 24 dB without clipping.

The signal processing blocks can be arranged in a custom program that is loaded to the RAM of the ADAV400. The available signal processing blocks are outlined in the Numeric Formats and Programming sections.

NUMERIC FORMATS

It is common in DSP systems to use a standardized method of specifying numeric formats. Fractional number systems are specified by an A.B format, where A is the number of bits to the left of the decimal point and B is the number of bits to the right of the decimal point.

The ADAV400 uses the same numeric format for both the coefficient values (stored in the parameter RAM) and the signal data values.

Numeric Format: 5.23

Range
−16.0 to (+16.0 − 1 LSB)

Examples
1000 0000 0000 0000 0000 0000 0000 = −16.0
1110 0000 0000 0000 0000 0000 0000 = −4.0
1111 1000 0000 0000 0000 0000 0000 = −1.0
1111 1110 0000 0000 0000 0000 0000 = −0.25
1111 1111 1111 1111 1111 1111 1111 = (1 LSB below 0.0)
0000 0000 0000 0000 0000 0000 0000 = 0.0
0000 0010 0000 0000 0000 0000 0000 = +0.25
0000 1000 0000 0000 0000 0000 0000 = +1.0
0010 0000 0000 0000 0000 0000 0000 = +4.0
0111 1111 1111 1111 1111 1111 1111 = (+16.0 − 1 LSB)

The serial port accepts up to 24 bits on the input and is sign-extended to the full 28 bits of the core. This allows internal gains of up to 24 dB without encountering internal clipping.

A digital clipper circuit is used between the output of the DSP core and the serial output ports (see Figure 22). This clips the top four bits of the signal to produce a 24-bit output with a range of +1.0 (−1 LSB) to −1.0.

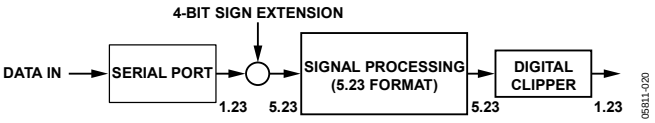

Figure 22. Numeric Precision and Clipping Structure

PROGRAMMING

On power-up, the default program of the ADAV400 passes the unprocessed input signals to the outputs, but the outputs are muted by default. There are 2560 instruction cycles per audio sample. This DSP runs in a stream-oriented manner, meaning all 2560 instructions are executed each sample period. The ADAV400 can also be set up to accept double- or quad-speed inputs by reducing the number of instructions per sample. This is set in the audio core control register.

The part is easily programmed using graphical tools provided by Analog Devices. No knowledge of DSP assembly code is required to program the ADAV400. Simply connect graphical blocks, such as biquad filters, dynamics processors, mixers, and delays, in a signal flow schematic. The schematic is then compiled, and the program and parameter files are loaded into the program RAM of the ADAV400 through the control port. Signal processing blocks available in the provided libraries include

- Single- and double-precision biquad filters
- Monochannel and multichannel dynamics processors
- Mixers and splitters
- Tone and noise generators
- First-order filters
- Fixed and variable gain
- RMS look-up tables
- Loudness
- Delay
- Stereo enhancement (Phat Stereo™)
- Dynamic bass boost
- Interpolators and decimators

Additional blocks are always in development. Analog Devices also provides proprietary and third-party algorithms for applications such as matrix decoding, bass enhancement, and surround virtualizers. Contact Analog Devices for information about licensing these algorithms.

RAMS AND REGISTERS

Table 10. Control Port Addresses

I²C Subaddress	Register Name	Read/Write Word Length
0 to 1023 (0x0000 to 0x03FF)	Parameter RAM	Write: 4 bytes; read: 4 bytes
1024 to 3584 (0x0400 to 0x0E00)	Program RAM	Write: 6 bytes; read: 6 bytes
4096 to 4159 (0x1000 to 0x103F)	Target/slew RAM	Write: 5 bytes; read: N/A
4160 to 4164 (0x1040 to 0x1044)	Parameter RAM Data Safe Load Register [0:4]	Write: 5 bytes; read: N/A
4165 to 4169 (0x1045 to 0x1049)	Parameter RAM Indirect Address Safe Load Register [0:4]	Write: 2 bytes; read: N/A
4170 to 4175 (0x104A to 0x104F)	Data Capture Register [0:5] (control port readback)	Write: 2 bytes; read: 3 bytes
4176 to 4177 (0x1050 to 0x1051)	Data capture registers (digital output)	Write: 2 bytes; read: N/A
4178 (0x1052)	Audio core control register	Write: 2 bytes; read: 2 bytes
4179 (0x1053)	RAM modulo control register	Write: 1 byte; read: 1 byte
4180 (0x1054)	Serial output control register	Write: 2 bytes; read: 2 bytes
4181 (0x1055)	Serial input control register	Write: 1 byte; read: 1 byte
4182 (0x1056)	SRC serial port control register	Write: 1 byte; read: 1 byte
4183 (0x1057)	ADC input mux control register	Write: 2 bytes; read: 2 bytes
4184 (0x1058)	Power control register	Write: 2 bytes; read: 2 bytes
4185 (0x1059)	User Control 1 register	Write: 2 bytes; read: 2 bytes
4186 (0x105A)	User Control 2 register	Write: 2 bytes; read: 2 bytes
4365 (0x110D)	DAC amplifier register	Write: 2 bytes; read: 2 bytes

Table 11. RAM Read/Write Modes

Memory	Size	Subaddress Range	Read	Write	Burst Mode Available	Write Modes
Parameter RAM	1024 × 28	0 to 1023 (0x0000 to 0x03FF)	Yes	Yes	Yes	Direct write,[1] safe load write
Program RAM	2560 × 42	1024 to 3584 (0x0400 to 0x0E00)	Yes	Yes	Yes	Direct write[1]
Target/Slew RAM	64 × 34	4096 to 4159 (0x1000 to 0x1044)	No	Yes	No	Safe load write

[1] To avoid clicks or pops, mute the DSP core first.

CONTROL PORT ADDRESSING

Table 10 shows the addressing of the RAM and register spaces on the ADAV400. The address space encompasses a set of registers and three RAMs: parameter, program, and target/slew. Table 11 lists the sizes and available writing modes of the parameter, program, and target/slew RAMs.

PARAMETER RAM CONTENTS

The parameter RAM is 28 bits wide and occupies Address 0 to Address 1023. The parameter RAM is initialized to all 0s on power-up. The data format of the parameter RAM is twos complement 5.23. This means that the coefficients can range from +16.0 (−1 LSB) to −16.0, with 1.0 represented by the binary word 0000 1000 0000 0000 0000 0000 0000.

Options for Parameter Updates

The parameter RAM can be written to and read from using one of the two following methods:

- Direct Read/Write.
  This method allows direct access to the program and parameter RAMs. It is normally used during a complete new load of the RAMs using burst mode addressing. To avoid clicks or pops in the outputs, it is recommended to set the clear registers bit in the audio core control register to 0.

- Safe Load Write.
  Up to five safe load registers can be loaded with parameter RAM address data. The data is transferred to the requested address when the RAM is idle. It is recommended to use this method for dynamic updates during run time. For example, a complete update of one biquad section can occur in one audio frame. This method is not available for writing to the program RAM or control registers. The following sections discuss these two options in more detail.

RECOMMENDED PROGRAM/PARAMETER LOADING PROCEDURES

When writing large amounts of data to the program or parameter RAM in direct write mode, disable the processor core to prevent pops or clicks in the audio output. The ADAV400 contains several mechanisms for disabling the core.

If the loaded program does not use the target/slew RAM as the main system volume control (for example, the default power-up program),

1. Assert Bit 9 (low to assert—default setting) and Bit 6 (high to assert) of the audio core control register. This clears the accumulators, the serial output registers, and the serial input registers.
2. Fill the program RAM using burst mode writes.
3. Fill the parameter RAM using burst mode writes.
4. Assert Bit 7 of the audio core control register to initiate a data memory clear sequence. Wait at least 100 µs for this sequence to complete. This bit is automatically cleared after the operation is complete.
5. Deassert Bit 9 and Bit 6 of the audio core control register to allow the core to begin normal operation

If the loaded program does use the target/slew RAM as the main system volume control,

1. Assert Bit 12 of the audio core control register. This begins a volume ramp-down, with a time constant determined by the upper bits of the target RAM. Wait for this ramp-down to complete (the user can poll Bit 13 of the audio core control register, or simply wait for a given amount of time).
2. Assert Bit 9 (low to assert) and Bit 6 (high to assert) of the audio core control register. This clears the accumulators, the serial output registers, and the serial input registers.
3. Fill the program RAM using burst mode writes.
4. Fill the parameter RAM using burst mode writes.
5. Assert Bit 7 of the audio core control register to initiate a data memory clear sequence. Wait at least 100 µs for this sequence to complete. This bit is automatically cleared after the operation is complete.
6. Deassert Bit 9 and Bit 6 of the audio core control register.
7. If the newly loaded program also uses the target/slew RAM, deassert Bit 12 of the audio core control register to begin a volume ramp-up procedure.

TARGET/SLEW RAM

The target/slew RAM is a bank of 64 RAM locations, each of which can be set to autoramp from one value to a desired final value in one of four modes.

When a program is loaded into the program RAM using one or more locations in the slew RAM to access internal coefficient data, the target/slew RAM is used by the DSP. Typically, these coefficients are used for volume controls or smooth cross-fading effects, but they can also be used to update any value in the parameter RAM. Each of the 64 locations in the slew RAM is linked to a corresponding location in the target RAM. When a new value is written to the target RAM using the control port, the corresponding slew RAM location begins to ramp toward the target. The value is updated once per audio frame (LRCLK period).

The target RAM is 34 bits wide. The lower 28 bits contain the target data in 5.23 format for the linear and exponential (constant dB and RC) ramp types. For constant time ramping, the lower 28 bits contain 16 bits in 2.14 format and 12 bits to set the current step. The upper six bits are used to determine the type and speed of the ramp envelope in all modes. The format of the data write for linear and exponential formats is shown in Table 12. Table 13 shows the data write format for the constant time ramping.

In normal operation, write data to the target/slew RAM using the safe load registers as described in the Safe Load Registers section. A mute slew RAM bit is included in the audio core control register to simultaneously set all the slew RAM target values to 0. This is useful for implementing a global multichannel mute. When this bit is deasserted, all slew RAM values return to their original premuted states.

Table 12. Linear, Constant dB, and RC Ramp Data Write

Byte 0	Byte 1	Bytes [2:4]
000000, curve_type [1:0]	time_const [3:0], data [27:24]	data [23:0]

Table 13. Constant Time Ramp Data Write

Byte 0	Byte 1	Bytes [2:4]
000000, curve_type [1:0]	update_step [0], #_of_steps [2:0], data [15:12]	data [11:0], reserved [11:0]

There are four types of ramping curves:

- Linear.
  The value slews to the target value using a fixed step size.
- Constant dB.
  The value slews to the target value using the current value to calculate the step size. The resulting curve has a constant rise and decay when measured in decibels.
- RC.
  The value slews to the target value using the difference between the target and current values to calculate the step size, resulting in a simple RC response.
- Constant Time.
  The value slews to the target value in a fixed number of steps in a linear fashion. The control port mute has no effect on this type of ramping curve.

Table 14. Target/Slew RAM Ramp Type Settings

Settings	Ramp Type
00	Linear
01	Constant dB
10	RC
11	Constant time

The following sections detail how the control port writes to the target/slew RAM to control the time constant and ramp type parameters.

Ramp Types [1:3]—Linear, Constant dB, RC (34-Bit Write)

The target word for the first three ramp types is broken into three parts. The 34-bit command is written with six leading 0s to extend the data write to five bytes. The parts of the target RAM write are

- Ramp type (two bits).
- Time constant (four bits).
- 0000 = fastest
  1111 = slowest
- Data (28 bits): 5.23 format.

Ramp Type 4—Constant Time (34-Bit Write)

The target word for the constant time ramp type is written in five parts, with the 34-bit command written with six leading 0s to extend the data write to five bytes. The parts of the constant time target RAM write are

- Ramp type (two bits).
- Update step (one bit). Set to 1 when a new target is loaded to trigger a step value update. The value is automatically reset after the step value is updated.
- Number of steps (three bits). The number of steps needed to slew to the target value is set by these three bits, with the number of steps equal to $2^{3\text{-bit setting} + 6}$.
  000 = 64
  001 = 128
  010 = 256
  011 = 512
  100 = 1024
  101 = 2048
  110 = 4096
  111 = 8196
- Data (16 bits): 2.14 format.
- Reserved (12 bits). When writing to the RAM, set all of these bits to 0.

Target/Slew RAM Initialization

On reset, the target/slew RAM initializes to preset values. The target RAM initializes to a linear ramp type with a time constant of 5 and the data set to 1.0. The slew RAM initializes to a value of 1.0. These defaults result in a full-scale (1.0 to 0.0) ramp time of 21.3 ms.

Linear Update

A linear update is the addition or subtraction of a constant value, referred to as a step. The equation to describe this step size is

$$Step = \frac{2^{13}}{\frac{10^{2\times(t_{CONST}-5)}}{20}}$$

The result of the equation is normalized to a 5.23 data format. This produces a time constant range from 6.75 ms to 213.4 ms (–60 dB relative to 0 dB full scale). An example of this kind of update is shown in Figure 23 and Figure 24. All slew RAM figure examples, except the half-scale constant time ramp plot (Figure 29), show an increasing or decreasing ramp between –80 dB and 0 dB (full scale). All figures except the constant time plots (Figure 28 and Figure 29) use a time constant of 0x7 (0x0 being the fastest, and 0xF being the slowest).

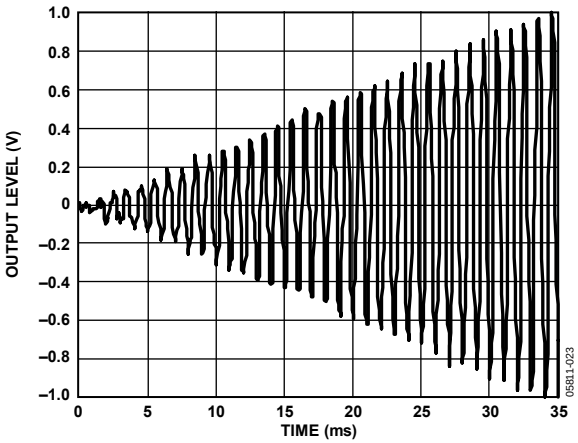

Figure 23. Slew RAM—Linear Update Increasing Ramp

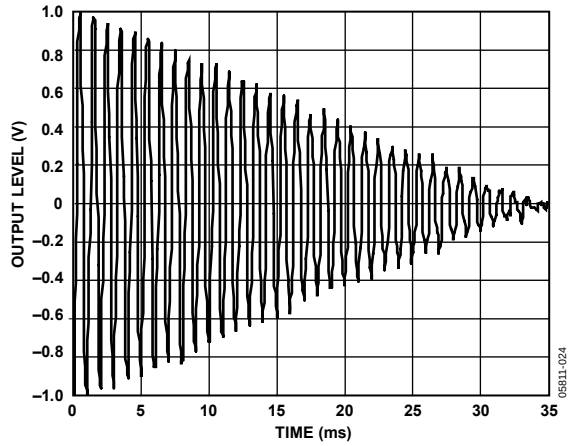

Figure 24. Slew RAM—Linear Update Decreasing Ramp

Constant dB and RC Updates (Exponential)

An exponential update is accomplished by shifts and additions with a range from 6.1 ms to 1.27 sec (−60 dB relative to 0 dB full scale). When the ramp type is set to 01 (constant dB), each step size is set to the current value in the slew data. When the ramp type bits are set to 10 (RC), the step size is equal to the difference between the values in the target RAM and the slew RAM (see Figure 25, Figure 26, and Figure 27).

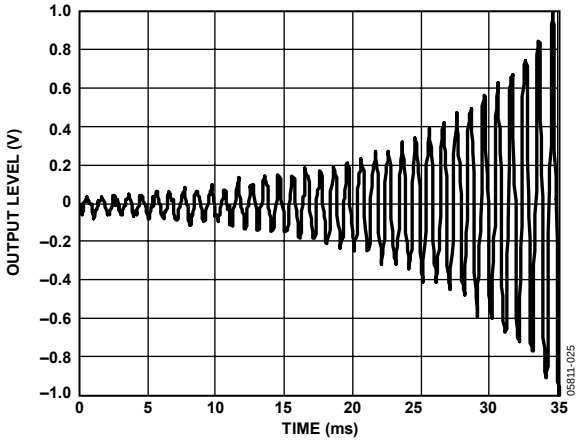

Figure 25. Slew RAM—Constant dB Update Increasing Ramp

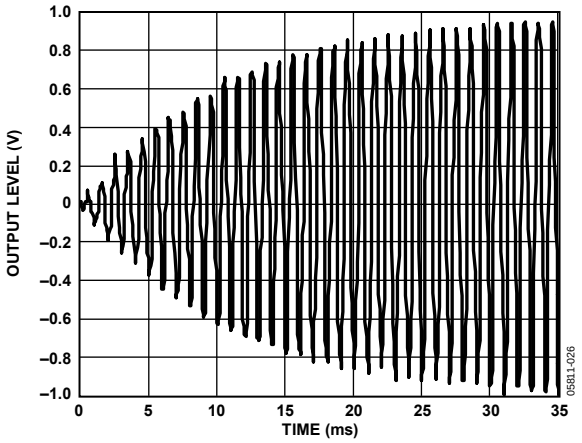

Figure 26. Slew RAM—RC Update Increasing Ramp

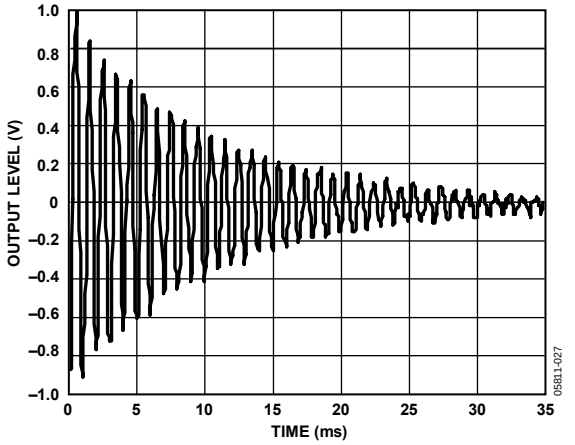

Figure 27. Slew RAM—Constant dB and RC Updates Decreasing Ramp, Full Scale

Constant Time Update

A constant time update is calculated by adding a step value that is determined after each target is loaded. The equation for this step size is

$$Step = (Target\ Data - Slew\ Data)/(Number\ of\ Steps)$$

Figure 28 shows a plot of the target/slew RAM operating in constant time mode. For this example, 128 steps are used to reach the target value. This type of ramping takes a fixed amount of time for a given number of steps, regardless of the difference in the initial state and the target value. Figure 29 shows a plot of a constant time ramp from –80 dB to –6 dB (half scale) using 128 steps; thus, the ramp takes the same amount of time as the previous ramp from –80 dB to 0 dB. A constant time decreasing ramp plot is shown in Figure 30.

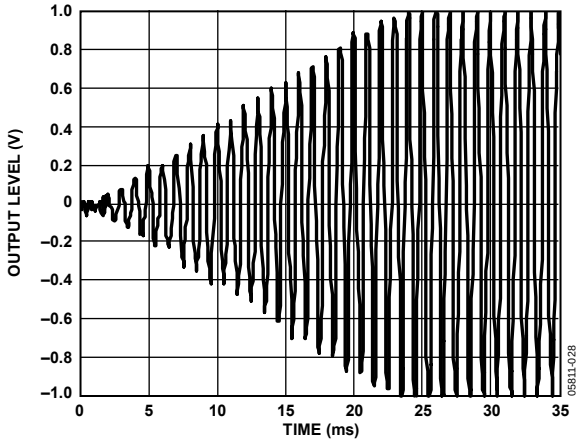

Figure 28. Slew RAM—Constant Time Update Increasing Ramp, Full Scale

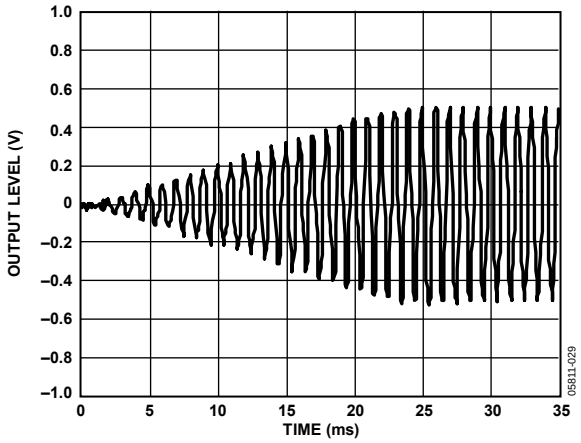

Figure 29. Slew RAM—Constant Time Update Increasing Ramp, Half Scale

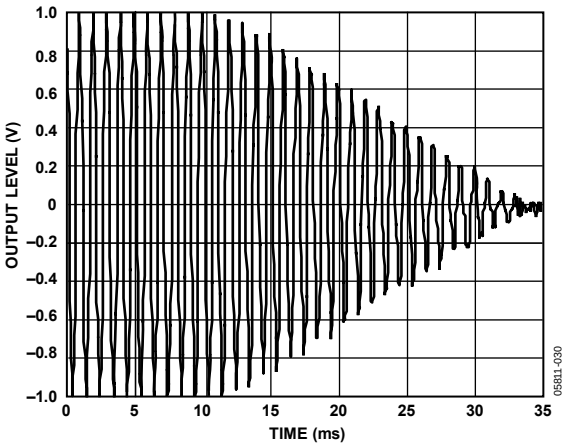

Figure 30. Slew RAM—Constant Time Update Decreasing Ramp, Full Scale

SAFE LOAD REGISTERS

Many applications require real-time control of signal processing parameters, such as filter coefficients, mixer gains, multichannel virtualizing parameters, or dynamics processing curves.

For example, if we consider a biquad to prevent instability from occurring, all five parameters of a biquad filter must be updated at the same time. Otherwise, the filter may execute with a mix of old and new coefficients for one or two audio frames. To eliminate this problem, the ADAV400 uses the safe load registers; there are five registers for the 28-bit parameter data and five for the parameter addresses. These addresses will indirectly address either the parameter RAM or the target/slew RAM.

Once these registers are loaded, the appropriate initiate safe transfer bit (there are separate bits for parameter and target/slew loads) in the audio core control register should be set.

The last five instructions of the program RAM are used for the safe load process, so the program length should be limited to 2555 cycles (2560 − 5). It is guaranteed that the safe load occurs within one LRCLK period (21 μs at f_S = 48 kHz) of the initiate safe transfer bit being set. Safe load only updates those safe load registers that have been loaded with new data since the last safe load operation. For example, if only two parameters or target RAM locations are to be updated, it is only necessary to load two of the safe load registers; the other safe load registers are ignored because they contain old data.

DATA CAPTURE REGISTERS

Data capture registers are used for debugging user-programmed blocks and are not required when using pre-existing library blocks.

The ADAV400 data capture feature allows the data at any node in the signal processing flow to be sent to one of six registers that can be read by the control port or to a serial output pin. Use this feature to monitor and display information about internal signal levels or compressor/limiter activity.

The ADAV400 contains six independent data capture registers that can be read via the I²C control port and can be used for monitoring static signals. In addition, two I²S digital output capture registers are available for monitoring dynamic signals.

For each of the data capture registers, a capture count and a register select must be set. The capture count is a number between 0 and 2559 that corresponds to the program step number where the capture will occur (see Table 15).

Table 15. Data Capture Control Registers

Register Bits	Function
13:2	12-bit program counter address
1:0	Register select
	00 = Mult_X_input
	01 = Mult_Y_input
	10 = MAC_output
	11 = Accum_fback

The register select field selects which one of four registers within the DSP core will be transferred to the data capture register when the program counter equals the capture count.

The capture count and register select bits are set by writing to one of the eight data capture registers at the following register addresses:

- 4170: Control Port Data Capture Setup Register 0
- 4171: Control Port Data Capture Setup Register 1
- 4172: Control Port Data Capture Setup Register 2
- 4173: Control Port Data Capture Setup Register 3
- 4174: Control Port Data Capture Setup Register 4
- 4175: Control Port Data Capture Setup Register 5
- 4176: Digital Out Data Capture Setup Register 0
- 4177: Digital Out Data Capture Setup Register 1

The captured data is in 5.19 twos complement data format for all eight register select fields. The four LSBs are truncated from the internal 5.23 data-word.

The formats for writing and reading to the data capture registers are listed in Table 22 and Table 23.

CONTROL PORT READ/WRITE DATA FORMATS

The read/write formats of the control port are designed to be byte oriented. To conform to this byte-oriented format, 0s are appended to the data fields before the MSB to extend the data-word to the next multiple of eight bits. For example, for parameter RAM, a 28-bit word is appended with four leading 0s, making the transfer four bytes; for program RAM, a 42-bit word is appended with six leading 0s, making the transfer six bytes. The data fields are appended to a 3-byte field consisting of a 7-bit chip address, a read/write bit, and an 11-bit RAM/register address for full I^2C transfer.

Burst mode is used to fill contiguous register or RAM locations. A burst mode write is initiated by writing the address and data of the first RAM/register location to be written followed by the next data-word, and so on. The ADAV400 control port auto-increments the internal address counter depending on the location being written to or read from, even across the boundaries of the different RAMs and registers locations.

Table 16. Parameter RAM Read/Write Format (Single Address)

Byte 0	Byte 1	Byte 2	Byte 3	Bytes [4:6]
chip_adr [6:0], R/$\overline{W}$	000, param_adr [12:8]	param_adr [7:0]	0000, param [27:24]	param [23:0]

Table 17. Parameter RAM Block Read/Write Format (Burst Mode)

Byte 0	Byte 1	Byte 2	Byte 3	Bytes [4:6]	Bytes [7:10]	Bytes [11:14]
chip_adr [6:0], R/$\overline{W}$	000, param_adr [12:8]	param_adr [7:0]	0000, param [27:24]	param [23:0]	0000 param [27:0]	0000 param [27:0]
			First parameter (param_adr)		Second parameter (param_adr + 1)	Third parameter (param_adr + 2)

Table 18. Program RAM Read/Write Format (Single Address)

Byte 0	Byte 1	Byte 2	Bytes [3:8]
chip_adr [6:0], R/$\overline{W}$	000, prog_adr [12:8]	prog_adr [7:0]	prog [42:0]

Table 19. Program RAM Block Read/Write Format (Burst Mode)

Byte 0	Byte 1	Byte 2	Bytes [3:8]	Bytes [9:14]	Bytes [15:20]
chip_adr [6:0], R/$\overline{W}$	000, prog_adr [12:8]	prog_adr [7:0]	prog [39:0]		
		First program word (prog_adr)		Second program word (prog_adr + 1)	Third program word (prog_adr + 2)

Table 20. Control Register Read/Write Format (16-Bit Register)

Byte 0	Byte1	Byte 2	Byte 3	Byte 4
chip_adr [6:0], R/$\overline{W}$	000, reg_adr [12:8]	reg_adr [7:0]	data [15:8]	data [7:0]

Table 21. Control Register Read/Write Format (8-Bit Register)

Byte 0	Byte1	Byte 2	Byte 3
chip_adr [6:0], R/$\overline{W}$	000, reg_adr [12:8]	reg_adr [7:0]	data [7:0]

Table 22. Data Capture Register Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
chip_adr [6:0], R/$\overline{W}$	000, data_capture_adr [12:8]	data_capture_adr [7:0]	000, progCount [10:6]	progCount [5:0], regSel [1:0]

Table 23. Data Capture (Control Port Readback) Register Read Format

Byte 0	Byte 1	Byte 2	Bytes [3:5]
chip_adr [6:0], R/$\overline{W}$	000, data_capture_adr [12:8]	data_capture_adr [7:0]	data [23:0]

Table 24. Safe Load Register Data Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Bytes [4:7]
chip_adr [6:0], R/$\overline{W}$	000, safeload_adr [12:8]	safeload_adr [7:0]	000000, data [33:32]	data [31:0]

Table 25. Safe Load Register Address Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
chip_adr [6:0], R/$\overline{W}$	000, safeload_adr [12:8]	safeload_adr [7:0]	0000, param_adr [11:8]	param_adr [7:0]

SERIAL DATA INPUT/OUTPUT PORTS

The flexible serial data input/output ports of the ADAV400 can be set to accept or transmit data in 2-channel format or in an 8- or 16-channel TDM stream. Data is processed in twos complement, MSB-first format. The left channel data field always precedes the right channel data field in the 2-channel streams. In the TDM modes, Slot 0 to Slot 3 (8-channel TDM) or Slot 0 to Slot 7 (16-channel TDM) fall in the first half of the audio frame, and Slot 4 to Slot 7 (8-channel TDM) or Slot 8 to Slot 15 (16-channel TDM) are in the second half of the frame. The serial modes are set in the serial input and output control registers.

The input and output control registers define the operation of the serial ports. Because BCLK1 and LRCLK1 are used for both input and output serial port timing, some care must be taken when individually programming serial modes. For example, programming the input serial port to TDM and the output port to left-justified is not a valid state.

In TDM mode, there are some restrictions to ADAV400 operation, which are outlined in Table 26. There are two modes of operation. In both 8-channel and 16-channel TDM modes, SDIN0 is the input for the TDM stream and SDO0 is the output.

Figure 34 shows the ADAV400 operating in TDM mode. Refer to the Serial Data Input/Output Ports section for a more complete description of the modes of operation.

Note that in 16-channel TDM mode, the ADC and DACs are no longer used because all 16 input and output channels have been redirected to the serial input and output ports.

Table 26. Serial Output Port Master/Slave Mode Capabilities

f_S	2-Channel Modes (I^2S, Left-Justified, Right-Justified)	8-Channel TDM	16-Channel TDM
48 kHz	Master and slave	Master and slave	Slave only
96 kHz	Master and slave	Master and slave	Slave only
192 kHz	Master and slave	Slave only	Slave only

Table 27. Data Format Configurations

Format	LRCLK Polarity	LRCLK Type	BCLK Polarity	MSB Position
I^2S (Figure 31)	Frame begins on falling edge	Clock	Data changes on falling edge	Delayed from LRCLK edge by one BCLK
Left-Justified (Figure 32)	Frame begins on rising edge	Clock	Data changes on falling edge	Aligned with LRCLK edge
Right-Justified (Figure 33)	Frame begins on rising edge	Clock	Data changes on falling edge	Delayed from LRCLK edge by 8, 12, or 16 BCLKs
TDM with Clock (Figure 34)	Frame begins on falling edge	Clock	Data changes on falling edge	Delayed from start of word clock by one BCLK
TDM with Pulse (Figure 35)	Frame begins on rising edge	Pulse	Data changes on falling edge	Delayed from start of word clock by one BCLK

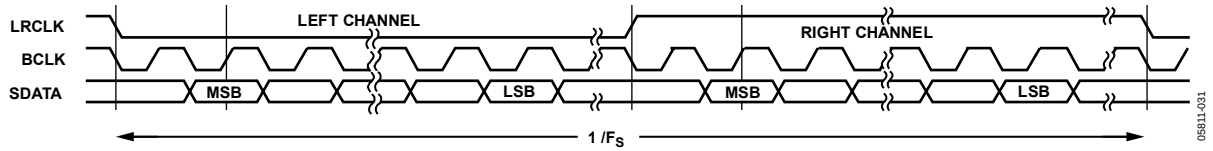

Figure 31. I²S Mode—16 to 24 Bits per Channel

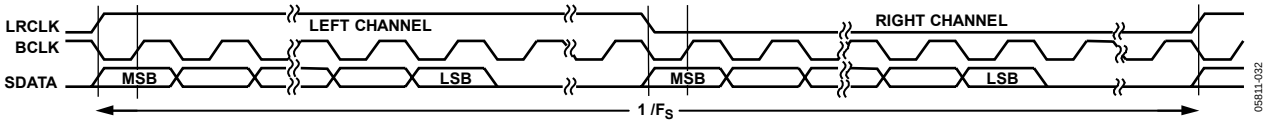

Figure 32. Left-Justified Mode—16 to 24 Bits per Channel

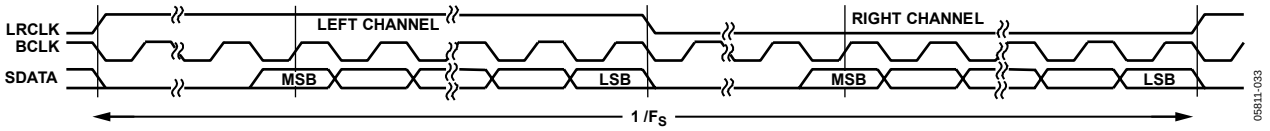

Figure 33. Right-Justified Mode—16 to 24 Bits per Channel

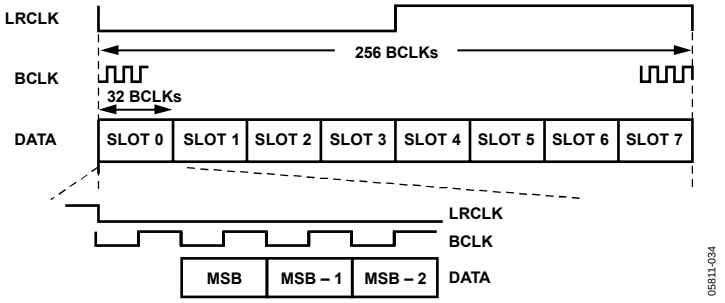

Figure 34. 8-Channel TDM Mode with Clock

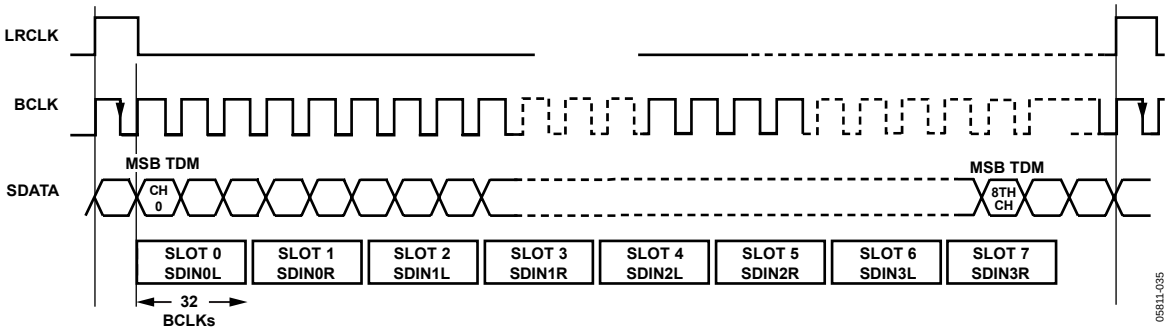

Figure 35. TDM Mode with Pulse Word Clock

CONTROL REGISTERS

Table 28. Audio Register Map

Register Address (Hex)	Register Name	Register Width (Bits)
0x1052	Audio core control register (see Table 29)	16
0x1053	RAM modulo control register (see Table 30)	8
0x1054	Serial output control register (see Table 31)	16
0x1055	Serial input control register (see Table 32)	8
0x1056	SRC serial port control register (see Table 33)	8
0x1057	ADC input mux control register (see Table 34)	16
0x1058	Power control register (see Table 35)	16
0x1059	User Control Register 1 (see Table 37)	16
0x105A	User Control Register 2 (see Table 36)	16
0x110D	DAC amplifier register (see Table 38)	16
0x1113	Headphone amplifier register (see Table 39)	16

Table 29. Audio Core Control Register
Register Address 0x1052 Default Readback = 0x4000

Register Bits	Function
15	Reserved (set to 0)
14[1]	Enable SDO2 and SDO3
	0 = enabled
	1 = disabled
13	Indicates when slew RAM is muted (read only)
12	Equivalent to writing 0s to the target RAM
	0 = normal operation
	1 = RAM zeroed
11	Reserved (set to 0)
10	Reserved (set to 0)
9	Clears internal processor registers (active low)
	0 = registers cleared
	1 = normal operation
8	Forces multiplier input to 0
	0 = normal operation
	1 = forced to 0
7	Initializes data RAM to 0
	0 = normal operation
	1 = enabled
6	Mutes serial input ports
	0 = normal operation
	1 = muted
5	Initiates safe load-to-target/slew RAM
	0 = off
	1 = on
4	Initiates safe load-to-parameter RAM
	0 = off
	1 = on
3:2	Reserved (set to 0)
1:0	Programs length
	00 = 2560 (48 kHz)
	01 = 1280 (96 kHz digital I/O only)
	10 = 640 (192 kHz digital I/O only)
	11 = reserved

[1] The polarity of this bit is inverted when read.

Table 30. RAM Modulo Control Register (Eight Bits)
Register Address 0x1053 Default = 0x28

Register Bits	Function
7:6	Reserved (set to 0)
5:0	RAM modulo size (1 LSB = 512 locations)

Table 31. Serial Output Control Register
Register Address 0x1054 Default = 0x0000

Register Bits	Function
15	Dither enable 0 = disabled 1 = enabled
14	TDM output mode 0 = 8-channel TDM 1 = 16-channel TDM
13	LRCLK polarity 0 = left low, right high 1 = left high, right low
12	BCLK polarity 0 = data changes on falling edge 1 = data changes on rising edge
11	Master/slave mode select 0 = slave 1 = master
10:9	BCLK frequency (master mode) 00 = 3.072 MHz (48 kHz) 01 = 6.144 MHz (96 kHz digital I/O only) 10 = 12.288 MHz (192 kHz digital I/O only) 11 = reserved
8:7	LRCLK frame sync frequency (master mode) 00 = 48 kHz 01 = 96 kHz 10 = 192 kHz 11 = reserved
6	Frame sync type 0 = LRCLK 1 = pulse
5	TDM enable 0 = serial data out 1 = TDM out
4:2	MSB position 000 = delay by 1 001 = delay by 0 010 = delay by 8 011 = delay by 12 100 = delay by 16 All others are reserved
1:0	Output word length 00 = 24 bits 01 = 20 bits 10 = 16 bits 11 = 16 bits

Table 32. Serial Input Control Register (Eight Bits)
Register Address 0x1055 Default = 0x00

Register Bits	Function
7:6	Reserved (set to 0)
5	TDM input mode 0 = 8-channel TDM 1 = 16-channel TDM
4	LRCLK polarity 0 = left low, right high 1 = left high, right low
3	BCLK polarity 0 = data changes on falling edge 1 = data changes on rising edge
2:0	Serial input mode 000 = I^2S 001 = left-justified 010 = 8-channel TDM 011 = right-justified, 24 bits 100 = right-justified, 20 bits 101 = right-justified, 18 bits 110 = right-justified, 16 bits All others are reserved

Table 33. SRC Serial Port Control Register (Eight Bits)
Register Address 0x1056 Default = 0x00

Register Bits	Function
7	Reserved (set to 0)
6:5	SRC serial input port select 00 = SDIN3 01 = SDIN2 10 = SDIN1 11 = SDIN0
4	LRCLK polarity 0 = left low, right high 1 = left high, right low
3	BCLK polarity 0 = data changes on falling edge 1 = data changes on rising edge
2:0	Serial input mode 000 = I^2S 001 = left-justified 010 = reserved 011 = right-justified, 24 bits 100 = right-justified, 20 bits 101 = right-justified, 18 bits 110 = right-justified, 16 bits All others are reserved

Table 34. ADC Input Mux Control Register
Register Address 0x1057 Default = 0x0001

Register Bits	Function
15:4	Reserved (set to 0)
3	AIN4 to ADC
2	AIN3 to ADC
1	AIN2 to ADC
0	AIN1 to ADC

Table 35. Power Control Register
Register Address 0x1058 Default = 0x0000

Register Bits	Function[1]
15	PLL
14	Reference buffer
13	ADC
12	VOUT4 DAC
11	VOUT3 DAC
10	VOUT2 DAC
9	VOUT1 DAC
8	AUX2 right DAC
7	AUX2 left DAC
6	AUX1/HP right DAC
5	AUX1/HP left DAC
4	Headphone amplifier right
3	Headphone amplifier left
2	SRC
1	Digital ADC and DAC engine
0	Audio processor

[1] 0 = powered down, 1 = powered up.

Table 36. User Control Register 2
Register Address 0x105A Default = 0x0000

Register Bits	Function
15:8	Reserved (set to 0)
7	Headphone amplifier mute 0 = normal operation 1 = mute
6:5	Reserved (set to 0)
4:0	Headphone amplifier attenuation 00000 = 0 dB 00001 = −1.5 dB 00010 = −3.0 dB …. …. 11110 = −45.0 dB 11111 = −46.5 dB

Table 37. User Control Register 1
Register Address 0x1059 Default Readback = 0x1E00

Register Bits	Function
15:13	Reserved (set to 0)
12:9	Reserved (set to 0) These bits read back as 0b1111
8	SRC mux enable 0 = disabled 1 = enabled
7	SRC lock indicator (read only) 0 = SRC not locked 1 = SRC locked
6	MCLKO pin enable 0 = MCLKO pin disabled 1 = MCLKO pin enabled
5:3	MCLKO select 000 = reserved 001 = 1024 × f_S (49.152 MHz) 010 = reserved 011 = reserved 1xx = 128 × f_S (6.144 MHz)
2:1	PLL clock select 00 = 64 × f_S (3.072 MHz) 01 = 128 × f_S (6.144 MHz) 10 = 256 × f_S (12.288 MHz) 11 = 512 × f_S (24.576 MHz)
0	PLL enable 0 = PLL bypassed 1 = PLL in use

Table 38. DAC Amplifier Register
Register Address 0x110D Default = 0x0000

Register Bits	Function
15:5	Reserved (set to 0)
4	DAC amplifier chopping[1] 0 = enabled 1 = disabled
3:0	Reserved (set to 0)

[1] Set this bit to 1 to obtain maximum performance from the DAC amplifier.

Table 39. Headphone Amplifier Register
Register Address 0x1113 Default = 0x0000

Register Bits	Function
15:1	Reserved (set to 0)
0	Headphone amplifier chopping[1] 0 = enabled 1 = disabled

[1] Set this bit to 1 to obtain maximum performance from the DAC amplifier.

AUDIO CORE CONTROL REGISTER

The bits in this register control the operation of the DSP core of the ADAV400 (see Table 29).

Enable SDO2 and SDO3 (Bit 14)

This bit is set to 1 by default and can be used to disable SDO2 and SDO3 if required.

Slew RAM Muted (Bit 13)

This bit is set to 1 when the slew RAM mute operation has been completed. This bit is read only and is automatically cleared by reading.

Write 0 to Target RAM (Bit 12)

Setting this bit to 1 is equivalent to writing 0s to all locations in the target RAM. This effectively mutes any slew RAMs, such as volume controls used in a signal flow. To enable normal operation, clear this bit to 0.

Clear Registers to All 0s (Bit 9)

Setting this bit to 0 sets the contents of the accumulators and serial output registers to 0. This bit defaults to 0; therefore, the ADAV400 powers up in clear mode and does not pass signals until a 1 is written to this bit. This is intended to prevent noises from inadvertently occurring during the power-up sequence.

Force Multiplier to 0 (Bit 8)

When this bit is set to 1, the input to the DSP multiplier is set to 0, which results in the multiplier output being 0. This control bit is included for maximum flexibility and is normally not used.

Initialize Data Memory with 0s (Bit 7)

Setting this bit to 1 initializes all data memory locations to 0. This bit is cleared to 0 after the operation is complete. Assert this bit after a complete program/parameter download has occurred to ensure click-free operation.

Zero Serial Input Port (Bit 6)

When this bit is set to 1, all input channels to the DSP core are forced to all 0s, effectively muting the output.

Initiate Safe Transfer to Target RAM (Bit 5)

Setting this bit to 1 initiates a safe load transfer to the target/slew RAM. This bit clears when the operation is complete. Of five safe load register pairs (address/data), only those registers that have been written since the last safe load event occurred are transferred. Address 0 corresponds to the first target RAM location.

Initiate Safe Transfer to Parameter RAM (Bit 4)

Setting this bit to 1 initiates a safe load transfer to the parameter RAM. This bit clears when the operation is complete. Of five safe load registers pairs (address/data), only those registers that have been written since the last safe load event occurred are transferred. Address 0 corresponds to the first parameter RAM location.

Program Length (Bits [1:0])

96 kHz and 192 kHz Modes

These bits set the length of the internal program. The default program length is 2560 instructions for f_S = 48 kHz, but the program length can be shortened by factors of 2 to accommodate sample rates higher than 48 kHz. For f_S = 96 kHz, set the program length to 1280 (01), and for f_S = 192 kHz, set the length to 640 steps (10).

Note that this is only valid for digital inputs and outputs.

RAM MODULO CONTROL REGISTER

The ADAV400 uses a modulo RAM addressing scheme that allows very efficient coding of filters and other blocks by automatically incrementing the data RAM pointer at the end of each sample period. This works well for most audio applications that involve filtering. However, in some cases auto-incrementing the data RAM pointer is undesirable—for example, when it is required to store a word in data RAM and then access it in a subsequent audio sample period.

For this reason, the data RAM in the ADAV400 can be partitioned into modulo and nonmodulo blocks by programming the RAM modulo control register (see Table 30). This register is programmed with the size of the modulo block required in blocks of 512 words, with a maximum data RAM size of 20,480 words, which is the default setting of the register. For example, if the register is programmed with the value 0x2, the modulo RAM is 1024 (2 × 512) words starting from Address 0 to Address 1023, and the nonmodulo RAM is 19,456 words starting from Address 1024.

This is not currently used in any of the library blocks within the development tool; however, it is included for maximum flexibility for custom software development.

SERIAL OUTPUT CONTROL REGISTERS

Dither Enable (Bit 15)

Setting this bit to 1 enables dither on the appropriate channels.

TDM Output Mode (Bit 14)

This bits selects either 8-channel or 16-channel TDM mode.

LRCLK Polarity (Bit 13)

When this bit is set to 0, the left channel data is clocked when LRCLK is low, and the right channel data is clocked when LRCLK is high. When this bit is set to 1, this sequence is reversed.

BCLK Polarity (Bit 12)

This bit controls on which edge of the bit clock the output data is clocked. Data changes on the falling edge of BCLK1 when this bit is set to 0, and on the rising edge when this bit is set to 1.

Master/Slave (Bit 11)

This bit determines whether the output port is a clock master or slave. The default setting is slave; on power-up, Pin BCLK1 and Pin LRCLK1 are set as inputs until this bit is set to 1, at which time they become clock outputs.

BCLK Frequency (Bits [10:9])

When the serial output port is a master, these bits set the frequency of the output bit clock, BCLK1.

Frame Sync Frequency (Bits [8:7])

When the output port is a master, these bits set the frequency of the output word clock on the LRCLK1.

Frame Sync Type (Bit 6)

This bit sets the type of signal on the LRCLK1 pin. When this bit is set to 0, the signal is a word clock with a 50% duty cycle; when this bit is set to 1, the signal is a pulse with a duration of one BCLK at the beginning of the data frame.

TDM Enable (Bit 5)

Setting this bit to 1 changes the output port from multiple serial outputs to a single TDM output stream available on SDO0. This bit must be set in both serial output control registers to enable 16-channel TDM on SDO0.

MSB Position (Bits [4:2])

These three bits set the position of the MSB of the data with respect to the LRCLK edge. The data outputs of the ADAV400 are always MSB first.

Output Word Length (Bits [1:0])

These bits set the word length of the output data-word. All bits following the LSB are set to 0.

SERIAL INPUT CONTROL REGISTER

TDM Input Mode (Bit 5)

This bit selects either 8-channel or 16-channel TDM mode.

LRCLK Polarity (Bit 4)

When this bit is set to 0, the left channel data on SDINx is clocked in when LRCLK1 is low, and the right channel input data is clocked in when LRCLK1 is high. When this bit is set to 1, this sequence is reversed.

In TDM mode, when this bit is set to 0, data is clocked on the next valid BCLK edge (polarity of BCLK is set in Bit 3 of this register) following a falling edge on LRCLK1. When this bit is set to 1 and running in TDM mode, the input data is valid on the BCLK edge following a rising edge on LRCLK1.

The serial input port can also operate with LRCLK1 as a pulse, rather than a clock. In this case, the first edge of the pulse is used by the ADAV400 to start the data frame. When the polarity bit is set to 0, data is clocked in on the falling edge of LRCLK1; when this bit is set to 1, data is clocked in on the rising edge.

BCLK Polarity (Bit 3)

This bit controls on which edge of the bit clock the input data changes and on which edge it is clocked. Data changes on the falling edge of BCLK1 when this bit is set to 0, and on the rising edge when this bit is set at 1.

Serial Input Mode (Bits [2:0])

These two bits control the data format that the input port expects to receive. It should be noted that Bit 3 and Bit 4 of the serial input control register will override these settings, so Bits 4 to Bit 0 must be set for correct operation. Refer to Figure 31, Figure 32, Figure 33, and Figure 34 for details on the different modes.

Table 27 can also be used to verify register settings for each serial data format.

SRC SERIAL PORT CONTROL REGISTER

SRC Serial Input Port Select (Bits [6:5])

These bits select which of the four serial data inputs are directed to the SRC.

LRCLK Polarity (Bit 4)

When this bit is set to 0, the left channel data on the selected channel is clocked in when LRCLK0 is low, and the right channel input data is clocked in when LRCLK1 is high. When this bit is set to 1, this sequence is reversed.

BCLK Polarity (Bit 3)

This bit controls on which edge of the bit clock the input data changes and on which edge it is clocked. Data changes on the falling edge of BCLK0 when this bit is set to 0, and on the rising edge when this bit is set to 1.

Serial Input Mode (Bits [2:0])

These two bits control the data format that the input port expects to receive. It should be noted that Bit 3 and Bit 4 of the serial input control register will override these settings, so Bits 4 to Bit 0 must be set for correct operation. Refer to Figure 31, Figure 32, Figure 33, and Figure 34 for details on the different modes. Table 27 can also be used to verify register settings for each serial data format.

Note that TDM is not supported on the SRC.

ADC INPUT MUX REGISTER

ADC Input Mux (Bits [3:0])

These bits are used to select which of the analog inputs are directed to the ADC. It is recommended that only one channel is selected at any time.

POWER CONTROL REGISTER

Power Control (Bits [15:0])

These bits can individually power up or power down the blocks of the ADAV400.

USER CONTROL REGISTER 2

Headphone Amplifier Mute (Bit 7)

When set, this bit mutes the analog headphone amplifier.

Headphone Amplifier Attenuation (Bits [4:0])

These bits set the analog gain of the headphone amplifier. It can be set in steps of −1.5 dB from 0 dB to −46.5 dB.

USER CONTROL REGISTER 1

SRC Mux Enable (Bit 8)

When this bit is set to 1, the SRC mux is enabled, passing the input selected by the SRC serial port control register to the SRC block, the output of which is then available to the DSP core. It also masks the selected serial data input as a direct input to the DSP core. See Figure 36 for more details on the SRC input configuration.

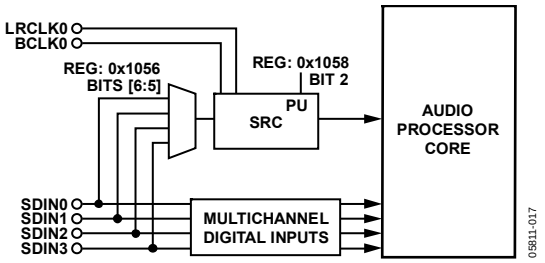

Figure 36. SRC Input Configuration

SRC Lock Indicator (Bit 7)

This bit is read only and indicates when the SRC is locked.

MCLKO Pin Enable (Bit 6)

With this bit set to 1, MCLKO is enabled and outputs the frequency selected by Bit 5 to Bit 3 in this register.

MCLKO Select (Bits [5:3])

These bits select the MCLKO frequency. All reserved settings are test modes and are not valid audio clocks.

PLL Clock Select (Bits [2:0])

These bits must be programmed to select the master clock, MCLKI, input frequency that is being used. For example, the default case is 64 × f_S (3.072 MHz), which means that BCLKx can also be used as the MCLKI.

DAC AMPLIFIER REGISTER

DAC Amplifier Chopping (Bit 4)

This bit should be set to 1 to ensure best performance on the headphone outputs.

TYPICAL APPLICATION DIAGRAM

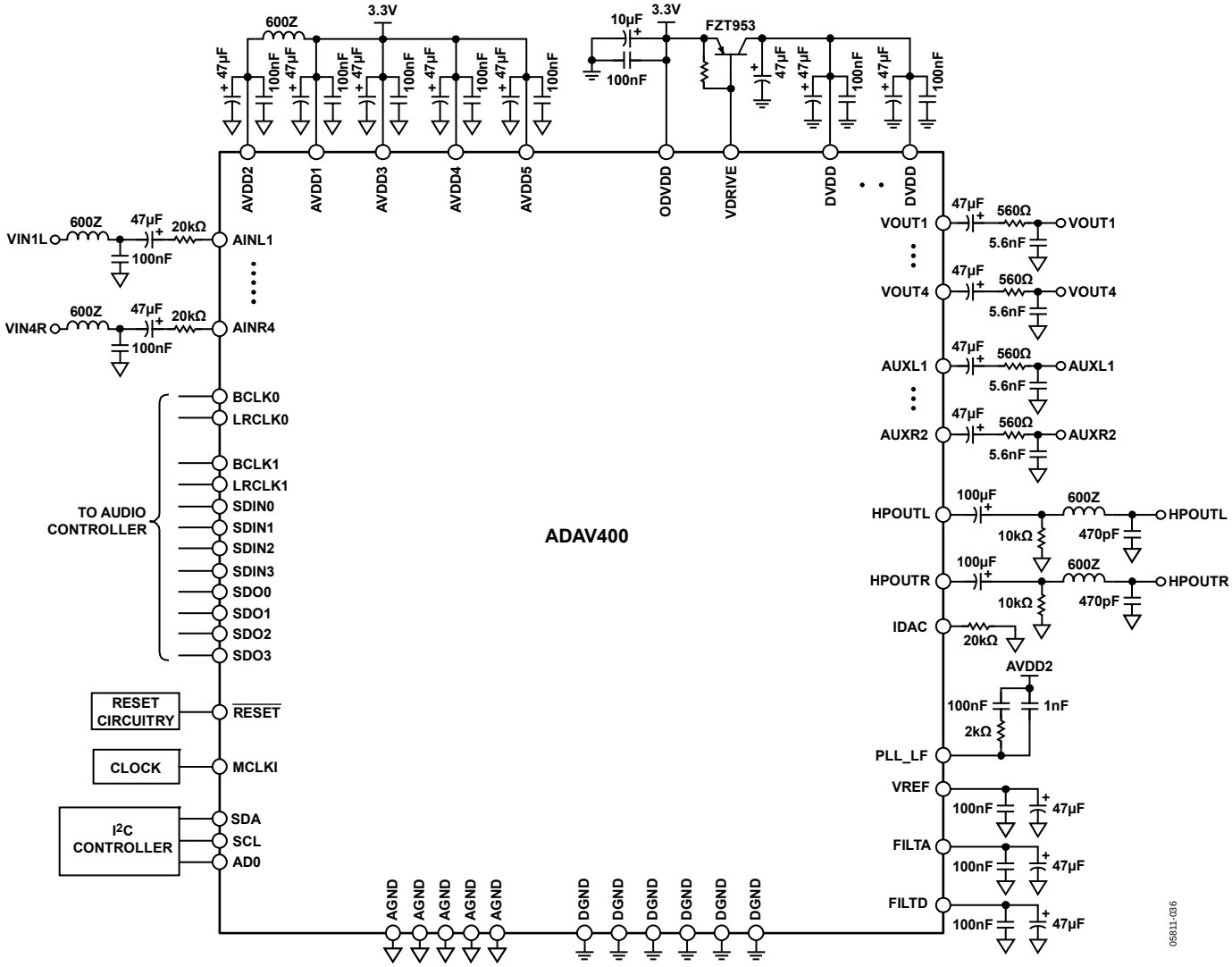

Figure 37. Typical Application Circuit

OUTLINE DIMENSIONS

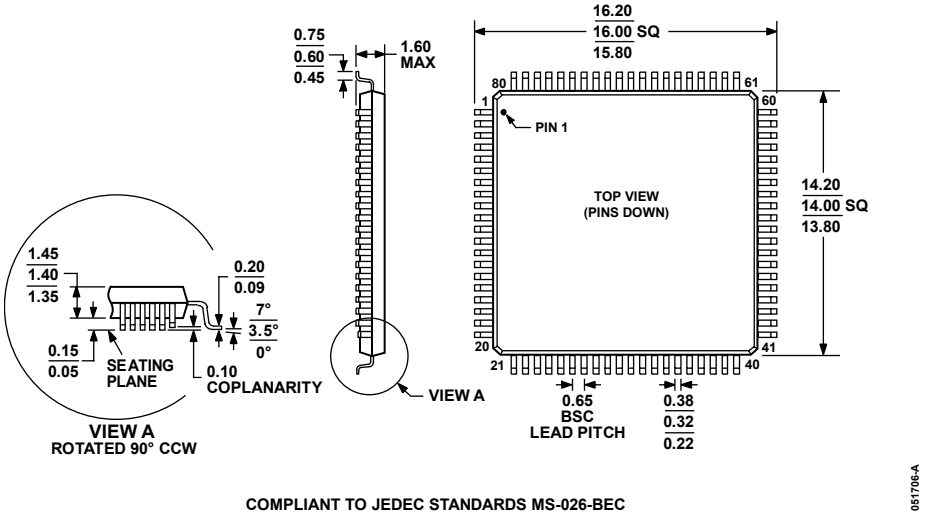

Figure 38. 80-Lead Low Profile Quad Flat Package [LQFP]
(ST-80-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADAV400KSTZ[1]	0°C to 70°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-2
ADAV400KSTZ-REEL[1]	0°C to 70°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-2
EVAL-ADAV400EBZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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