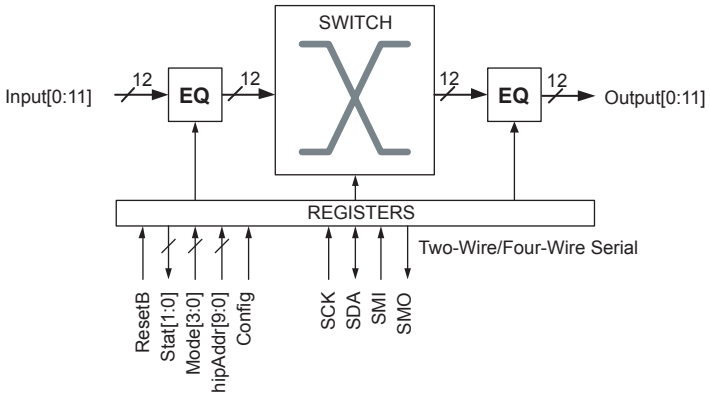
DATA INTERCONNECT

VSC3312

VITESSE®

6.5 Gbps 12x12 Crosspoint Switch

BLOCK DIAGRAM:



FEATURES:	BENEFITS:
6.5 Gbps non-return-to-zero (NRZ) data bandwidth	Transparent support for virtually all data rates and protocols
Fully non-blocking and multicasting switch core with per-pin signal inversion capability	Allows complete flexibility in routing and distributing signals
Multiple time-constant programmable input and output equalization	Compensates for multiple impairments in a signal path
Wide equalization adjustment range	Supports all types of interconnect media: PCB, backplanes, and cable
Fully asynchronous operation with <1 ns latency	No adjustments based on data rate or reference clock required
Reconfigurable Input/Output (I/O) capability	Customize the I/O to the application
LOS detection and forwarding	OOB forwarding for protocols like SAS and SATA

APPLICATIONS:

- Wideband signal switching and clean-up
- Line driver or receiver
- Backplane signal fanout, driver, or receiver
- Copper cable driver or receiver
- PCB signal enhancement

VPPD-01370
Revision 1.0

VSC3312

6.5 Gbps 12x12 Crosspoint Switch

GENERAL DESCRIPTION:

The VSC3312 is a 12-port 6.5 Gbps asynchronous switch with advanced signal equalization designed for high-speed serial backplanes and cable interconnect applications. VSC3312 switches allow multicast, loopback, and reconfigurable Input/Output (I/O) capability, allowing for great flexibility in allocating and routing signals in a broad range of applications. The VSC3312 includes dual time-constant equalization, which significantly reduces jitter associated with driving multigigabit signals across backplanes and cables.

Using a fully asynchronous architecture allows any data rate or protocol on any channel without the need for an external reference clock. This gives the VSC3312 wire-like interoperability in virtually any application that uses binary signaling.

The VSC3312 can also be used as a buffer that simplifies and enhances the design of high-speed signal paths by providing signal equalization at both inputs and outputs to reduce or reverse signal degradation due to transmission line effects.

The VSC3312 has a total of 24 ports. Eight are dedicated inputs, eight are dedicated outputs, and the remaining eight may be configured as either inputs or outputs without restriction. This design provides the flexibility of using the device as a standard 12x12 crosspoint, or any ratio from 8x16 to 16x8. This unique feature allows full I/O utilization in any application that has less than a 2:1 ratio between inputs and outputs. In many cases, this translates to a significant reduction in chip count.

Featuring programmable input signal equalization and output pre-emphasis, each with multiple time constants, the VSC3312 is also ideal for countering signal degradation over a wide variety of transmission media types and lengths.

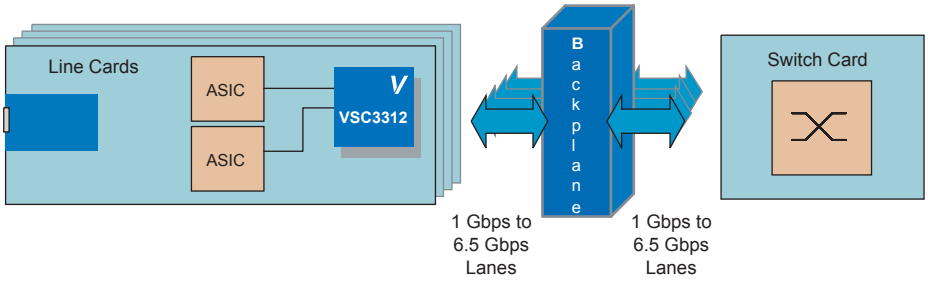
Typical power consumption for the device is 160 mW per active channel, and unused channels may be de-activated to save the power associated with those ports. The output drivers for the VSC3312 also a feature a wide supply voltage range, from 1.8 V to 3.3 V, that allows flexibility in matching the output swing to the application requirements.

The VSC3312 has a LOS detector with programmable thresholds on every input port. The LOS status can be made to appear at either of two status pins for external use. The LOS signal can also be switched to each of the outputs in concert with the high-speed switching core. LOS forwarding can be enabled for each of the outputs, which will cause the outputs to be squelched in response to a LOS detect at the corresponding input, thereby propagating signal envelopes through the switch.

Programming of the VSC3312 is through a standard two-wire serial interface. The interface address can be hardwired through static pins or through a proprietary two-pin interface that allows for address selection after power-up. All pin functions such as Config, ResetB, and Status pin states are also accessible through registers to ensure maximum flexibility.

For more information about signal integrity solutions, visit the Vitesse Web site at www.vitesse.com/SI.

BACKPLANE APPLICATION:



SPECIFICATIONS:

- 6.5 Gbps non-return-to-zero (NRZ) per-channel data rate
- 2.5 V core, 1.8 V, 2.5 V, and 3.3 V high-speed I/O
- 3.2 W maximum at 3.3 V, or 2.4 W at 2.5 V, or 2 W at 1.8 V

741 Calle Plano
Camarillo, CA 93012, USA
Tel: +1 805.388.3700
Fax: +1 805.987.5896
www.vitesse.com
sales@vitesse.com