FAIRCHILD SEMICONDUCTOR™

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MM74C914
Hex Schmitt Trigger with Extended Input Voltage

General Description

The MM74C914 is a monolithic CMOS Hex Schmitt trigger with special input protection scheme. This scheme allows the input voltage levels to exceed V_{CC} or ground by at least 10V (V_{CC} −25V to GND + 25V), and is valuable for applications involving voltage level shifting or mismatched power supplies.

The positive and negative-going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (typ 0.0005V/°C at V_{CC} = 10V). And the hysteresis, $V_{T+} - V_{T-} \geq 0.2\ V_{CC}$ is guaranteed.

Features

- Hysteresis: 0.45 V_{CC} (typ.) 0.2 V_{CC}guaranteed
- Special input protection: Extended Input Voltage Range
- Wide supply voltage range: 3V to 15V
- High noise immunity: 0.7 V_{CC} (typ.)
- Low power TTL compatibility: Fan out of 2 driving 74L

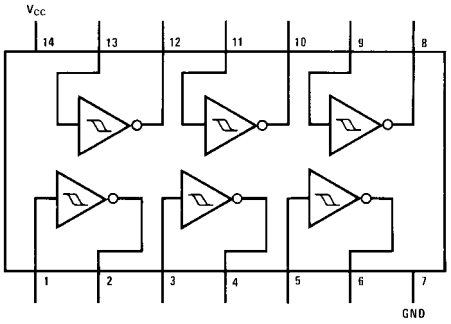
Ordering Code:

Order Number	Package Number	Package Description
MM74C914M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
MM74C914N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

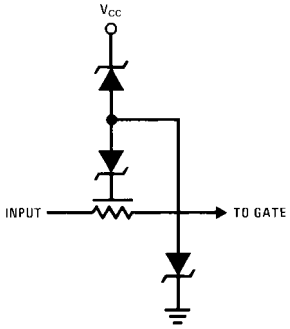
Connection Diagrams

Pin Assignments for DIP



Top View

Special Input Protection



8V ≈ 25V
for the diodes.

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Absolute Maximum Ratings (Note 1)

Voltage at any Input Pin	V_{CC} − 25V to GND + 25V
Voltage at any other Pin	−0.3Vto V_{CC} + 0.3V
Operating Temperature Range (T_A)	−40°C to +85°C
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum (V_{CC})	18V
Lead Temperature (T_L)	
(Soldering, 10 seconds)	300°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics tables provide conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
V_{T+}	Positive Going Threshold Voltage	V_{CC} = 5V	3.0	3.6	4.3	V
		V_{CC} = 10V	6.0	6.8	8.6	V
		V_{CC} = 15V	9.0	10	12.9	
V_{T-}	Negative Going Threshold Voltage	V_{CC} = 5V	0.7	1.4	2.0	V
		V_{CC} = 10V	1.4	3.2	4.0	V
		V_{CC} = 15V	2.1	5	6.0	
$V_{T+} - V_{T-}$	Hysteresis	V_{CC} = 5V	1.0	2.2	3.6	V
		V_{CC} = 10V	2.0	3.6	7.2	V
		V_{CC} = 15V	3.0	5	10.8	V
$V_{OUT(1)}$	Logical"1" Output Voltage	V_{CC} = 5V, I_O = −10 µA	4.5			V
		V_{CC} = 10V, I_O = −10 µA	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = +10 µA			0.5	V
		V_{CC} = 10V, I_O = +10 µA			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 25V		0.005	5.0	µA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = −10V	−100	−0.005		µA
I_{CC}	Supply Current	V_{CC} = 15V, V_{IN} = − 10V/25V		0.05	300	µA
		V_{CC} = 5V, V_{IN} = − 2.5V (Note 2)		20		µA
		V_{CC} = 10V, V_{IN} = 5V (Note 2)		200		µA
		V_{CC} = 15V, V_{IN} = 7.5V (Note 2)		600		µA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	4.3			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			0.7	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V, I_O = −360 µA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 4.75V, I_O = 360 µA			0.4	V
OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

Note 2: Only one input is at ½ V_{CC}, the others are either at V_{CC} or GND.

AC Electrical Characteristics (Note 3)

$T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay from Input to Output	$V_{CC} = 5V$		220	400	ns
t_{PLH}		$V_{CC} = 10V$		80	200	ns
C_{IN}	Input Capacitance	Any Input (Note 4)		5		pF
C_{PD}	Power Dissipation Capacitance	Per Gate (Note 5)		20		pF

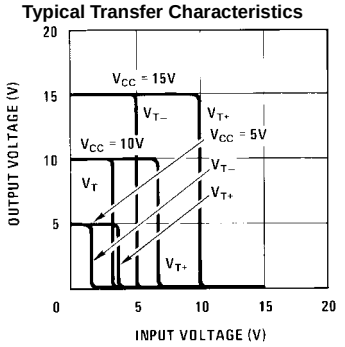
Note 3: AC Parameters are guaranteed by DC correlated testing.

Note 4: Capacitance is guaranteed by periodic testing.

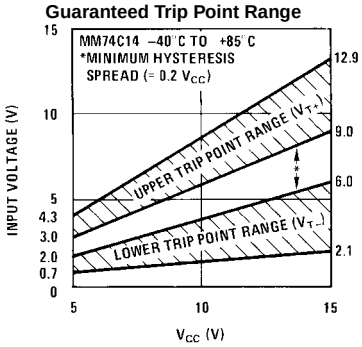
Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics Application Note, AN-90.

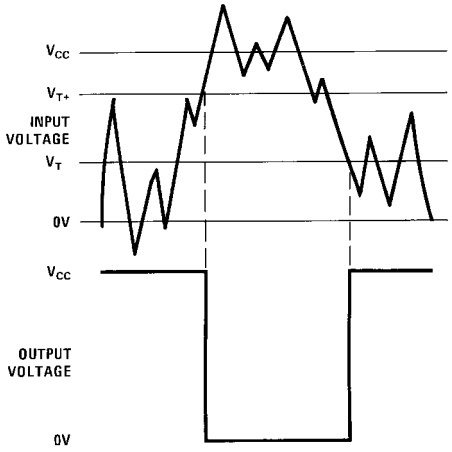
Typical Performance Characteristics

Typical Transfer Characteristics

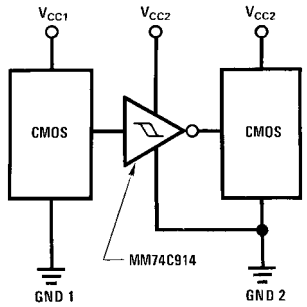


Guaranteed Trip Point Range





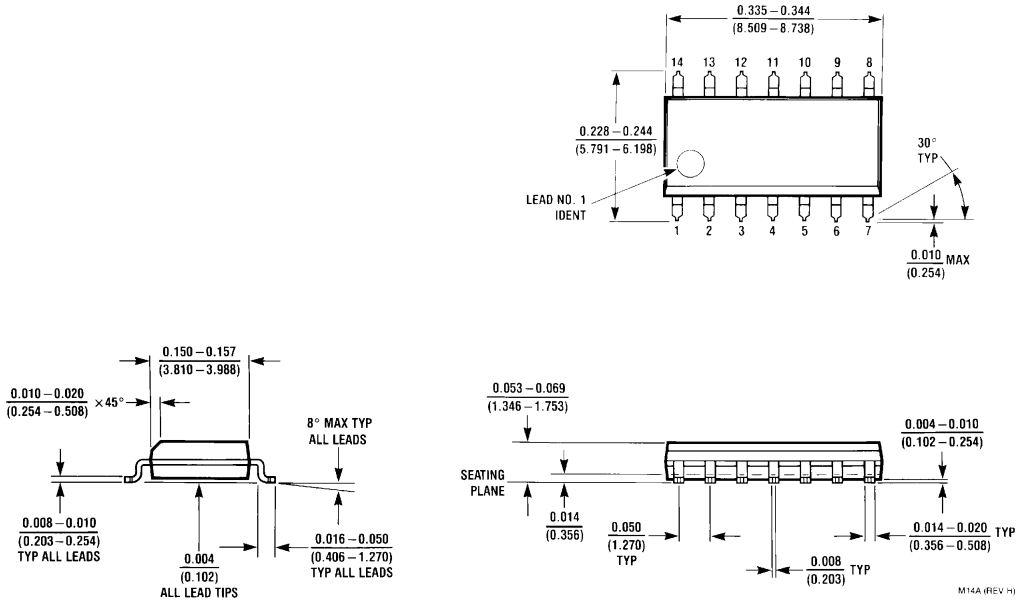
Typical Application



Note: $V_{CC1} = V_{CC2}$

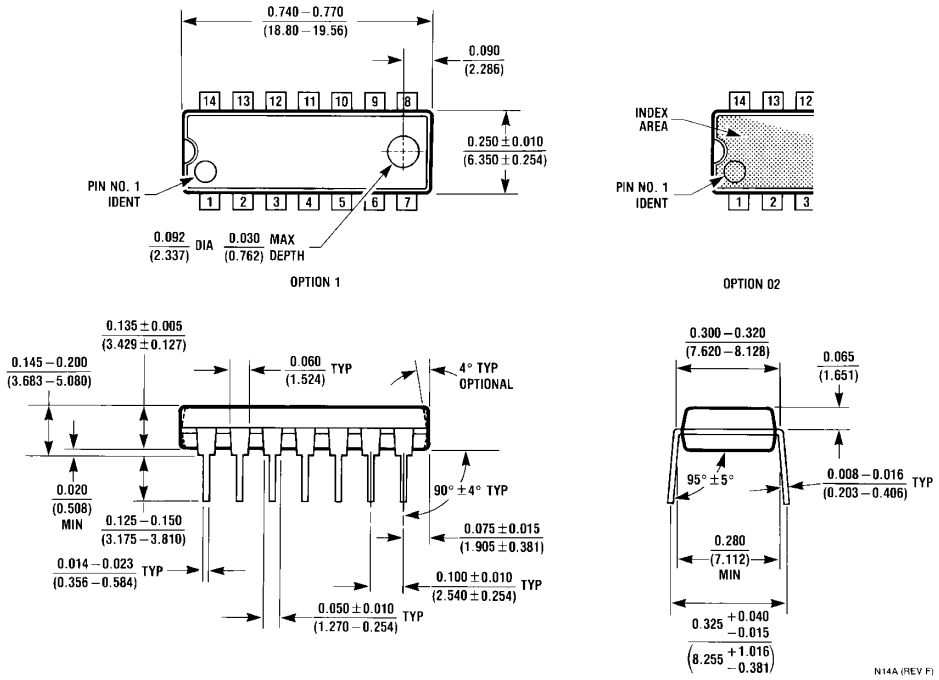
GND1 = GND2

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

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