Ordering number : ENA1254A

STK672-340-E

ON Semiconductor®

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Thick-Film Hybrid IC

Unipolar Fixed-Current Chopper (External-Excited PWM) Scheme and Built-in Phase Signal Distribution IC

Two-Phase Stepping Motor Driver (Square Wave Drive) Output Current 2.2A

Overview

The STK672-340-E is a unipolar fixed-current chopper type 2-phase stepping motor driver hybrid IC. It features power MOSFETs in the output stage and a built-in phase signal distribution IC. The incorporation of a phase distribution IC allows the STK672-340-E to control the speed of the motor based on the frequency of an external input clock signal. It supports two types of excitation for motor control: 2-phase excitation and 1-2 phase excitation. It also provides a function for switching the motor direction.

The STK672-340-E features an ENABLE pin, a function not provided in the STK672-120-E. When the ENABLE pin is set low while the clock signal is being supplied, all MOSFET devices are forced to the off state. When ENABLE is set high again later, the IC resumes operation, continuing with the prior excitation timing.

Applications

- Two-phase stepping motor drive in send/receive facsimile units.
- Paper feed in copiers, industrial robots, and other applications that require 2-phase stepping motor drive.

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Features

- The motor speed can be controlled by the frequency of an external clock signal (the CLOCK pin signal).
- The excitation type is switched according to the state (low or high) of the MODE pin. The mode is set to 2-phase or 1-2 phase excitation on the rising edge of the clock signal.
- A motor direction switching pin (the CWB pin) is provided.
- Supports Schmitt input for 2.5V High level input.
- The motor current can be set by changing the Vref pin voltage. Since a 0.14Ω current detection resistor is built in, a current of 1A is set for each 0.14V of applied voltage.
- The input frequency range for the clock signal used for motor speed control is 0 to 50kHz.
- Supply voltage ranges: V_{CC} = 10 to 42V, V_{DD} = 5.0V ±5%
- This IC supports motor operating currents of up to 2.2A at Tc = 105°C, and of up to 3.6A at Tc = 25°C.
- Provides a function that, during clock input, forces all MOSFET devices to the off state when the ENABLE pin is set low, and then, when ENABLE is set high, resumes operation continuing with the prior excitation timing.

Specifications

Absolute Maximum Ratings at Tc = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	V_{CC} max	No signal	52	V
Maximum supply voltage 2	V_{DD} max	No signal	-0.3 to +7.0	V
Input voltage	V_{IN} max	Logic input pins	-0.3 to +7.0	V
Output current	I_{OH} max	V_{DD} = 5V, CLOCK ≥ 200Hz	3.6	A
Allowable power dissipation	Pd max	With an arbitrarily large heat sink. Per MOSFET	8	W
Operating substrate temperature	Tc max		105	°C
Junction temperature	Tj max		150	°C
Storage temperature	Tstg		-40 to +125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	unit
Operating supply voltage 1	V_{CC}	With signals applied	10 to 42	V
Operating supply voltage 2	V_{DD}	With signals applied	5.0±5%	V
Input voltage	V_{IH}		0 to V_{DD}	V
Output current 1	$I_{OH}1$	Tc=105°C, CLOCK≥200Hz	2.2	A
Output current 2	$I_{OH}2$	Tc=80°C, CLOCK≥200Hz, See the motor current (I_{OH}) derating curve	2.7	A
CLOCK frequency	f_{CL}	Minimum pulse width: at least 10μs	0 to 50	kHz
Phase driver withstand voltage	V_{DSS}	I_D=1mA (Tc=25°C)	100min	V
Recommended operating substrate temperature	Tc	No condensation	0 to 105	°C

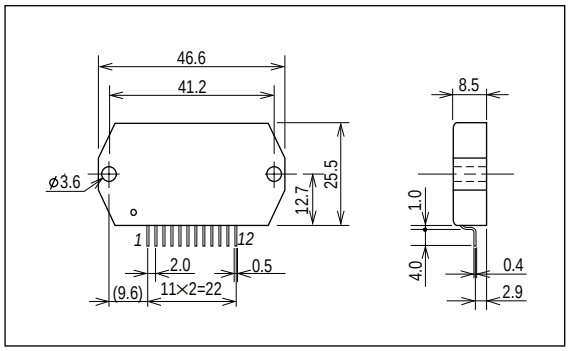
Electrical Characteristics at Tc = 25°C, V_{CC} = 24V, V_{DD} = 5V

Parameter	Symbol	Conditions	Rating			unit
			min	typ	max	
V_{DD} supply current	I_{CCO}	CLOCK=GND		3.1	7	mA
Output average current	Ioave	With R/L=3Ω/3.8mH in each phase Vref = 0.137V	0.52	0.58	0.64	A
FET diode forward voltage	Vdf	If=1A (R_L=23Ω)		1.1	1.7	V
Output saturation voltage	Vsat	R_L=23Ω		0.31	0.44	V
Input high voltage	V_{IH}	Pins 8 to 12 (5 pins)	2.5			V
Input low voltage	V_{IL}	Pins 8 to 12 (5 pins)			0.6	V
Input current	I_{IL}	With pins 8 to 12 at the ground level.			10	μA
Vref input voltage	VrH	Pin 7	0		3.5	V
Vref input bias current	I_{IB}	With pin 7 at 1V		50	500	nA
PWM frequency	fc		35	45	55	kHz

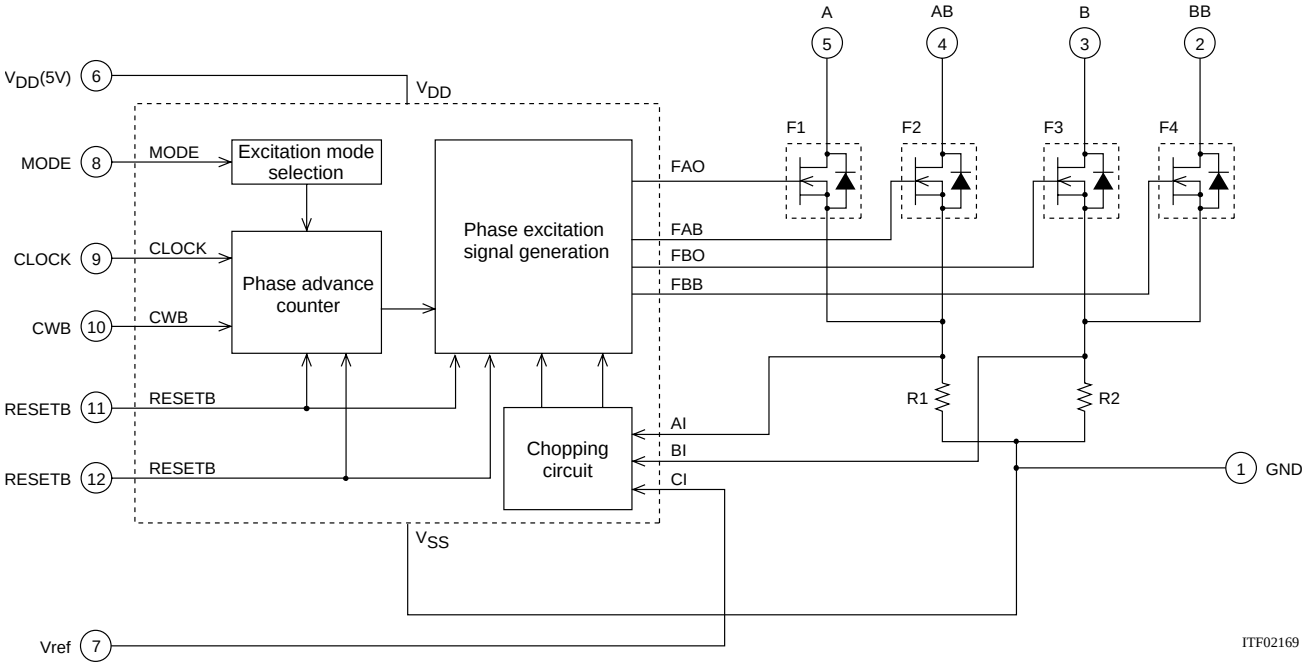
Note: A fixed-voltage power supply must be used.

Package Dimensions

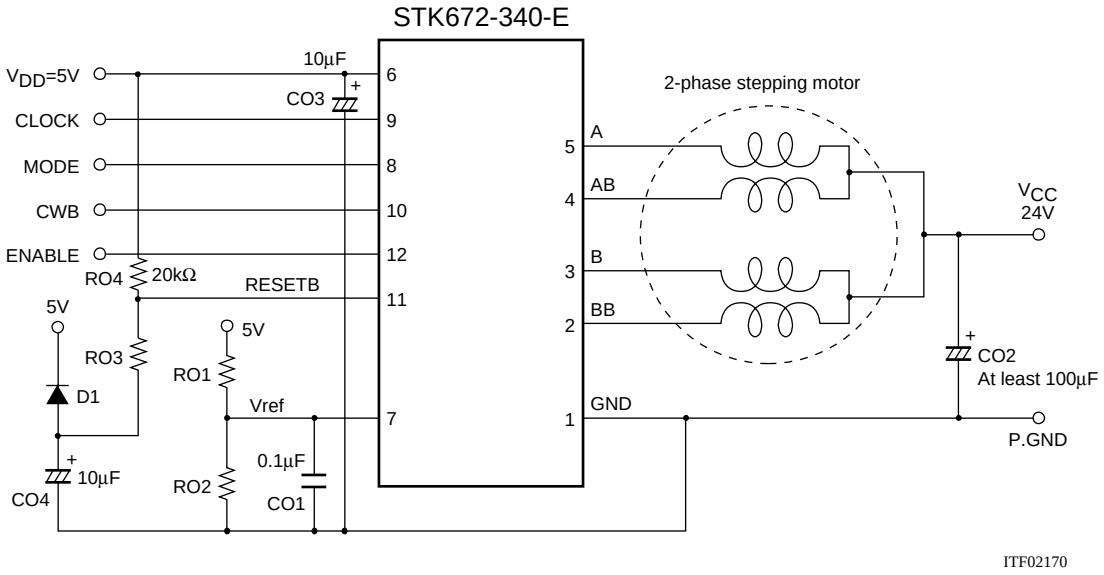
unit:mm (typ)



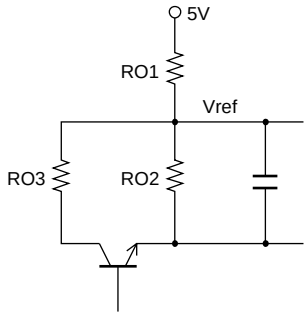
Internal Equivalent Circuit Block Diagram

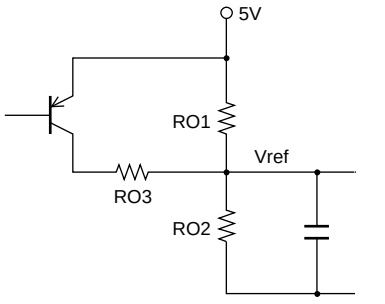


Sample Application Circuit

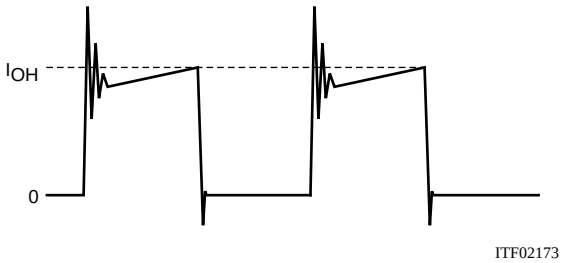


- To minimize noise in the 5V system, locate the ground side of capacitor CO2 in the above circuit as close as possible to pin 1 of the IC. Also, if at all possible, the ground used for Vref must not be common to the P.GND pattern, but must be directly wired from pin 1.
- Insert resistor RO3 (47 to 100Ω) so that the discharge energy from capacitor CO4 is not directly applied to the CMOS IC in this hybrid device. If the diode D1 has Vf characteristics with Vf less than or equal to 0.6V (when If = 0.1A), this will be smaller than the CMOS IC input pin diode Vf. If this is the case RO3 may be replaced with a short without problem.
- Apply 2.5V High level input to pins 8, 9, 10, 11, and 12.
- Since the input pins do not have built-in pull-up resistors, when the open-collector type pins 8, 9, 10, 11, and 12 are used as inputs, a 10 to 47kΩ pull-up resistor (to V_{DD}) must be used.
- To prevent incorrect operation due to chopping noise, we recommend inserting 470 to 1000pF capacitors between pin 1 and each of the pins 8, 9, 10, and 12.
  (With the open-collector type IC, we also recommend inserting a 470 to 1000pF capacitor between pin 11 (RESETB) and pin 1 when pin 11 is used as an input.)
- The following circuit (for a lowered current of over 0.2A) is recommended if the application needs to temporarily lower the motor current. Here, a value of close to 100kΩ must be used for resistor RO1 to make the transistor output saturation voltage as low as possible.





• Motor current peak value I_{OH} setting



I_{OH} = Vref ÷ Rs
Vref = (RO2 ÷ (RO1 + RO2)) × 5V (or 3.3V)
Rs is the hybrid IC internal current detection resistor.
In the STK672-330-E (and STK672-350-E) Rs is 0.195Ω.
(In the STK672-340-E and STK672-360-E, Rs is 0.14Ω.)

Input Pin Functions

Pin Name	Pin No.	Function	Input Conditions When Operating
CLOCK	9	Reference clock for motor phase current switching	Operates on the rising edge of the signal
MODE	8	Excitation mode selection	Low: 2-phase excitation High: 1-2 phase excitation
CWB	10	Motor direction switching	Low: CW (forward) High: CCW (reverse)
RESETB	11	System reset and A, AB, B, and BB outputs cutoff. Applications must apply a reset signal for at least 10μs when V_{DD} is first applied.	A reset is applied by a low level
ENABLE	12	The A, AB, B, and BB outputs are turned off, and after operation is restored by returning the ENABLE pin to the high level, operation continues with the same excitation timing as before the low-level input.	The A, AB, B, and BB outputs are turned off by a low-level input.

(1) A simple reset function is formed from D1, CO4, RO3, and RO4 in this application circuit. With the CLOCK input held low, when the 5V supply voltage is brought up a reset is applied if the motor output phases A and BB are driven. If the 5V supply voltage rise time is slow (over 50ms), the motor output phases A and BB may not be driven. Increase the value of the capacitor CO4 and check circuit operation again.
(2) See the timing chart for the concrete details on circuit operation.

Usage Notes

1. STK672-340-E input signal functions and timing (Specifications common to the STK672-330-E as well)
(All inputs have no internal pull-up resistor.)

[RESETB and CLOCK (Input signal timing when power is first applied)]
As shown in the timing chart, a RESETB signal input is required by the driver to operate with the timing in which the F1 gate is turned on first. The RESETB signal timing must be set up to have a width of at least 10μs, as shown below. The capacitor CO4, and the resistors RO3 and RO4 in the application circuit form simple reset circuit that uses the RC time constant rising time. However, when designing the RESETB input based on V_{IH} levels, the application must have the timing shown in figure 1.

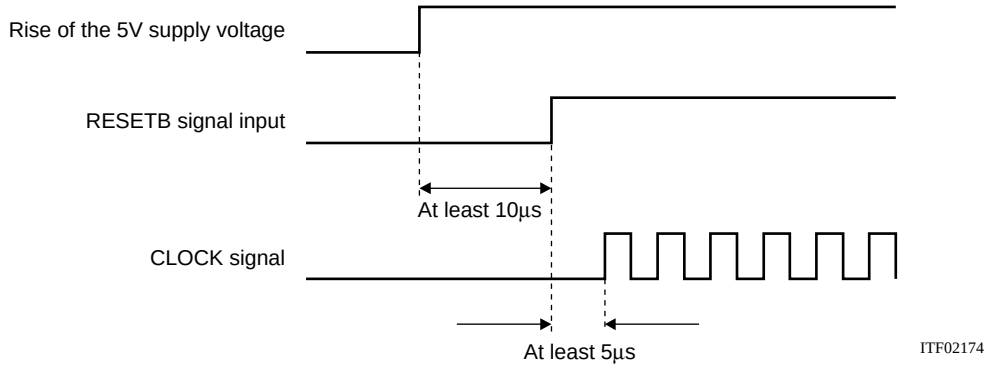


Figure 1 RESETB and CLOCK Signals Input Timing

[CLOCK (Phase switching clock)]
- Input frequency: DC to 50kHz
- Minimum pulse width: 10μs
- Signals are read on the rising edge.

[CWB (Motor direction setting)]

The direction of rotation is switched by setting CWB to 1 (high) or 0 (low). See the timing charts for details on the operation of the outputs.

Note: The state of the CWB input must not be changed during the 6.25μs period before and after the rising edge of the CLOCK input.

[ENABLE (Forcible on/off control of the A, AB, B, and BB outputs, and selection of the operate or hold state for hybrid IC internal operation)]

ENABLE = 1 (high): Normal operation

ENABLE = 0 (low): Outputs A, AB, B, and BB forced to the off state.

If, during the state where CLOCK signal input is provided, the ENABLE pin is set to 0 (low) and then is later restored to the 1 (high) state, the IC will resume operation with the excitation timing continued from before the point ENABLE was set to 0 (low).

[MODE (Excitation mode selection)]

MODE = 0 (low): 2-phase excitation

MODE = 1 (high): 1-2 phase excitation

See the timing charts for details on output operation in these modes.

Note: The state of the MODE input must not be changed during the 5μs period before and after the rising edge of the CLOCK input.

2. Allowable motor current operating range

The motor current (I_{OH}) must be held within the range corresponding to the area under the curve shown in figure 3. For example, if the operating substrate temperature Tc is 105°C, then I_{OH} must be held under I_{OH} = 2.2A, and in hold mode I_{OH} must be held under I_{OH} = 1.8A.

3. Thermal design

[Operating range in which a heat sink is not used]

This section discusses the safe operating range when no heat sink is used.

In the maximum ratings specifications, Tc max is specified to be 105°C, and when mounted in an actual end product system, the Tc max value must never be exceeded during operation. Tc can be expressed by formula (A) below, and thus the range for ΔTc must be stipulated so that Tc is always under 105°C.

$$Tc = Ta + \Delta Tc \quad (A)$$

Ta: Hybrid IC (HIC) ambient temperature, ΔTc: Temperature increase across the aluminum substrate

As shown in figure 5, the value of ΔTc increases as the hybrid IC internal average power dissipation P_D increases. As shown in figure 4, P_D increases with the motor current. Here we describe the actual P_D calculation using the example shown in the motor current timing chart in figure 2.

Since there are periods when current flows and periods when the current is off during actual motor operation, P_D cannot be determined from the data presented in figure 4. Therefore, we calculate P_D assuming that actual motor operation consists of repetitions of the operation shown in figure 2.

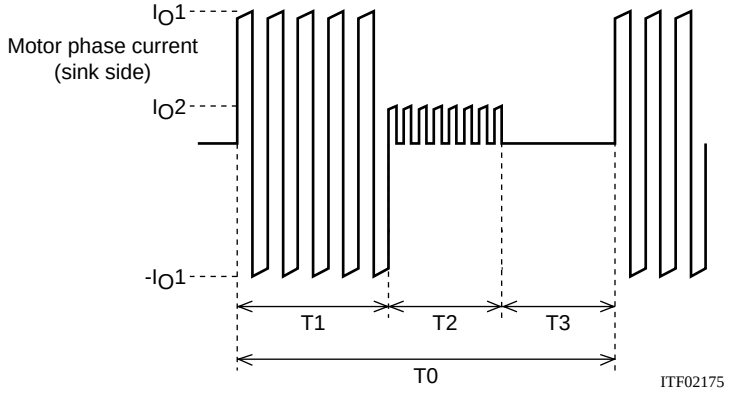


Figure 2 Motor Current Timing

T1: Motor rotation operation time
T2: Motor hold operation time
T3: Motor current off time
T2 may be reduced, depending on the application.
T0: Single repeated motor operating cycle
I_O1 and I_O2: Motor current peak values
Due to the structure of motor windings, the phase current is a positive and negative current with a pulse form.
Note that figure 2 presents the concepts here, and that the on/off duty of the actual signals will differ.

The hybrid IC (HIC) internal average power dissipation P_D can be calculated from the following formula.

$$P_D = (T1 \times P1 + T2 \times P2 + T3 \times 0) \div T0 \quad \cdots\cdots (I)$$

(Here, P1 is the P_D for I_O1 and P2 is the P_D for I_O2)

If the value calculated in formula (I) above is under 1.5W, then from figure 5 we see that operation is allowed up to an ambient temperature Ta of 60°C.

While the operating range when a heat sink is not used can be determined from formula (I) above, figure 4 is merely a single example of one operating mode for a single motor.
For example, while figure 4 shows a 2-phase excitation motor, if 1-2 phase excitation is used with a 500Hz clock frequency, the drive will be turned off for 25% of the time and the dissipation P_D will be reduced to 75% of that in figure 4.
It is extremely difficult for calculate the internal average power dissipation P_D for all possible end product conditions. After performing the above rough calculations, always install the hybrid IC (HIC) in an actual end product and verify that the substrate temperature Tc does not rise above 105°C.

[Operating range in which a heat sink is used]

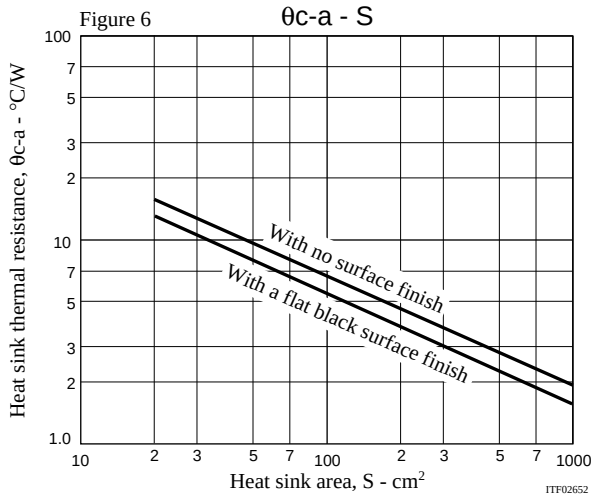
Although a heat sink is attached to lower Tc if the hybrid IC (HIC) internal average power dissipation P_D increases, the resulting size can be found using the value of θc-a in Equation (II) below and the graph depicted in Figure 6.

$$\theta c\text{-}a = (Tc\ max - Ta) \div P_D \quad \text{---------- (II)}$$

Tc max: Maximum operating substrate temperature =105°C
Ta: HIC ambient temperature

Although a heat sink can be designed based on equations (I) and (II) above, be sure to mount the HIC in a set and confirm that the substrate temperature, Tc, is 105°C or less.
The average HIC power loss, P_D, described above represents the power loss when there is no avalanche operation. To add the loss during avalanche operations, be sure to add Equation (2), "Allowable STK672-3** Avalanche Energy Value", to P_D.

Figure 6



4. STK672-340-E Allowable Avalanche Energy Value

[Allowable Range in Avalanche Mode]

When driving a 2-phase stepping motor with constant current chopping using an STK672-3** Series hybrid IC, the waveforms shown in Figure 7 below result for the output current, I_D, and voltage, V_{DS}.

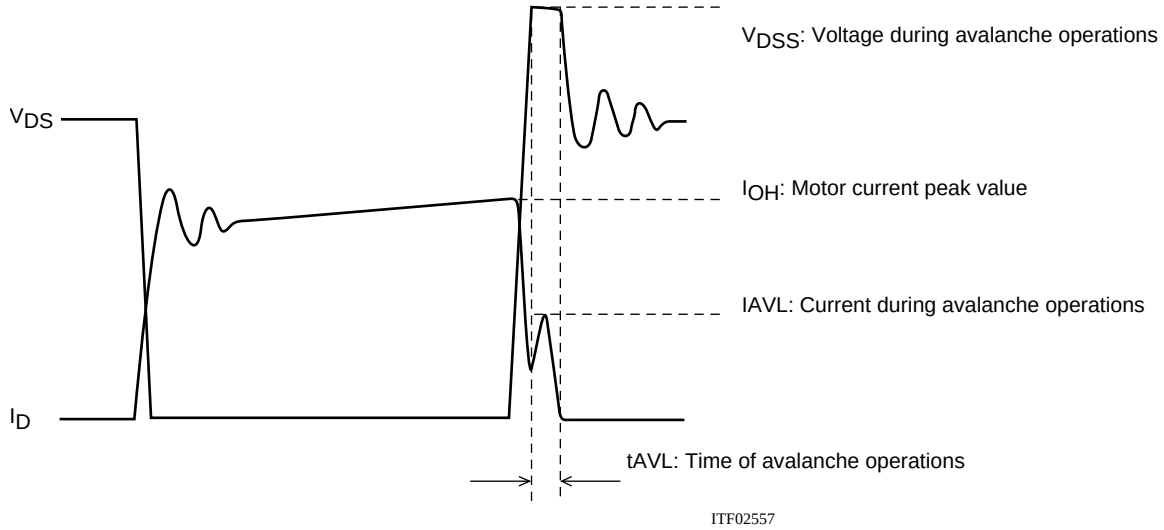


Figure 7 Output Current, I_D, and Voltage, V_{DS}, Waveforms 1 of the STK672-3** Series when Driving a 2-Phase Stepping Motor with Constant Current Chopping

When operations of the MOSFET built into STK672-3** Series ICs is turned off for constant current chopping, the I_D signal falls like the waveform shown in the figure above. At this time, the output voltage, V_{DS}, suddenly rises due to electromagnetic induction generated by the motor coil.

In the case of voltage that rises suddenly, voltage is restricted by the MOSFET V_{DSS}. Voltage restriction by V_{DSS} results in a MOSFET avalanche. During avalanche operations, I_D flows and the instantaneous energy at this time, EAVL1, is represented by Equation (1).

$$EAVL1=V_{DSS}\times IAVL\times 0.5\times tAVL \quad \text{---------- (1)}$$

V_{DSS}: V units, IAVL: A units, tAVL: sec units

The coefficient 0.5 in Equation (1) is a constant required to convert the IAVL triangle wave to a square wave.

During STK672-3** Series operations, the waveforms in the figure above repeat due to the constant current chopping operation. The allowable avalanche energy, EAVL, is therefore represented by Equation (2) used to find the average power loss, PAVL, during avalanche mode multiplied by the chopping frequency in Equation (1).

$$PAVL=V_{DSS}\times IAVL\times 0.5\times tAVL\times fc \quad \text{---------- (2)}$$

fc: Hz units (fc is set to the PWM frequency of 50kHz.)

For V_{DSS}, IAVL, and tAVL, be sure to actually operate the STK672-3** Series and substitute values when operations are observed using an oscilloscope.

Ex. If V_{DSS}=110V, IAVL=1A, tAVL=0.2μs when using a STK672-340-E driver, the result is:

$PAVL=110\times 1\times 0.5\times 0.2\times 10^{-6}\times 50\times 10^{3}=0.55W$

V_{DSS}=110V is a value actually measured using an oscilloscope.

The allowable loss range for the allowable avalanche energy value, PAVL, is shown in the graph in Figure 9. When examining the avalanche energy, be sure to actually drive a motor and observe the I_D, V_{DSS}, and tAVL waveforms during operation, and then check that the result of calculating Equation (2) falls within the allowable range for avalanche operations.

[I_D and V_{DSS} Operating Waveforms in Non-avalanche Mode]

Although the waveforms during avalanche mode are given in Figure 7, sometimes an avalanche does not result during actual operations.

Factors causing avalanche are listed below.

- Poor coupling of the motor's phase coils (electromagnetic coupling of A phase and AB phase, B phase and BB phase).
- Increase in the lead inductance of the harness caused by the circuit pattern of the P.C. board and motor.
- Increases in V_{DSS}, tAVL, and IAVL in Figure 7 due to an increase in the supply voltage from 24V to 36V.

If the factors above are negligible, the waveforms shown in Figure 7 become waveforms without avalanche as shown in Figure 8.

Under operations shown in Figure 8, avalanche does not occur and there is no need to consider the allowable loss range of PAVL shown in Figure 9.

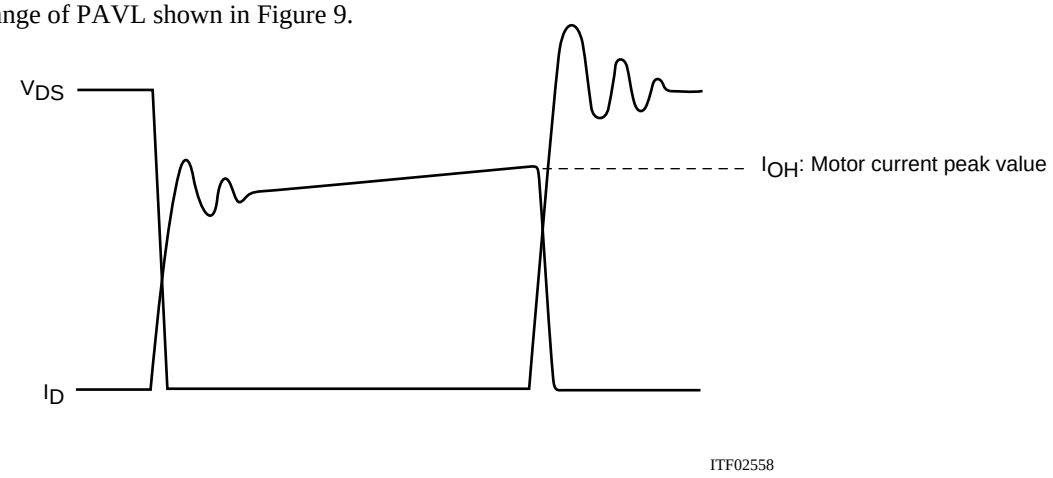
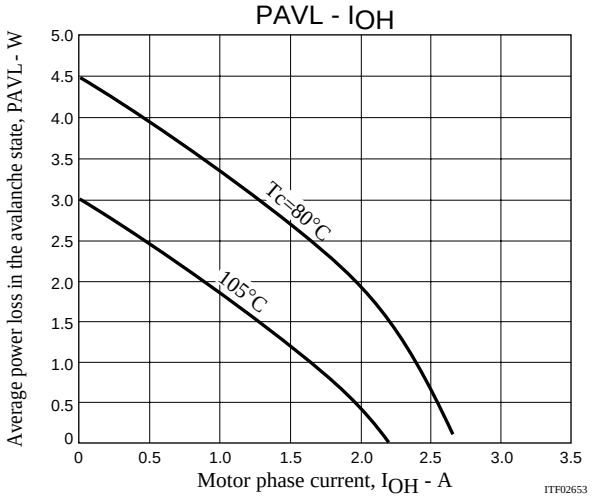


Figure 8 Output Current, I_D, and Voltage, V_{DS}, Waveforms 2 of the STK672-3** Series when Driving a 2-Phase Stepping Motor with Constant Current Chopping

Figure 9 Allowable Loss Range, PAVL-I_{OH} During STK672-340-E Avalanche Operations



Note:

The operating conditions given above represent a loss when driving a 2-phase stepping motor with constant current chopping.

Because it is possible to apply 3.0W or more at I_{OH}=0A, be sure to avoid using the MOSFET body diode that is used to drive the motor as a zener diode.

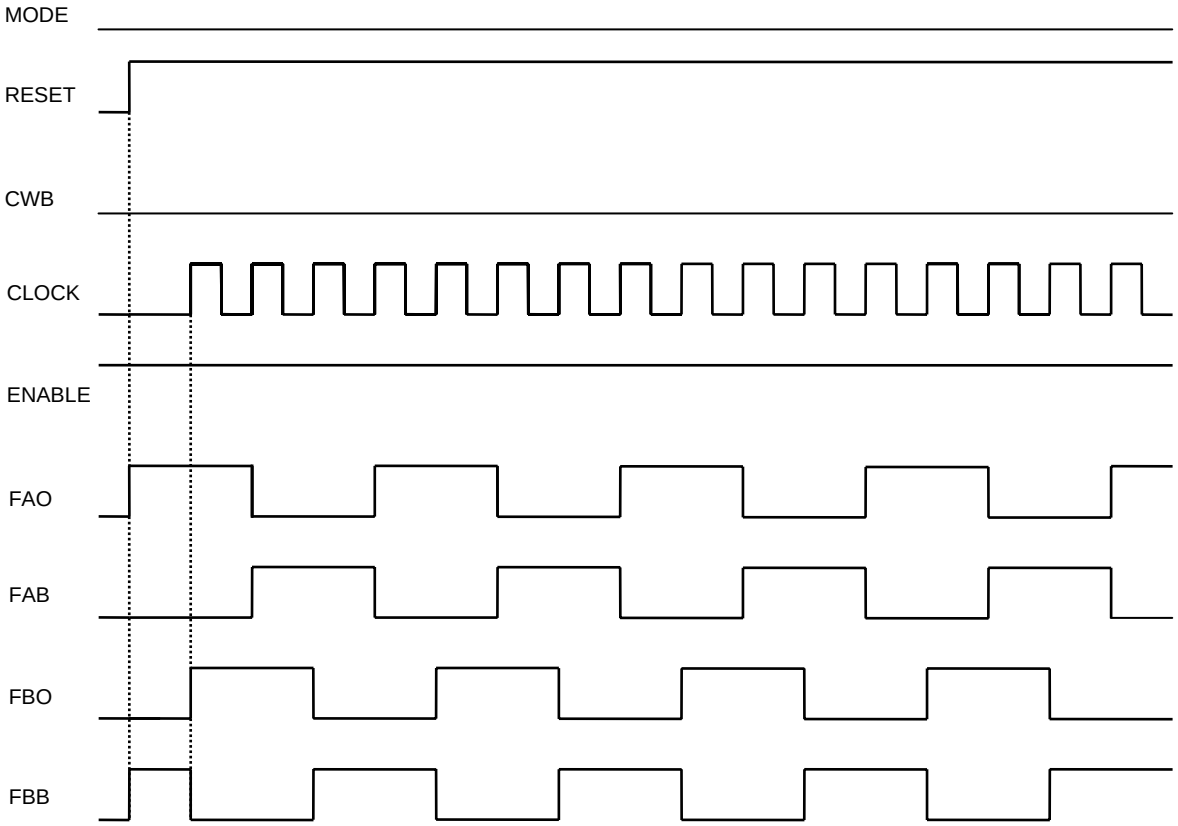
[Smoke Emission Precuations]

If any of the output pins 2, 3, 4, and 5 is held open, the electrical stress onto the driver due to the inductive energy accumulated in the motor could cause short-circuit followed by permanent damage to the internal MOSFET.

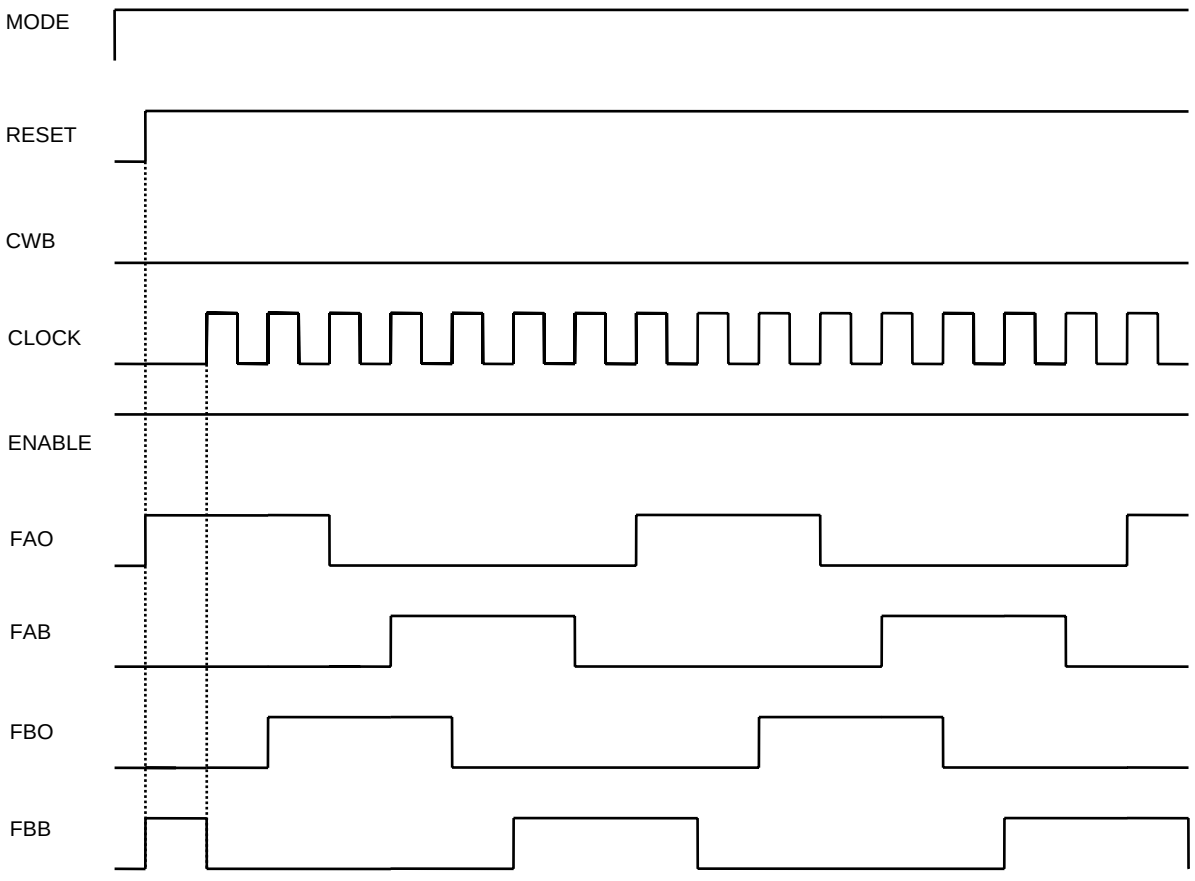
As a result, the STK672-340-E may give rise to emit smoke.

Timing Charts

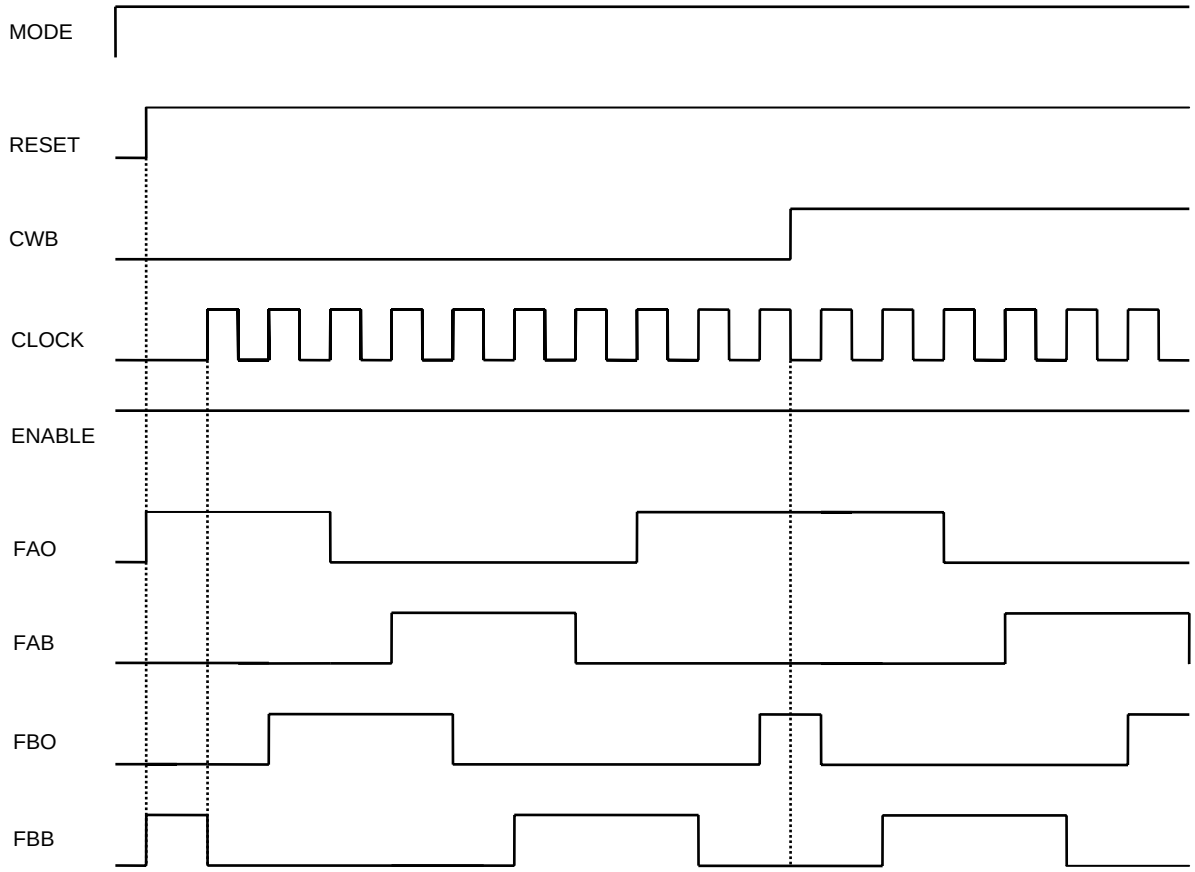
2-phase excitation



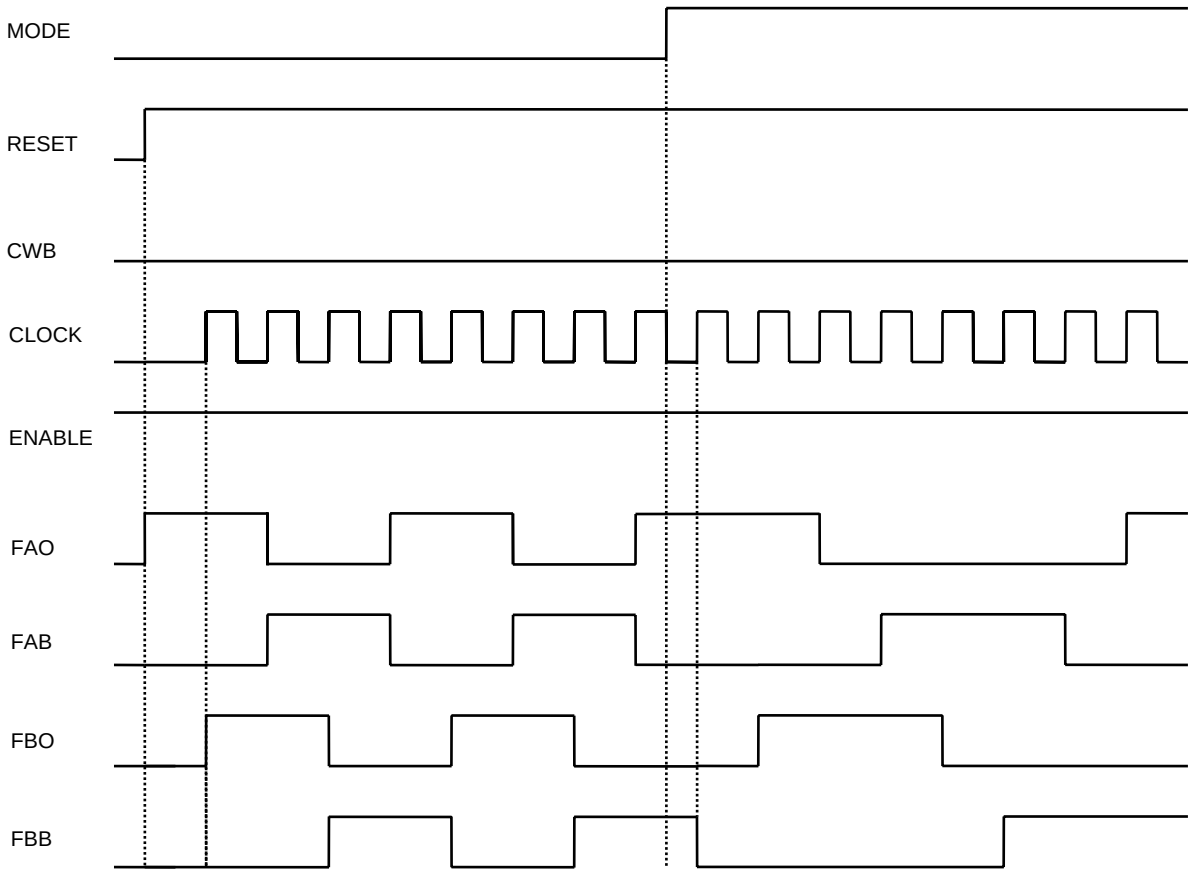
1-2 phase excitation



1-2 phase excitation (CWB)



Switching from 2-phase to 1-2 phase excitation



1-2 phase excitation (ENABLE)

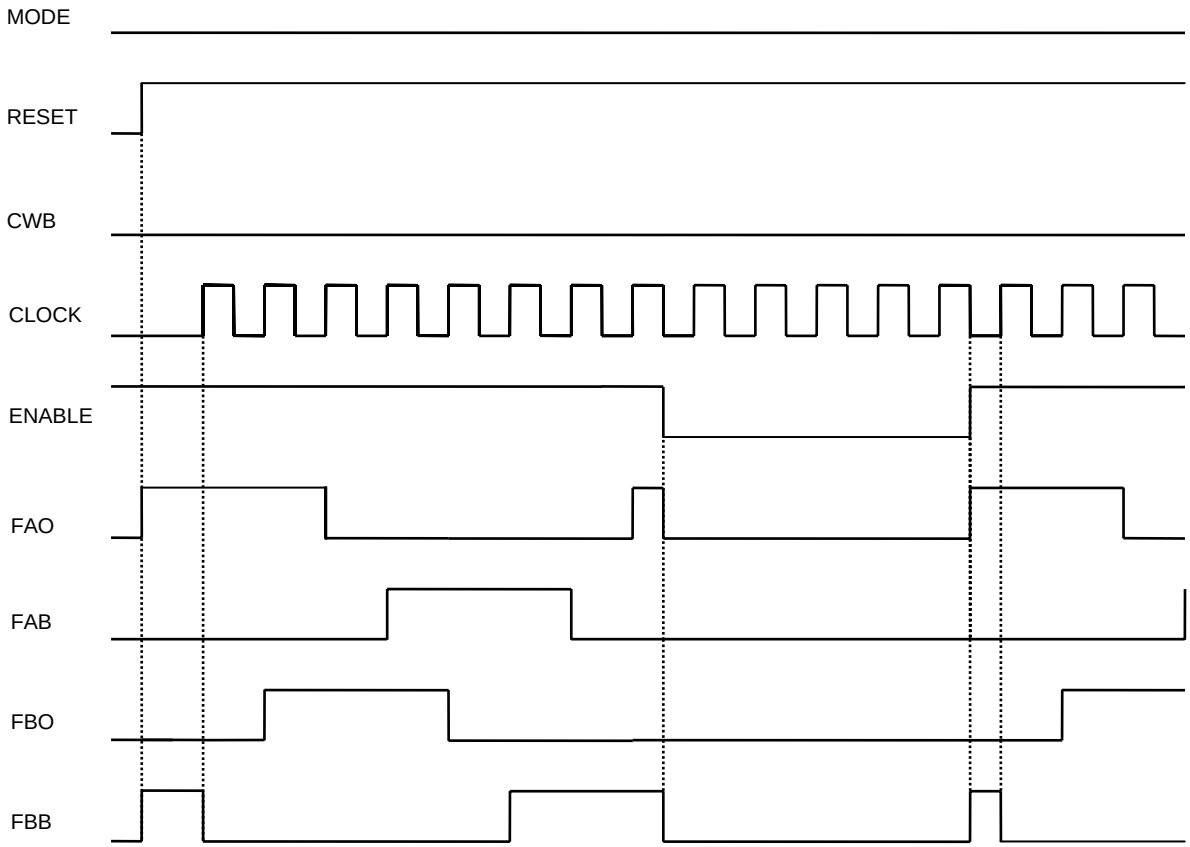


Figure 3 I_{OH} - Tc

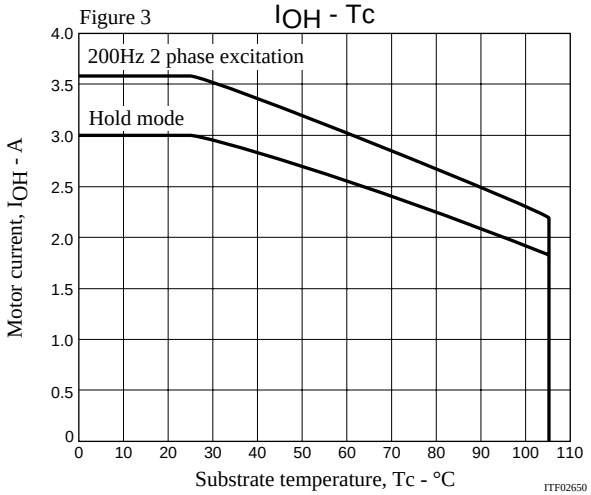


Figure 4 P_D - I_{OH}

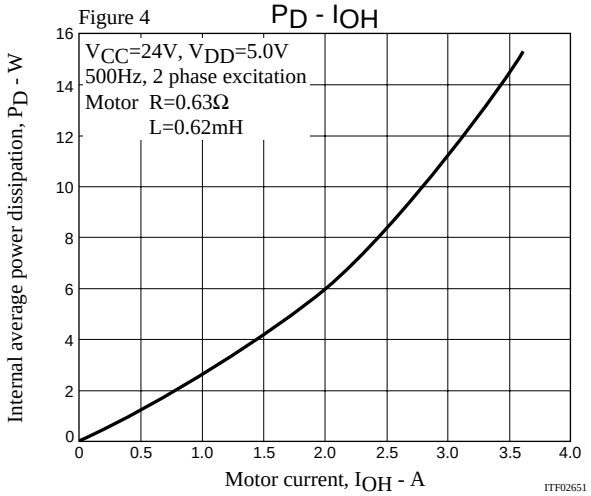


Figure 5 ΔTc - P_D