

TPS53647 4-Phase, D-CAP+, Step-Down, Buck Controller with NVM and PMBus™ Interface for ASIC Power and High-Current Point-of-Load

1 Features

- 8-bit Selectable BOOT Voltage via Pinstrap or NVM: 0.5 V to 2.5 V (down to 5-mV Step)
- 1-, 2-, 3-, or 4- Phase Operation
- PMBus™ System Interface for Telemetry of Voltage, Current, Power, Temperature, and Fault Conditions
- 1.8-V and 3.3-V PMBus Bias Compatible
- Fault Reporting: Output Voltage, Output Current, and Temperature
- Configurable with Non-Volatile Memory (NVM) or Resistor Pinstrap
- 16 Levels of Programmable OCP with Pinstrap or NVM
- Fast Transient with DCAP+™ Control
- Optimized Efficiency at Light and Heavy Loads
- Support Pre-Bias Startup
- Phase Current Imbalance Detection and Reporting
- 8 Independent Levels of Overshoot Reduction (OSR) and Undershoot Reduction (USR)
- Driverless Configuration for Efficient High-Frequency Switching
- Fully Compatible with CSD95372BQ5MC NexFET™ Power Stage
- Accurate, Adjustable Voltage Positioning
- 300-kHz to 1-MHz Frequency Selections with Closed-loop Frequency Control
- Patented AutoBalance™ Phase Balancing
- Uses TI's [Fusion Digital Power Designer GUI](#)
- Dynamic Phase Shedding with Programmable Current Threshold
- Conversion Voltage Range: 4.5 V to 17 V
- Small, 6 mm x 6 mm, 40-Pin, QFN, PowerPAD™ Package

2 Applications

- Application-Specific Integrated Circuit (ASIC) Power in Communications Equipment
- High Density Power Solutions
- Server Power
- Smart Power Systems

3 Description

The TPS53647 is a high-current, multi-phase, step-down controller. The device offers built-in non-volatile memory (NVM) and PMBus interface. It is compatible with the NexFET power stages (CSD95372BQ5MC). The TPS53647 provides 8-bit BOOT voltage selection covering output voltage from 0.5 V to 2.5 V, with steps as small as 5 mV, which is ideal for high current application with accurate output voltage setting. Advanced control features such as D-CAP+ architecture with undershoot reduction (USR) and overshoot reduction (OSR) provide fast transient response, lowest output capacitance, and high efficiency. The TPS53647 also provides novel phase interleaving strategy and dynamic phase shedding for efficiency improvement at light loads. In addition, the TPS53647 supports the PMBus communication interface with systems for telemetry of voltage, current, power, temperature, and fault conditions. Some of the configurations can be programmed by pinstrap or PMBus and stored in non-volatile memory to minimize the external component count.

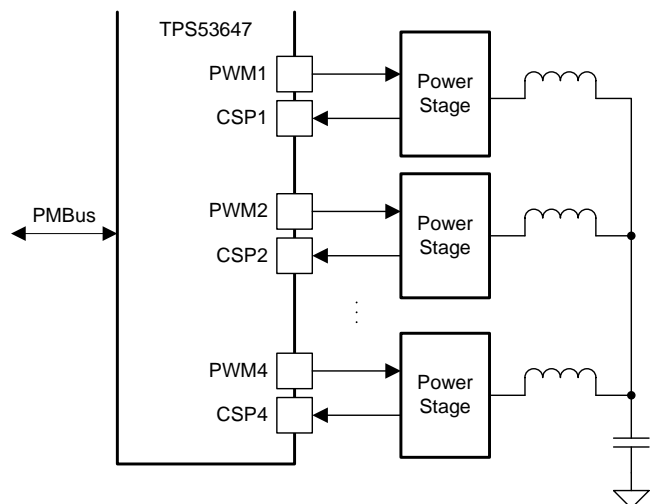
The TPS53647 is offered in a space saving, thermally enhanced 40-pin QFN package and is rated to operate from -40°C to 125°C .

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|----------|-------------------|
| TPS53647 | QFN (40) | 6.00 mm x 6.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

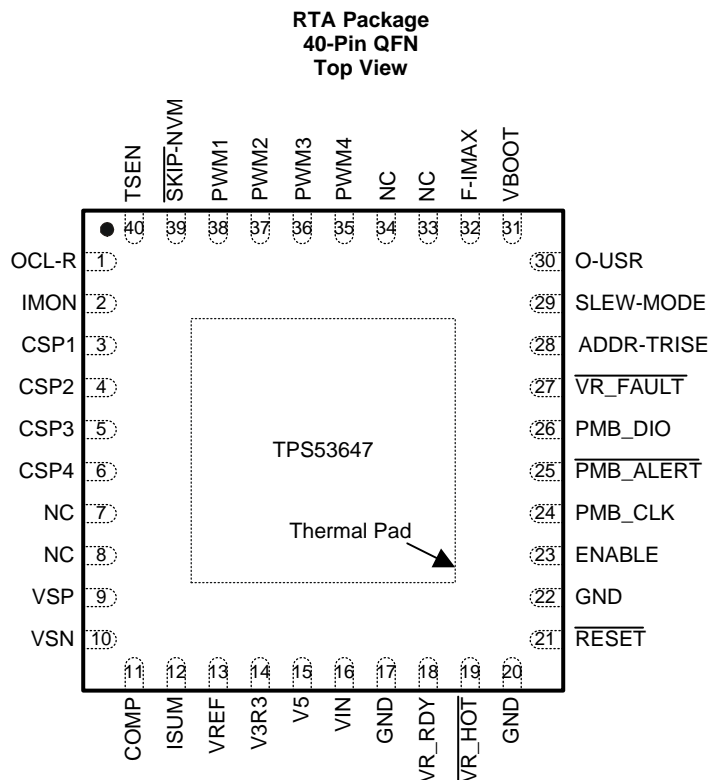


4 Revision History

| Changes from Revision A (September 2016) to Revision B | Page |
|--|------|
| • Updated V3R3 LDO section | 18 |
| • Added temperature default value VR_HOT and VR_FAULT Indication section | 30 |
| • Corrected factory default value of VOUT_OV_FAULT_RESPONSE command in Table 7 | 38 |
| • Corrected factory default value of VIN_OV_FAULT_LIMIT command in Table 7 | 38 |
| • Corrected factory default value of MFR_ID command in Table 7 | 39 |
| • Corrected factory default value of MFR_SPECIFIC_44 command in Table 7 | 40 |

| Changes from Original (June 2015) to Revision A | Page |
|--|------|
| • Updated the $V_{\text{ADDR-TRISE}}$ condition of the PADDR specification in the Electrical Characteristics table from "1.647 V" to "1.615 V" | 8 |
| • Updated the $V_{\text{OCL-R}}$ condition of the I_{OCLX} specification in the Electrical Characteristics table from "0.8 V" to "0.85 V" | 9 |
| • Updated the $V_{\text{OCL-R}}$ condition of the I_{OCLX} specification in the Electrical Characteristics table from "1.0 V" to "0.95 V" | 9 |
| • Updated the $V_{\text{OCL-R}}$ condition of the V_{RAMP} specification in the Electrical Characteristics table to " ± 50 mV" | 9 |
| • Updated the $V_{\text{SLEW-MODE}}$ condition of the V_{MODE} specification in the Electrical Characteristics table from "1.647 V with ± 20 mV tolerance" to "1.615 V with ± 10 mV tolerance" | 11 |
| • Updated the $V_{\text{O-USR}}$ condition of the V_{USR} specification in the Electrical Characteristics table from " $V_{\text{O-USR}} \geq 1.55$ V (USR OFF)" to " $1.55 \text{ V} \leq V_{\text{O-USR}} \leq 1.6 \text{ V}$ " | 11 |
| • Updated the V_{BOOT} ($B_7B_6B_5B_4$) condition of the V_{BOOT} specification in the Electrical Characteristics table from "1.647 V with ± 20 mV tolerance" to "1.615 V with ± 10 mV tolerance" | 12 |
| • Clarified the READ_VIN (88h) section..... | 69 |
| • Corrected typographical error in READ_VOUT (8Bh) section..... | 71 |
| • Clarified the READ_IOUT (8Ch) section | 71 |
| • Clarified the READ_TEMPERATURE_1 (8Dh) section..... | 72 |
| • Clarified the READ_POUT (96h) section..... | 73 |
| • Clarified the READ_POUT (96h) section..... | 74 |
| • Clarified the MFR_SPECIFIC_04 (Read VOUT) (D4h) section | 78 |
| • Updated the MFR_SPECIFIC_14 (Ramp Height) (DEh) section | 86 |
| • Clarified the Set the Load-Line section | 97 |
| • Updated Table 79 | 97 |
| • Updated Table 82 | 98 |
| • Added Receiving Notification of Documentation Updates section | 114 |
| • Added Community Resources section | 114 |

5 Pin Configuration and Functions



NC = No internal connection

Pin Functions

| PIN | | I/O ⁽¹⁾ | DESCRIPTION |
|------------|-----|--------------------|--|
| NAME | NO. | | |
| ADDR-TRISE | 28 | I | Voltage divider to VREF pin. A resistor ($R_{ADDR-TRISE}$) connected between this pin and GND sets the 3-bits. Bit 2 and bit 1 set the rise slew rate. Bit 0 Selects the LSB of BOOT voltage. The voltage ($V_{ADDR-TRISE}$) sets 4 bits PMBus address. The device latches these settings when V3R3 powers up. |
| COMP | 11 | O | Output of the g_m error amplifier. Resistors and capacitors connected between this pin and the VREF pin set the compensation. |
| CSP1 | 3 | I | Positive current sense inputs. Connect to the IOUT pin of TI smart power stages (ex: CSD95372BQ5MC). Tie CSP4, CSP3, or CSP2 to the V3R3 pin according to Table 3 to disable the corresponding phase. |
| CSP2 | 4 | | |
| CSP3 | 5 | | |
| CSP4 | 6 | | |
| ENABLE | 23 | I | VR enable. 1-V I/O level; 100-ns debounce. |
| F-IMAX | 32 | I | Voltage divider to VREF pin. A resistor (R_{F-IMAX}) connected between this pin and GND sets the operating frequency of the controller. The voltage level (V_{F-IMAX}) sets the maximum operating current of the converter. The IMAX value is an 8-bit A/D where $V_{F-IMAX} = V_{VREF} \times I_{MAX} / 255$. Both are latched at V3R3 power-up. |
| GND | 17 | G | Ground pin. |
| GND | 20 | G | Connect these pins to GND. Note this is not IC ground pin. |
| | 22 | | |

(1) I = Input, O = Output, P = Power, I/O = Bi-directional, GND = ground

Pin Functions (continued)

| PIN | | I/O ⁽¹⁾ | DESCRIPTION |
|-------------------------|-----|--------------------|---|
| NAME | NO. | | |
| IMON | 2 | O | Analog current monitor output. $V_{IMON} = \frac{I_O \times 5m\Omega \times R_{IMON}}{35k\Omega}$ |
| ISUM | 12 | O | A resistor (R_{ISUM}) connected between this pin and VREF pin determines the droop. $V_{ISUM} = \frac{I_O \times 5m\Omega \times g_{M(isum)} \times R_{ISUM}}{n} + V_{REF}$ (where n is the number of phases) |
| NC | 7 | — | No connection. Leave the pin open or pull up to V3R3 pin. |
| | 8 | | |
| | 33 | — | No connection. |
| | 34 | | |
| OCL-R | 1 | I | A resistor (R_{OCL-R}) connected between this pin and GND and the voltage level (V_{OCL-R}) select 1 of 16 OCL levels (per phase current-limit). V_{OCL-R} also sets one of four RAMP levels. The device latches these settings when V3R3 powers up. |
| O-USR | 30 | I | Voltage divider to VREF pin. A resistor (R_{O-USR}) connected between this pin and GND selects one of seven OSR thresholds or OFF. The voltage level (V_{O-USR}) sets one of seven USR levels or OFF. The device latches these settings when V3R3 powers up. |
| $\overline{PMB_ALERT}$ | 25 | O | I ² C PMBus interrupt line. Open drain. 3.3-V and 1.8-V logic level. |
| PMB_CLK | 24 | I | I ² C PMBus clock. 3.3-V and 1.8-V logic level. |
| PMB_DIO | 26 | I/O | I ² C PMBus digital I/O line. 3.3-V and 1.8-V logic level. |
| PWM1 | 38 | O | PWM signals for each phase |
| PWM2 | 37 | | |
| PWM3 | 36 | | |
| PWM4 | 35 | | |
| \overline{RESET} | 21 | I | Reset pin. If this pin is low for more than 1000 ns, the controller pulls the output voltage to the V_{BOOT} level. |
| $\overline{SKIP-NVM}$ | 39 | O | A resistor ($R_{\overline{SKIP-NVM}}$) connected between this pin and GND sets either pinstrap or NVM configuration mode. This pin can also connect to the FCCM pin of TI smart power stages (ex: CSD95372BQ5MC) for SKIP or FCCM operation. |
| SLEW-MODE | 29 | I | Voltage divider to VREF pin. A resistor ($R_{SLEW-MODE}$) connected between this pin and GND sets 8 slew rates. The voltage level ($V_{SLEW-MODE}$) sets 4-bit operation modes. Bit 7 for DAC mode (1 for VR12.0; 0 for VR12.5). Bit 6 for the 4-phase interleaving mode (1 for 1/3 and 2/4 two phase interleaving; 0 for 4 phase interleaving individually). Bit 4 for enabling dynamic phase add or drop (1 for enable; 0 for disable). Bit 3 sets zero load-line (1 for zero load-line; 0 for non-zero load-line) The device latches these settings when V3R3 powers up. |
| TSEN | 40 | I | Connect to the TAO/FAULT pin of TI smart power stages (ex: CSD95372BQ5MC) to sense the highest temperature of the power stages and to sense the fault signal from the power stages. |
| V3R3 | 14 | O | 3.3-V LDO output. Bypass this pin to GND with a ceramic capacitor with a value of 1- μ F or larger. |
| V5 | 15 | P | 5-V power input. Bypass this pin to GND with a ceramic capacitor with a value of 1- μ F or larger. This pin is used to power all internal analog circuits. |
| VBOOT | 31 | I | Voltage divider to VREF pin. A resistor (R_{VBOOT}) connected between this pin and GND sets 3 bits (B[3:1]). The voltage level (V_{VBOOT}) sets 4 bits (B[7:4]). The total 7 bits set 7 of 8 bits of VID of boot voltage (B[7:1]). The device latches these settings when V3R3 powers up. |
| VIN | 16 | P | Input voltage supply. This pin is also used for input voltage sensing for on-time control and input undervoltage lockout (UVLO). |
| VR_RDY | 18 | O | Power good open-drain output for the controller. This pin is typically pulled up to V3R3 pin through a resistor with a value of 3-k Ω or larger. |
| $\overline{VR_FAULT}$ | 27 | O | VR fault indicator (open-drain). The failures include shorts of the high-side FETs, over temperature, output overvoltage, and overcurrent conditions of the input. The fault signal should be used on the platform to remove the power source either by firing a shunting SCR to blow a fuse or by turning off the AC power supply. When the failure occurs, the $\overline{VR_FAULT}$ pin is LOW. This pin is typically pulled up to V3R3 pin through a resistor with a value of 3-k Ω or larger. Leave this pin floating if not used. |
| $\overline{VR_HOT}$ | 19 | O | Thermal flag open drain output. Active low. This pin is typically pulled up to V3R3 pin through a resistor with a value of 3-k Ω or larger. Leave this pin floating if not used. |

Pin Functions (continued)

| PIN | | I/O ⁽¹⁾ | DESCRIPTION |
|-------------|-----|--------------------|--|
| NAME | NO. | | |
| VREF | 13 | O | 1.7-V, 500- μ A, LDO reference voltage. Bypass this pin to GND with a ceramic capacitor with a value of 0.33 μ F. Connect the VREF pin to the REFIN pin of TI smart power stages (ex: CSD95372BQ5MC) as the current-sense reference voltage. |
| VSN | 10 | I | Negative input of the remote voltage sense amplifier. Connect this pin directly to the GND of the load. |
| VSP | 9 | I | Positive input of the remote voltage sense amplifier. Connect this pin directly to the load. |
| Thermal Pad | | GND | Thermal pad. Connect the thermal pad to the ground plane with multiple vias. |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾ ⁽²⁾

| | | MIN | MAX | UNIT |
|--|--|------|-----|------|
| Input Voltage | VIN | -0.3 | 19 | V |
| | V5 | -0.3 | 6 | |
| | ADDR-TRISE, CSP1, CSP2, CSP3, CSP4, ENABLE, F-IMAX, OCL-R, O-USR, PMB_CLK, PMB_DIO, RESET, SLEW-MODE, VBOOT, VSP | -0.3 | 3.6 | |
| | TSEN | -0.3 | 6 | |
| | GND, VSN | -0.3 | 0.3 | |
| Output Voltage | VREF | -0.3 | 1.8 | V |
| | IMON, ISUM, <u>PMB_ALERT</u> , PWM1, PWM2, PWM3, PWM4, SKIP-NVM, V3R3, VR_RDY, VR_FAULT, VR_HOT | -0.3 | 3.6 | |
| | COMP | -0.3 | 6 | |
| Operating Junction Temperature, T _J | | -40 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the network ground terminal GND unless otherwise noted.

6.2 Handling Ratings

| | | MIN | MAX | UNIT | |
|--------------------|---------------------------|--|------|------|----|
| T _{stg} | Storage temperature range | -55 | 150 | °C | |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | -2.5 | 2.5 | kV |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | -1.5 | 1.5 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT | |
|----------------|--------------------------------|---|------|-----|-------------------|---|
| V _I | Input voltage | VIN | 4.5 | 12 | 17 | V |
| | | TSEN | -0.1 | | 5.5 | |
| | | V5 | 4.5 | 5 | 5.5 | |
| | | ADDR-TRISE, F-IMAX, OCL-R, O-USR, SLEW-MODE, VBOOT | 0.1 | | V _{VREF} | |
| | | CSP1, CSP2, CSP3, CSP4, VSP | -0.1 | | 2.5 | |
| | | ENABLE, PMB_CLK, PMB_DIO | -0.1 | | 3.5 | |
| | | GND, VSN | -0.1 | | 0.1 | |
| V _O | Output voltage | VREF | -0.1 | | 1.72 | V |
| | | V3R3 | -0.1 | 3.3 | 3.5 | |
| | | IMON, ISUM, $\overline{\text{PMB_ALERT}}$, PWM1, PWM2, PWM3, PWM4, $\overline{\text{SKIP-NVM}}$, $\overline{\text{VR_RDY}}$, $\overline{\text{VR_FAULT}}$, $\overline{\text{VR_HOT}}$ | -0.1 | | 3.5 | |
| | | COMP | -0.1 | | 5.5 | |
| T _A | Operating free air temperature | -40 | | 125 | °C | |

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TPS53647 | UNIT |
|-------------------------------|--|-----------|------|
| | | RTA (QFN) | |
| | | 40 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 30.6 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 14.2 | |
| R _{θJB} | Junction-to-board thermal resistance | 6.9 | |
| ψ _{JT} | Junction-to-top characterization parameter | 0.2 | |
| ψ _{JB} | Junction-to-board characterization parameter | 6.8 | |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 1.8 | |

 (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com/lit/an/spra953).

6.5 Electrical Characteristics

over recommended free-air temperature range, $V_{VIN} = 12\text{ V}$, $V_{V5} = 5\text{ V}$, $V_{VSN} = \text{GND}$, $V_{VSP} = V_{OUT}$ (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---------------------------------------|---|-------|-----------------|-------|---------------|
| SUPPLY: CURRENTS, UVLO, AND POWER-ON RESET | | | | | | |
| I_{VIN} | VIN supply current, 4-phase active | $V_{VDAC} < V_{VSP} < V_{VDAC} + 100\text{ mV}$, ENABLE = HI | | | 115 | μA |
| I_{V5} | V5 supply current | PMBus Idle, ENABLE = HI | | 6.1 | 7 | mA |
| I_{VSSBY} | V5 standby current | ENABLE = LO | | 2 | 2.6 | mA |
| V_{V3R3} | V3R3 output voltage | $I_{V3R3} = 0\text{ A}$ | 3.2 | 3.3 | 3.4 | V |
| $V_{V3R3(\text{dropout})}$ | V3R3 load regulation | $I_{V3R3} = 5\text{ mA}$ | | | 100 | mV |
| $V_{V5UVLOH}$ | V5 UVLO OK threshold | Ramp up | 4.1 | 4.25 | 4.5 | V |
| $V_{V5UVLOL}$ | V5 UVLO fault threshold | Ramp down | 3.95 | 4.05 | 4.25 | V |
| $V_{HYS(V5)}$ | V5 UVLO hysteresis | Hysteresis | 0.15 | 0.23 | 0.3 | V |
| $V_{VINUVLO}$ | VIN UVLO voltage | MFR_SPEC_16[1:0] = 00 | 4.2 | 4.5 | 4.7 | V |
| | | MFR_SPEC_16[1:0] = 01 | 6.9 | 7.25 | 7.45 | |
| | | MFR_SPEC_16[1:0] = 10 | 8.6 | 9.0 | 9.25 | |
| | | MFR_SPEC_16[1:0] = 11 | 9.8 | 10.3 | 10.7 | |
| $V_{HYS(VIN)}$ | VIN UVLO hysteresis voltage | Hysteresis voltage | | 1 | | V |
| REFERENCES: DAC AND VREF | | | | | | |
| V_{VIDSTP} | VID Step size | VR12.5: Change VID0 HI to LO to HI | | 10 | | mV |
| | | VR12.0: Change VID0 HI to LO to HI | | 5 | | mV |
| V_{DAC1} | Closed Loop VSP tolerance | VR12.0: $0.61\text{ V} \leq V_{VSP} \leq 0.995\text{ V}$, $I_{OUT} = 0\text{ A}$, $0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ | -6 | | 6.5 | mV |
| V_{DAC2} | Closed Loop VSP tolerance | VR12.0: $1\text{ V} \leq V_{VSP} \leq 1.52\text{ V}$, $I_{OUT} = 0\text{ A}$, $0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ | -0.6 | | 0.6 | % |
| V_{DAC3} | Closed Loop VSP tolerance | VR12.5: $1.50\text{ V} \leq V_{VSP} \leq 2.50\text{ V}$, $I_{OUT} = 0\text{ A}$, $0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ | -1 | | 1 | % |
| V_{DAC4} | Closed Loop VSP tolerance | VR12.0: $0.61\text{ V} \leq V_{VSP} \leq 0.995\text{ V}$, $I_{OUT} = 0\text{ A}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ | -8 | | 8 | mV |
| V_{DAC5} | Closed Loop VSP tolerance | VR12.0: $1.0\text{ V} \leq V_{VSP} \leq 1.52\text{ V}$, $I_{OUT} = 0\text{ A}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ | -0.8 | | 0.8 | % |
| V_{DAC6} | Closed Loop VSP tolerance | VR12.5: $1.50\text{ V} \leq V_{VSP} \leq 2.50\text{ V}$, $I_{OUT} = 0\text{ A}$, $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ | -1.1 | | 1.0 | % |
| V_{VREF} | VREF output | $4.5 \leq V_{V5} \leq 5.5\text{ V}$, $I_{VREF} = 0\text{ A}$ | 1.685 | 1.70 | 1.717 | V |
| $V_{VREFSRC}$ | VREF output source | $I_{VREF} = 0\text{ to }500\text{ }\mu\text{A}$ | -4 | -1 | | mV |
| $V_{VREFSNK}$ | VREF output sink | $I_{VREF} = -500\text{ to }0\text{ }\mu\text{A}$ | | 1 | 4 | mV |
| CURRENT SENSE: AMPLIFIER AND PHASE BALANCING | | | | | | |
| G_{CSINT} | Internal current sense gain | Gain from (CSPx – VREF) to PWM comparator | | 1.0 | | V/V |
| COMPENSATOR: VOLTAGE POSITIONING AND AMPLIFIER | | | | | | |
| $g_{M(\text{isum})}$ | ISUM amplifier transconductance | $V_{VSP} = 1.7\text{ V}$ | | 500 | | μS |
| $g_{M(\text{comp})}$ | COMP amplifier transconductance | $V_{VSP} = 1.7\text{ V}$ | | 1000 | | μS |
| $V_{CCLAMPN}$ | COMP amplifier negative clamp voltage | $(V_{VREF} - V_{COMP})$ | | $V_{RAMP} + 20$ | | mV |
| $V_{CCLAMP P}$ | COMP amplifier positive clamp voltage | $(V_{COMP} - V_{VREF})$ | 2.1 | 2.2 | 2.3 | V |
| VOLTAGE SENSE: VSP AND VSN | | | | | | |
| I_{VSP} | VSP input bias current | Not in fault, disable or UVLO, $V_{VSP} = V_{VDAC} = 2.3\text{ V}$, $V_{VSN} = 0\text{ V}$ | | | 300 | μA |
| I_{VSN} | VSN input bias current | Not in fault, disable or UVLO, $V_{VSP} = V_{VDAC} = 2.3\text{ V}$, $V_{VSN} = 0\text{ V}$ | -30 | -23 | | μA |
| R_{SFTSTP} | Transistor resistance | Connect to VSP | | 10 | | k Ω |
| LOGIC (RESET, VR_RDY, VR_FAULT, VR_HOT, AND ENABLE) INTERFACE PINS: I/O VOLTAGE AND CURRENT | | | | | | |
| R_{RPGDL} | Open drain pull-down resistance | VR_RDY, pulldown resistance at 0.31 V | | 36 | 50 | Ω |
| I_{VRTTLK} | Open drain leakage current | VR_HOT, VR_RDY, hi-Z leakage, apply 3.3 V in off state | -2 | 0.2 | 2 | μA |
| V_{RSTL} | RESET logic low | RESET Pin | | | 0.8 | V |
| V_{RSTH} | RESET logic high | RESET Pin | 1.2 | | | V |
| $T_{RSTTDLY}$ | RESET Delay Time | | | 1 | | μs |
| V_{ENL} | ENABLE logic low | | | | 0.3 | V |
| V_{ENH} | ENABLE logic high | | 0.8 | | | V |
| I_{ENH} | I/O 1.1- V leakage | Leakage current, $V_{ENABLE} = 1.1\text{ V}$ | | | 25 | μA |
| PMBUS INTERFACE PINS: I/O VOLTAGE AND CURRENT | | | | | | |
| V_{PMBL} | PMBus pins logic low | | | | 0.8 | V |
| V_{PMBH} | PMBus pins logic high | | 1.2 | | | V |
| I_{PMBL} | Logic low input current | $V_{PMBUS} = 0\text{ V}$ | -10 | | 10 | μA |
| I_{PMBH} | Logic high input current | $V_{PMBUS} = 1.8\text{ V}$ | -10 | | 10 | μA |

Electrical Characteristics (continued)

over recommended free-air temperature range, $V_{VIN} = 12\text{ V}$, $V_{V5} = 5\text{ V}$, $V_{VSN} = \text{GND}$, $V_{VSP} = V_{OUT}$ (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--|---|---|-----|---------|-----|------|--|
| ADDR-TRISE PIN: PMBUS ADDRESS, SOFT START RISE TIME SETTING | | | | | | | |
| SL _{RISE} | Soft start rise slew rate in terms of V_{OUT} slew rate | $R_{\text{ADDR-TRISE}} \leq 20\text{ k}\Omega$ or $R_{\text{ADDR-TRISE}} = 24\text{ k}\Omega$ or $\text{MFR_SPEC_12}<1:0> = 00\text{b}$ | | 1 | | | |
| | | $R_{\text{ADDR-TRISE}} = 30\text{ k}\Omega$ or $R_{\text{ADDR-TRISE}} = 39\text{ k}\Omega$ or $\text{MFR_SPEC_12}<1:0> = 01\text{b}$ | | 1/2 | | | |
| | | $R_{\text{ADDR-TRISE}} = 56\text{ k}\Omega$ or $R_{\text{ADDR-TRISE}} = 75\text{ k}\Omega$ or $\text{MFR_SPEC_12}<1:0> = 10\text{b}$ | | 1/4 | | | |
| | | $R_{\text{ADDR-TRISE}} = 100\text{ k}\Omega$ or $R_{\text{ADDR-TRISE}} = 150\text{ k}\Omega$ or $\text{MFR_SPEC_12}<1:0> = 11\text{b}$ | | 1/8 | | | |
| BOOT | BOOT voltage set (B0) | $R_{\text{ADDR-TRISE}} \leq 20\text{ k}\Omega$ or $R_{\text{ADDR-TRISE}} = 30\text{ k}\Omega$ or $R_{\text{ADDR-TRISE}} = 56\text{ k}\Omega$ or $R_{\text{ADDR-TRISE}} = 100\text{ k}\Omega$, or $\text{MFR_SPEC_11}[0] = 0\text{b}$ | | 0 | | | |
| | | $R_{\text{ADDR-TRISE}} = 24\text{ k}\Omega$ or $R_{\text{ADDR-TRISE}} = 39\text{ k}\Omega$ or $R_{\text{ADDR-TRISE}} = 75\text{ k}\Omega$ or $R_{\text{ADDR-TRISE}} = 150\text{ k}\Omega$, or $\text{MFR_SPEC_11}[0] = 1\text{b}$ | | 1 | | | |
| PADDR | PMBus address bits set ($11P_40P_2P_1P_0$) | $V_{\text{ADDR-TRISE}} \leq 0.053\text{ V}$ with $\pm 20\text{ mV}$ tolerance | | 1100000 | | | |
| | | $V_{\text{ADDR-TRISE}} = 0.159\text{ V}$ with $\pm 20\text{ mV}$ tolerance | | 1100001 | | | |
| | | $V_{\text{ADDR-TRISE}} = 0.266\text{ V}$ with $\pm 20\text{ mV}$ tolerance | | 1100010 | | | |
| | | $V_{\text{ADDR-TRISE}} = 0.372\text{ V}$ with $\pm 20\text{ mV}$ tolerance | | 1100011 | | | |
| | | $V_{\text{ADDR-TRISE}} = 0.478\text{ V}$ with $\pm 20\text{ mV}$ tolerance | | 1100100 | | | |
| | | $V_{\text{ADDR-TRISE}} = 0.584\text{ V}$ with $\pm 20\text{ mV}$ tolerance | | 1100101 | | | |
| | | $V_{\text{ADDR-TRISE}} = 0.691\text{ V}$ with $\pm 20\text{ mV}$ tolerance | | 1100110 | | | |
| | | $V_{\text{ADDR-TRISE}} = 0.797\text{ V}$ with $\pm 20\text{ mV}$ tolerance | | 1100111 | | | |
| | | $V_{\text{ADDR-TRISE}} = 0.903\text{ V}$ with $\pm 20\text{ mV}$ tolerance | | 1110000 | | | |
| | | $V_{\text{ADDR-TRISE}} = 1.009\text{ V}$ with $\pm 20\text{ mV}$ tolerance | | 1110001 | | | |
| | | $V_{\text{ADDR-TRISE}} = 1.116\text{ V}$ with $\pm 20\text{ mV}$ tolerance | | 1110010 | | | |
| | | $V_{\text{ADDR-TRISE}} = 1.222\text{ V}$ with $\pm 20\text{ mV}$ tolerance | | 1110011 | | | |
| | | $V_{\text{ADDR-TRISE}} = 1.328\text{ V}$ with $\pm 20\text{ mV}$ tolerance | | 1110100 | | | |
| | | $V_{\text{ADDR-TRISE}} = 1.434\text{ V}$ with $\pm 20\text{ mV}$ tolerance | | 1110101 | | | |
| $V_{\text{ADDR-TRISE}} = 1.541\text{ V}$ with $\pm 20\text{ mV}$ tolerance | | 1110110 | | | | | |
| $V_{\text{ADDR-TRISE}} = 1.615\text{ V}$ with $\pm 10\text{ mV}$ tolerance | | 1110111 | | | | | |

Electrical Characteristics (continued)

over recommended free-air temperature range, $V_{VIN} = 12\text{ V}$, $V_{V5} = 5\text{ V}$, $V_{VSN} = \text{GND}$, $V_{VSP} = V_{OUT}$ (unless otherwise noted).

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|---|--|--|-----|-----|------|------------|
| OCL-R PIN: OVERCURRENT THRESHOLDS AND RAMP SETTINGS | | | | | | |
| I_{OCLx} | Phase OCL level (CSPx-VREF) (valley current-limit) | $R_{OCL-R} = 20\text{ k}\Omega$ and $V_{OCL-R} \leq 0.85\text{ V}$ or $MFR_SPEC_00[3:0] = 0000b$ | 21 | 24 | 27 | A |
| | | $R_{OCL-R} = 24\text{ k}\Omega$ and $V_{OCL-R} \leq 0.85\text{ V}$ or $MFR_SPEC_00[3:0] = 0001b$ | 25 | 27 | 30 | |
| | | $R_{OCL-R} = 30\text{ k}\Omega$ and $V_{OCL-R} \leq 0.85\text{ V}$ or $MFR_SPEC_00[3:0] = 0010b$ | 28 | 30 | 33 | |
| | | $R_{OCL-R} = 39\text{ k}\Omega$ and $V_{OCL-R} \leq 0.85\text{ V}$ or $MFR_SPEC_00[3:0] = 0011b$ | 31 | 33 | 36 | |
| | | $R_{OCL-R} = 56\text{ k}\Omega$ and $V_{OCL-R} \leq 0.85\text{ V}$ or $MFR_SPEC_00[3:0] = 0100b$ | 34 | 36 | 39 | |
| | | $R_{OCL-R} = 75\text{ k}\Omega$ and $V_{OCL-R} \leq 0.85\text{ V}$ or $MFR_SPEC_00[3:0] = 0101b$ | 37 | 39 | 42 | |
| | | $R_{OCL-R} = 100\text{ k}\Omega$ and $V_{OCL-R} \leq 0.85\text{ V}$ or $MFR_SPEC_00[3:0] = 0110b$ | 40 | 42 | 45 | |
| | | $R_{OCL-R} \geq 150\text{ k}\Omega$ and $V_{OCL-R} \leq 0.85\text{ V}$ or $MFR_SPEC_00[3:0] = 0111b$ | 43 | 45 | 48 | |
| | | $R_{OCL-R} = 20\text{ k}\Omega$ and $V_{OCL-R} \geq 0.95\text{ V}$ or $MFR_SPEC_00[3:0] = 1000b$ | 46 | 48 | 51 | |
| | | $R_{OCL-R} = 24\text{ k}\Omega$ and $V_{OCL-R} \geq 0.95\text{ V}$ or $MFR_SPEC_00[3:0] = 1001b$ | 49 | 51 | 54 | |
| | | $R_{OCL-R} = 30\text{ k}\Omega$ and $V_{OCL-R} \geq 0.95\text{ V}$ or $MFR_SPEC_00[3:0] = 1010b$ | 52 | 54 | 57 | |
| | | $R_{OCL-R} = 39\text{ k}\Omega$ and $V_{OCL-R} \geq 0.95\text{ V}$ or $MFR_SPEC_00[3:0] = 1011b$ | 55 | 57 | 60 | |
| | | $R_{OCL-R} = 56\text{ k}\Omega$ and $V_{OCL-R} \geq 0.95\text{ V}$ or $MFR_SPEC_00[3:0] = 1100b$ | 58 | 60 | 63 | |
| | | $R_{OCL-R} = 75\text{ k}\Omega$ and $V_{OCL-R} \geq 0.95\text{ V}$ or $MFR_SPEC_00[3:0] = 1101b$ | 61 | 63 | 66 | |
| | | $R_{OCL-R} = 100\text{ k}\Omega$ and $V_{OCL-R} \geq 0.95\text{ V}$ or $MFR_SPEC_00[3:0] = 1110b$ | 64 | 66 | 69 | |
| $R_{OCL-R} \geq 150\text{ k}\Omega$ and $V_{OCL-R} \geq 0.95\text{ V}$ or $MFR_SPEC_00[3:0] = 1111b$ | 67 | 69 | 72 | | | |
| V_{RAMP} | Ramp setting | $V_{OCL-R} = 0.2\text{ V} \pm 50\text{mV}$ or $V_{OCL-R} = 1.0\text{ V} \pm 50\text{mV}$ or $MFR_SPEC_14[2:0] = 001b$ | 30 | 40 | 50 | mV_{P-P} |
| | | $V_{OCL-R} = 0.4\text{ V} \pm 50\text{mV}$ or $V_{OCL-R} = 1.2\text{ V} \pm 50\text{mV}$ or $MFR_SPEC_14[2:0] = 011b$ | 70 | 80 | 90 | |
| | | $V_{OCL-R} = 0.6\text{ V} \pm 50\text{mV}$ or $V_{OCL-R} = 1.4\text{ V} \pm 50\text{mV}$ or $MFR_SPEC_14[2:0] = 110b$ | 135 | 145 | 155 | |
| | | $V_{OCL-R} = 0.8\text{ V} \pm 50\text{mV}$ or $V_{OCL-R} = 1.6\text{ V} \pm 50\text{mV}$ or $MFR_SPEC_14[2:0] = 111b$ | 180 | 190 | 205 | |
| F-IMAX PIN: FREQUENCY AND IMAX SETTINGS | | | | | | |
| f_{SW} | Switching frequency (See Switching Characteristics) | | | | | |
| I_{MAX} | IMAX values | $V_{F-IMAX(min)} = 0.136\text{ V}$ $I_{MAX} = (V_{F-IMAX} / V_{VREF} \times 256) - 0.5$ | 18 | 20 | 22 | A |
| | | $V_{F-IMAX(min)} = 0.403\text{ V}$ $I_{MAX} = (V_{F-IMAX} / V_{VREF} \times 256) - 0.5$ | 58 | 60 | 62 | |
| | | $V_{F-IMAX(min)} = 0.536\text{ V}$ $I_{MAX} = (V_{F-IMAX} / V_{VREF} \times 256) - 0.5$ | 78 | 80 | 82 | |
| | | $V_{F-IMAX(min)} = 0.803\text{ V}$ $I_{MAX} = (V_{F-IMAX} / V_{VREF} \times 256) - 0.5$ | 118 | 120 | 122 | |

Electrical Characteristics (continued)

 over recommended free-air temperature range, $V_{VIN} = 12\text{ V}$, $V_{V5} = 5\text{ V}$, $V_{VSN} = \text{GND}$, $V_{VSP} = V_{OUT}$ (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-------------------|--|------|------|-----|-------------|
| SLEW-MODE PIN: SLEW RATES and MODE SELECTIONS | | | | | | |
| SL _{SET} | Slew rate setting | $R_{\text{SLEW-MODE}} \leq 20\text{ k}\Omega$ or MFR_SPEC_13[2:0] = 000b and MFR_SPEC_07[2] = 0b | 0.28 | 0.34 | | mV/ μ s |
| | | $R_{\text{SLEW-MODE}} = 24\text{ k}\Omega$ or MFR_SPEC_13[2:0] = 001b and MFR_SPEC_07[2] = 0b | 0.60 | 0.68 | | |
| | | $R_{\text{SLEW-MODE}} = 30\text{ k}\Omega$ or MFR_SPEC_13[2:0] = 010b and MFR_SPEC_07[2] = 0b | 0.91 | 1.02 | | |
| | | $R_{\text{SLEW-MODE}} = 39\text{ k}\Omega$ or MFR_SPEC_13[2:0] = 011b and MFR_SPEC_07[2] = 0b | 1.22 | 1.36 | | |
| | | $R_{\text{SLEW-MODE}} = 56\text{ k}\Omega$ or MFR_SPEC_13[2:0] = 100b and MFR_SPEC_07[2] = 0b | 1.53 | 1.7 | | |
| | | $R_{\text{SLEW-MODE}} = 75\text{ k}\Omega$ or MFR_SPEC_13[2:0] = 101b and MFR_SPEC_07[2] = 0b | 1.85 | 2.04 | | |
| | | $R_{\text{SLEW-MODE}} = 100\text{ k}\Omega$ or MFR_SPEC_13[2:0] = 110b and MFR_SPEC_07[2] = 0b | 2.16 | 2.38 | | |
| | | $R_{\text{SLEW-MODE}} \geq 150\text{ k}\Omega$ or MFR_SPEC_13[2:0] = 111b and MFR_SPEC_07[2] = 0b | 2.48 | 2.74 | | |
| | | $R_{\text{SLEW-MODE}} \leq 20\text{ k}\Omega$ or MFR_SPEC_13[2:0] = 000b and MFR_SPEC_07[2] = 1b | 1.53 | 1.7 | | |
| | | $R_{\text{SLEW-MODE}} = 24\text{ k}\Omega$ or MFR_SPEC_13[2:0] = 001b and MFR_SPEC_07[2] = 1b | 1.85 | 2.04 | | |
| | | $R_{\text{SLEW-MODE}} = 30\text{ k}\Omega$ or MFR_SPEC_13[2:0] = 010b and MFR_SPEC_07[2] = 1b | 2.16 | 2.38 | | |
| | | $R_{\text{SLEW-MODE}} = 39\text{ k}\Omega$ or MFR_SPEC_13[2:0] = 011b and MFR_SPEC_07[2] = 1b | 2.48 | 2.74 | | |
| | | $R_{\text{SLEW-MODE}} = 56\text{ k}\Omega$ or MFR_SPEC_13[2:0] = 100b and MFR_SPEC_07[2] = 1b | 2.79 | 3.08 | | |
| | | $R_{\text{SLEW-MODE}} = 75\text{ k}\Omega$ or MFR_SPEC_13[2:0] = 101b and MFR_SPEC_07[2] = 1b | 3.10 | 3.43 | | |
| | | $R_{\text{SLEW-MODE}} = 100\text{ k}\Omega$ or MFR_SPEC_13[2:0] = 110b and MFR_SPEC_07[2] = 1b | 3.41 | 3.76 | | |
| $R_{\text{SLEW-MODE}} \geq 150\text{ k}\Omega$ or MFR_SPEC_13[2:0] = 111b and MFR_SPEC_07[2] = 1b | 3.73 | 4.13 | | | | |

Electrical Characteristics (continued)

over recommended free-air temperature range, $V_{VIN} = 12\text{ V}$, $V_{V5} = 5\text{ V}$, $V_{VSN} = \text{GND}$, $V_{VSP} = V_{OUT}$ (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|--|-----|------|-----|------|
| MODE | MODE bits set ⁽¹⁾ ($M_3M_2M_1M_0$) | $V_{SLEW-MODE} \leq 0.053\text{ V}$ with $\pm 20\text{ mV}$ tolerance, or MFR_SPEC_13[7:3] = 00x00 | | 0000 | | |
| | | $V_{SLEW-MODE} = 0.159\text{ V}$ with $\pm 20\text{ mV}$ tolerance, MFR_SPEC_13[7:3] = 00x01b | | 0001 | | |
| | | $V_{SLEW-MODE} = 0.266\text{ V}$ with $\pm 20\text{ mV}$ tolerance, MFR_SPEC_13[7:3] = 00x10b | | 0010 | | |
| | | $V_{SLEW-MODE} = 0.372\text{ V}$ with $\pm 20\text{ mV}$ tolerance, MFR_SPEC_13[7:3] = 00x11b | | 0011 | | |
| | | $V_{SLEW-MODE} = 0.478\text{ V}$ with $\pm 20\text{ mV}$ tolerance, MFR_SPEC_13[7:3] = 01x00b | | 0100 | | |
| | | $V_{SLEW-MODE} = 0.584\text{ V}$ with $\pm 20\text{ mV}$ tolerance, MFR_SPEC_13[7:3] = 01x01b | | 0101 | | |
| | | $V_{SLEW-MODE} = 0.691\text{ V}$ with $\pm 20\text{ mV}$ tolerance, MFR_SPEC_13[7:3] = 01x10b | | 0110 | | |
| | | $V_{SLEW-MODE} = 0.797\text{ V}$ with $\pm 20\text{ mV}$ tolerance, MFR_SPEC_13[7:3] = 01x11b | | 0111 | | |
| | | $V_{SLEW-MODE} = 0.903\text{ V}$ with $\pm 20\text{ mV}$ tolerance, MFR_SPEC_13[7:3] = 10x00b | | 1000 | | |
| | | $V_{SLEW-MODE} = 1.009\text{ V}$ with $\pm 20\text{ mV}$ tolerance, MFR_SPEC_13[7:3] = 10x01b | | 1001 | | |
| | | $V_{SLEW-MODE} = 1.116\text{ V}$ with $\pm 20\text{ mV}$ tolerance, MFR_SPEC_13[7:3] = 10x10b | | 1010 | | |
| | | $V_{SLEW-MODE} = 1.222\text{ V}$ with $\pm 20\text{ mV}$ tolerance, MFR_SPEC_13[7:3] = 10x11b | | 1011 | | |
| | | $V_{SLEW-MODE} = 1.328\text{ V}$ with $\pm 20\text{ mV}$ tolerance, MFR_SPEC_13[7:3] = 11x00b | | 1100 | | |
| | | $V_{SLEW-MODE} = 1.434\text{ V}$ with $\pm 20\text{ mV}$ tolerance, MFR_SPEC_13[7:3] = 11x01b | | 1101 | | |
| $V_{SLEW-MODE} = 1.541\text{ V}$ with $\pm 20\text{ mV}$ tolerance, MFR_SPEC_13[7:3] = 11x10b | | 1110 | | | | |
| $V_{SLEW-MODE} = 1.615\text{ V}$ with $\pm 10\text{ mV}$ tolerance, MFR_SPEC_13[7:3] = 11x11b | | 1111 | | | | |
| O-USR PIN: OVERSHOOT AND UNDERSHOOT REDUCTION THRESHOLD SETTING | | | | | | |
| V_{OSR} | OSR voltage setting | $R_{O-USR} \leq 20\text{ k}\Omega$ or MFR_SPEC_09 [2:0] = 000b | 20 | 30 | 40 | mV |
| | | $R_{O-USR} = 24\text{ k}\Omega$ or MFR_SPEC_09 [2:0] = 001b | 30 | 40 | 50 | |
| | | $R_{O-USR} = 30\text{ k}\Omega$ or MFR_SPEC_09 [2:0] = 010b | 50 | 60 | 70 | |
| | | $R_{O-USR} = 39\text{ k}\Omega$ or MFR_SPEC_09 [2:0] = 011b | 70 | 80 | 90 | |
| | | $R_{O-USR} = 56\text{ k}\Omega$ or MFR_SPEC_09 [2:0] = 100b | 90 | 100 | 110 | |
| | | $R_{O-USR} = 75\text{ k}\Omega$ or MFR_SPEC_09 [2:0] = 101b | 110 | 120 | 130 | |
| | | $R_{O-USR} = 100\text{ k}\Omega$ or MFR_SPEC_09 [2:0] = 110b | 130 | 140 | 150 | |
| | | $R_{O-USR} \geq 150\text{ k}\Omega$ or MFR_SPEC_09 [2:0] = 111b | | OFF | | |
| V_{USR} | USR voltage setting | $V_{O-USR} = 0.2\text{ V}$ with $\pm 50\text{ mV}$ tolerance or MFR_SPEC_09 [6:4] = 000b | 10 | 20 | 30 | mV |
| | | $V_{O-USR} = 0.4\text{ V}$ with $\pm 50\text{ mV}$ tolerance or MFR_SPEC_09 [6:4] = 001b | 20 | 30 | 40 | |
| | | $V_{O-USR} = 0.6\text{ V}$ with $\pm 50\text{ mV}$ tolerance or MFR_SPEC_09 [6:4] = 010b | 50 | 60 | 70 | |
| | | $V_{O-USR} = 0.8\text{ V}$ with $\pm 50\text{ mV}$ tolerance or MFR_SPEC_09 [6:4] = 011b | 70 | 80 | 90 | |
| | | $V_{O-USR} = 1.0\text{ V}$ with $\pm 50\text{ mV}$ tolerance or MFR_SPEC_09 [6:4] = 100b | 90 | 100 | 110 | |
| | | $V_{O-USR} = 1.2\text{ V}$ with $\pm 50\text{ mV}$ tolerance or MFR_SPEC_09 [6:4] = 101b | 110 | 120 | 130 | |
| | | $V_{O-USR} = 1.4\text{ V}$ with $\pm 50\text{ mV}$ tolerance or MFR_SPEC_09 [6:4] = 110b | 130 | 140 | 150 | |
| $1.55\text{ V} \leq V_{O-USR} \leq 1.6\text{ V}$ or MFR_SPEC_09 [6:4] = 111b | | OFF | | | | |
| V_{OSRHYS} | OSR voltage hysteresis ⁽¹⁾ | All settings | | 10 | | mV |
| V_{USRHYS} | USR voltage hysteresis ⁽¹⁾ | All settings | | 10 | | mV |

(1) Specified by design. Not production tested.

Electrical Characteristics (continued)

 over recommended free-air temperature range, $V_{VIN} = 12\text{ V}$, $V_{V5} = 5\text{ V}$, $V_{VSN} = \text{GND}$, $V_{VSP} = V_{OUT}$ (unless otherwise noted).

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|--|------|------|---------------|
| VBOOT PIN: BOOT VOLTAGE SETTING | | | | | |
| $V_{BOOT}^{(1)}$ | BOOT voltage setting ($B_3B_2B_1$) | $R_{VBOOT} \leq 20\text{ k}\Omega$, or MFR_SPEC_11 [3:1] = 000b | | 000 | |
| | | $R_{VBOOT} = 24\text{ k}\Omega$, or MFR_SPEC_11 [3:1] = 001b | | 001 | |
| | | $R_{VBOOT} = 30\text{ k}\Omega$, or MFR_SPEC_11 [3:1] = 010b | | 010 | |
| | | $R_{VBOOT} = 39\text{ k}\Omega$, or MFR_SPEC_11 [3:1] = 011b | | 011 | |
| | | $R_{VBOOT} = 56\text{ k}\Omega$, or MFR_SPEC_11 [3:1] = 100b | | 100 | |
| | | $R_{VBOOT} = 75\text{ k}\Omega$, or MFR_SPEC_11 [3:1] = 101b | | 101 | |
| | | $R_{VBOOT} = 100\text{ k}\Omega$, or MFR_SPEC_11 [3:1] = 110b | | 110 | |
| | | $R_{VBOOT} \geq 150\text{ k}\Omega$, or MFR_SPEC_11 [3:1] = 111b | | 111 | |
| | BOOT voltage setting ($B_7B_6B_5B_4$) | $V_{VBOOT} \leq 0.053\text{ V}$ with $\pm 20\text{ mV}$ tolerance, or MFR_SPEC_11 [7:4] = 0000b | | 0000 | |
| | | $V_{VBOOT} = 0.159\text{ V}$ with $\pm 20\text{ mV}$ tolerance, or MFR_SPEC_11 [7:4] = 0001b | | 0001 | |
| | | $V_{VBOOT} = 0.266\text{ V}$ with $\pm 20\text{ mV}$ tolerance, or MFR_SPEC_11 [7:4] = 0010b | | 0010 | |
| | | $V_{VBOOT} = 0.372\text{ V}$ with $\pm 20\text{ mV}$ tolerance, or MFR_SPEC_11 [7:4] = 0011b | | 0011 | |
| | | $V_{VBOOT} = 0.478\text{ V}$ with $\pm 20\text{ mV}$ tolerance, or MFR_SPEC_11 [7:4] = 0100b | | 0100 | |
| | | $V_{VBOOT} = 0.584\text{ V}$ with $\pm 20\text{ mV}$ tolerance, or MFR_SPEC_11 [7:4] = 0101b | | 0101 | |
| | | $V_{VBOOT} = 0.691\text{ V}$ with $\pm 20\text{ mV}$ tolerance, or MFR_SPEC_11 [7:4] = 0110b | | 0110 | |
| | | $V_{VBOOT} = 0.797\text{ V}$ with $\pm 20\text{ mV}$ tolerance, or MFR_SPEC_11 [7:4] = 0111b | | 0111 | |
| | | $V_{VBOOT} = 0.903\text{ V}$ with $\pm 20\text{ mV}$ tolerance, or MFR_SPEC_11 [7:4] = 1000b | | 1000 | |
| | | $V_{VBOOT} = 1.009\text{ V}$ with $\pm 20\text{ mV}$ tolerance, or MFR_SPEC_11 [7:4] = 1001b | | 1001 | |
| | | $V_{VBOOT} = 1.116\text{ V}$ with $\pm 20\text{ mV}$ tolerance, or MFR_SPEC_11 [7:4] = 1010b | | 1010 | |
| | | $V_{VBOOT} = 1.222\text{ V}$ with $\pm 20\text{ mV}$ tolerance, or MFR_SPEC_11 [7:4] = 1011b | | 1011 | |
| | | $V_{VBOOT} = 1.328\text{ V}$ with $\pm 20\text{ mV}$ tolerance, or MFR_SPEC_11 [7:4] = 1100b | | 1100 | |
| $V_{VBOOT} = 1.434\text{ V}$ with $\pm 20\text{ mV}$ tolerance, or MFR_SPEC_11 [7:4] = 1101b | | | 1101 | | |
| $V_{VBOOT} = 1.541\text{ V}$ with $\pm 20\text{ mV}$ tolerance, or MFR_SPEC_11 [7:4] = 1110b | | 1110 | | | |
| $V_{VBOOT} = 1.615\text{ V}$ with $\pm 10\text{ mV}$ tolerance, or MFR_SPEC_11 [7:4] = 1111b | | 1111 | | | |
| PROTECTION: OVP, UVP, VR_RDY | | | | | |
| V_{OVFPF} | Pre-bias OVP voltage threshold ⁽¹⁾ | ENABLE is low and $V_{VSP} > V_{OVFPF}$, PWM \rightarrow LO | | 2.75 | V |
| V_{OVPH5} | Fixed OVP voltage threshold (VR12.5) | ENABLE is high and $(V_{VSP} - V_{VSN}) > V_{OVPH5}$ for 1 μs , PWM \rightarrow LO, $V_{OUT(max)} \leq 1.8\text{ V}$ | | 2.2 | V |
| | | $1.8\text{ V} < V_{OUT(max)} \leq 2.0\text{ V}$ | | 2.4 | |
| | | $2.0\text{ V} < V_{OUT(max)} \leq 2.2\text{ V}$ | | 2.6 | |
| | | $V_{OUT(max)} > 2.2\text{ V}$ | | 2.8 | |
| V_{OVPF0} | Fixed OVP voltage threshold (VR12.0) | ENABLE is high and $(V_{VSP} - V_{VSN}) > V_{OVPH5}$ for 1 μs , PWM \rightarrow LO, | 1.7 | 1.75 | 1.8 |
| V_{OVPT5} | Tracking OVP offset (VR12.5) | Measured at the VSP pin w/r/t VID code, device latches OFF | 340 | 375 | 405 |
| V_{OVPT0} | Tracking OVP offset (VR12.0) | Measured at the VSP pin w/r/t VID code, device latches OFF | 200 | 225 | 250 |
| V_{RDYL} | VR_RDY low (UVP) threshold | Measured at the VSP pin w/r/t VID code, device latches OFF | 175 | 207 | 235 |
| $t_{RDYDGLTO}$ | VR_RDY deglitch time | Time from VSP out of overvoltage threshold to VR_RDY low | | 1 | μs |
| $t_{RDYDGLTU}$ | VR_RDY deglitch time | Time from VSP out of undervoltage threshold to VR_RDY low, ($f_{SW} = 500\text{ kHz}$) | | 32 | μs |
| t_{HICCUP} | Hiccup delay after UVP and OCP | | | 22 | ms |

Electrical Characteristics (continued)

over recommended free-air temperature range, $V_{VIN} = 12\text{ V}$, $V_{V5} = 5\text{ V}$, $V_{VSN} = \text{GND}$, $V_{VSP} = V_{OUT}$ (unless otherwise noted).

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--|--|--|-----|---------------------------------|--------------|------------------|
| TSEN PIN AND THERMAL SHUTDOWN: THERMAL VOLTAGE LEVELS | | | | | | |
| V_{TSEN} | Thermal voltage definition | $T_J = 90^\circ\text{C}$ | | 1.32 | V | |
| | | $T_J = 95^\circ\text{C}$ | | 1.36 | | |
| | | $T_J = 100^\circ\text{C}$ | | 1.4 | | |
| | | $T_J = 105^\circ\text{C}$ | | 1.44 | | |
| | | $T_J = 110^\circ\text{C}$ | | 1.48 | | |
| | | $T_J = 115^\circ\text{C}$ | | 1.52 | | |
| | | $T_J = 120^\circ\text{C}$ | | 1.56 | | |
| I_{TSEN} | TSEN current | Leakage current | | -3 | 3 | μA |
| OTP_{THLD} | Over temperature protection threshold | Based on the temperature measured on TSEN pin, default value | | 125 | | $^\circ\text{C}$ |
| OTP_{HYS} | Over temperature protection hysteresis | | | 15 | | $^\circ\text{C}$ |
| PWM and SKIP-NVM OUTPUT: I/O VOLTAGE AND CURRENT$^\circ\text{C}$ | | | | | | |
| V_{PWML} | PWMx output low level | $I_{LOAD} = -1\text{ mA}$ | | 0.15 | 0.3 | V |
| V_{PWMH} | PWMx output high Level | $I_{LOAD} = +1\text{ mA}$ | 2.5 | | | V |
| $V_{SKIP-NVM_L}$ | SKIP-NVM output low Level | $I_{LOAD} = -1\text{ mA}$ | | 0.15 | 0.3 | V |
| $V_{SKIP-NVM_H}$ | SKIP-NVM output high Level | $I_{LOAD} = +1\text{ mA}$ | 2.5 | | | V |
| R_{P-S_UV} | PWMx/SKIP-NVM resistance ⁽¹⁾ | ENABLE = LOW, or UVLO | | 10 | | $\text{M}\Omega$ |
| DYNAMIC PHASE SHEDDING: THRESHOLDS | | | | | | |
| I_{DPSTHL} | Dynamic phase add/drop low threshold current | MFR_SPEC_15 [3] = 0b | | N.A | A | |
| | | MFR_SPEC_15 [3] = 1b | | $10\% \times 4 \times I_{OCLx}$ | | |
| I_{DPSTHH} | Dynamic phase add/drop high threshold voltage | MFR_SPEC_15 [2:0] = 000b | | $15\% \times 4 \times I_{OCLx}$ | A | |
| | | MFR_SPEC_15 [2:0] = 001b | | $20\% \times 4 \times I_{OCLx}$ | | |
| | | MFR_SPEC_15 [2:0] = 010b | | $25\% \times 4 \times I_{OCLx}$ | | |
| | | MFR_SPEC_15 [2:0] = 011b | | $30\% \times 4 \times I_{OCLx}$ | | |
| | | MFR_SPEC_15 [2:0] = 1xxb | | $35\% \times 4 \times I_{OCLx}$ | | |
| I_{DPSHYS} | Dynamic phase add/drop high hysteresis voltage | Hysteresis | | $5\% \times 4 \times I_{OCLx}$ | A | |
| PROGRAMMABLE DROOP SETTING | | | | | | |
| DROOP | Droop percentage settings | MFR_SPEC_08 [7:0] = 00h | | 0 | % | |
| | | MFR_SPEC_08 [7:0] = 01h | | 25 | | |
| | | MFR_SPEC_08 [7:0] = 02h | | 50 | | |
| | | MFR_SPEC_08 [7:0] = 03h | | 75 | | |
| | | MFR_SPEC_08 [7:0] = 04h (Default Setting) | | 100 | | |
| | | MFR_SPEC_08 [7:0] = 10h | | 80 | | |
| | | MFR_SPEC_08 [7:0] = 20h | | 85 | | |
| | | MFR_SPEC_08 [7:0] = 30h | | 90 | | |
| | | MFR_SPEC_08 [7:0] = 40h | | 95 | | |
| | | MFR_SPEC_08 [7:0] = 50h | | 105 | | |
| | | MFR_SPEC_08 [7:0] = 60h | | 110 | | |
| | | MFR_SPEC_08 [7:0] = 70h | | 115 | | |
| | | MFR_SPEC_08 [7:0] = 80h | | 120 | | |
| | | MFR_SPEC_08 [7:0] = 90h | | 125 | | |
| MFR_SPEC_08 [7:0] = A0h | | 150 | | | | |
| SKIP-NVM PIN: PROGRAM MODE SETTING (NVM OR PINSTRAP) | | | | | | |
| PGRM | Program mode for the configurations | $R_{SKIP-NVM} \leq 20\text{ k}\Omega$ | | Pinstrap | Program Mode | |
| | | $R_{SKIP-NVM} \geq 100\text{ k}\Omega$ | | NVM | | |

Electrical Characteristics (continued)

over recommended free-air temperature range, $V_{VIN} = 12\text{ V}$, $V_{V5} = 5\text{ V}$, $V_{VSN} = \text{GND}$, $V_{VSP} = V_{OUT}$ (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------|--------------------------------|--|-------|-----|------|------|
| IMON PIN: CURRENT MONITOR | | | | | | |
| $I_{IMON4LK}$ | 0% IMAX level current output | 4 phase, IMAX=80A, $\Sigma i_L = 0\text{ A}$, $R_{IMON}=74.38k\Omega$ | 0 | | 4 | A |
| $I_{IMON4LO}$ | 20% IMAX level current output | 4 phase, IMAX=80A, $\Sigma i_L = 16\text{ A}$, $R_{IMON}=74.38k\Omega$ | 13 | 16 | 18.5 | A |
| $I_{IMON4MID}$ | 100% IMAX level current output | 4 phase, IMAX=80A, $\Sigma i_L = 80\text{ A}$, $R_{IMON}=74.38k\Omega$ | 75 | 80 | 84 | A |
| $I_{IMON4HI}$ | 125% IMAX level current output | 4 phase, IMAX=80A, $\Sigma i_L = 100\text{ A}$, $R_{IMON}=74.38k\Omega$ | 94 | 100 | 105 | A |
| VOUT MEASUREMENT: READ_VOVT | | | | | | |
| $M_{VOUT(mg)}$ | V_{OUT} measurement range | | 0.5 | | 2.3 | V |
| READ_VOVT accuracy | | $0.5\text{ V} \leq V_{OUT} < 0.7\text{ V}$, VR12.0 mode | -2 | | +2 | VID |
| | | $0.7\text{ V} \leq V_{OUT} \leq 1.0\text{ V}$, VR12.0 mode | -1 | | +1 | |
| | | $1.0\text{ V} < V_{OUT} \leq 1.52\text{ V}$, VR12.0 mode | -2 | | +2 | |
| | | $0.5\text{ V} \leq V_{OUT} \leq 2.3\text{ V}$, VR12.5 mode | -1 | | +1 | |
| MFR_READ_VOVT accuracy | | $0.5\text{ V} \leq V_{OUT} < 0.7\text{ V}$, VR12.0 mode | -12.5 | | 12.5 | mV |
| | | $0.7\text{ V} \leq V_{OUT} \leq 1.0\text{ V}$, VR12.0 mode | -7.5 | | 7.5 | |
| | | $1.0\text{ V} < V_{OUT} \leq 1.52\text{ V}$, VR12.0 mode | -10 | | 10 | |
| | | $0.5\text{ V} \leq V_{OUT} \leq 2.3\text{ V}$, VR12.5 mode | -12.5 | | 12.5 | |

6.6 I/O Timing Requirements

| | | | MIN | TYP | MAX | UNIT |
|----------------|--|---|-----|-----|-----|------|
| $t_{STARTUP1}$ | Startup time | $V_{BOOT} > 0\text{ V}$, no faults, time from V3R3 high to VOUT ramp, $C_{VREF} = 1\text{ }\mu\text{F}$ | | | 1.2 | ms |
| $t_{STARTUP2}$ | Startup time | $V_{BOOT} > 0\text{ V}$, no faults, time from V3R3 high until the controller responds to PMBus commands, $C_{VREF} = 1\text{ }\mu\text{F}$ | | | 1.5 | ms |
| t_{RDY_POD} | VR_RDY power-on-delay time ⁽¹⁾ | DAC settled to VR_RDY going high | | 1 | | ms |
| t_{OFF_MIN} | Controller minimum OFF time ⁽¹⁾ | Fixed value | 20 | 50 | 80 | ns |
| t_{EN_RDY} | ENABLE low to VR_RDY low | | 20 | | 100 | ns |
| t_{RDY_VSP} | VR_RDY low to VSP change ⁽¹⁾ | | | | 100 | ns |

(1) Specified by design. Not production tested.

6.7 Switching Characteristics

 $T_A = 25^\circ\text{C}$. (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|------------------------------|---------------------|--|-----|------|------|-----|
| F-IMAX PIN: FREQUENCY | | | | | | |
| f_{sw} | Switching frequency | $V_{\text{VIN}} = 12\text{ V}$, $V_{\text{VSP}} = 1.7\text{ V}$ $R_{\text{F-IMAX}} = 20\text{ k}\Omega$ and $\text{MFR_SPEC_12}[7] = 0\text{b}$; or $\text{MFR_SPEC_12}[7:4] = 0000\text{b}$ | 270 | 300 | 330 | kHz |
| | | $V_{\text{VIN}} = 12\text{ V}$, $V_{\text{VSP}} = 1.7\text{ V}$ $R_{\text{F-IMAX}} = 24\text{ k}\Omega$ and $\text{MFR_SPEC_12}[7] = 0\text{b}$; or $\text{MFR_SPEC_12}[7:4] = 0001\text{b}$ | 360 | 400 | 440 | |
| | | $V_{\text{VIN}} = 12\text{ V}$, $V_{\text{VSP}} = 1.7\text{ V}$ $R_{\text{F-IMAX}} = 30\text{ k}\Omega$ and $\text{MFR_SPEC_12}[7] = 0\text{b}$; or $\text{MFR_SPEC_12}[7:4] = 0010\text{b}$ | 450 | 500 | 550 | |
| | | $V_{\text{VIN}} = 12\text{ V}$, $V_{\text{VSP}} = 1.7\text{ V}$ $R_{\text{F-IMAX}} = 39\text{ k}\Omega$ and $\text{MFR_SPEC_12}[7] = 0\text{b}$; or $\text{MFR_SPEC_12}[7:4] = 0011\text{b}$ | 540 | 600 | 660 | |
| | | $V_{\text{VIN}} = 12\text{ V}$, $V_{\text{VSP}} = 1.7\text{ V}$ $R_{\text{F-IMAX}} = 56\text{ k}\Omega$ and $\text{MFR_SPEC_12}[7] = 0\text{b}$; or $\text{MFR_SPEC_12}[7:4] = 0100\text{b}$ | 630 | 700 | 770 | |
| | | $V_{\text{VIN}} = 12\text{ V}$, $V_{\text{VSP}} = 1.7\text{ V}$ $R_{\text{F-IMAX}} = 75\text{ k}\Omega$ and $\text{MFR_SPEC_12}[7] = 0\text{b}$; or $\text{MFR_SPEC_12}[7:4] = 0101\text{b}$ | 720 | 800 | 880 | |
| | | $V_{\text{VIN}} = 12\text{ V}$, $V_{\text{VSP}} = 1.7\text{ V}$ $R_{\text{F-IMAX}} = 100\text{ k}\Omega$ and $\text{MFR_SPEC_12}[7] = 0\text{b}$; or $\text{MFR_SPEC_12}[7:4] = 0110\text{b}$ | 810 | 900 | 990 | |
| | | $V_{\text{VIN}} = 12\text{ V}$, $V_{\text{VSP}} = 1.7\text{ V}$ $R_{\text{F-IMAX}} = 150\text{ k}\Omega$ and $\text{MFR_SPEC_12}[7] = 0\text{b}$; or $\text{MFR_SPEC_12}[7:4] = 0111\text{b}$ | 900 | 1000 | 1100 | |
| | | $V_{\text{VIN}} = 12\text{ V}$, $V_{\text{VSP}} = 1.7\text{ V}$ $R_{\text{F-IMAX}} = 20\text{ k}\Omega$ and $\text{MFR_SPEC_12}[7] = 1\text{b}$; or $\text{MFR_SPEC_12}[7:4] = 1000\text{b}$ | 315 | 350 | 385 | |
| | | $V_{\text{VIN}} = 12\text{ V}$, $V_{\text{VSP}} = 1.7\text{ V}$ $R_{\text{F-IMAX}} = 24\text{ k}\Omega$ and $\text{MFR_SPEC_12}[7] = 1\text{b}$; or $\text{MFR_SPEC_12}[7:4] = 1001\text{b}$ | 405 | 450 | 495 | |
| | | $V_{\text{VIN}} = 12\text{ V}$, $V_{\text{VSP}} = 1.7\text{ V}$ $R_{\text{F-IMAX}} = 30\text{ k}\Omega$ and $\text{MFR_SPEC_12}[7] = 1\text{b}$; or $\text{MFR_SPEC_12}[7:4] = 1010\text{b}$ | 495 | 550 | 605 | |
| | | $V_{\text{VIN}} = 12\text{ V}$, $V_{\text{VSP}} = 1.7\text{ V}$ $R_{\text{F-IMAX}} = 39\text{ k}\Omega$ and $\text{MFR_SPEC_12}[7] = 1\text{b}$; or $\text{MFR_SPEC_12}[7:4] = 1011\text{b}$ | 585 | 650 | 715 | |
| | | $V_{\text{VIN}} = 12\text{ V}$, $V_{\text{VSP}} = 1.7\text{ V}$ $R_{\text{F-IMAX}} = 56\text{ k}\Omega$ and $\text{MFR_SPEC_12}[7] = 1\text{b}$; or $\text{MFR_SPEC_12}[7:4] = 1100\text{b}$ | 675 | 750 | 825 | |
| | | $V_{\text{VIN}} = 12\text{ V}$, $V_{\text{VSP}} = 1.7\text{ V}$ $R_{\text{F-IMAX}} = 75\text{ k}\Omega$ and $\text{MFR_SPEC_12}[7] = 1\text{b}$; or $\text{MFR_SPEC_12}[7:4] = 1101\text{b}$ | 765 | 850 | 935 | |
| | | $V_{\text{VIN}} = 12\text{ V}$, $V_{\text{VSP}} = 1.7\text{ V}$ $R_{\text{F-IMAX}} = 100\text{ k}\Omega$ and $\text{MFR_SPEC_12}[7] = 1\text{b}$; or $\text{MFR_SPEC_12}[7:4] = 1110\text{b}$ | 855 | 950 | 1045 | |
| | | $V_{\text{VIN}} = 12\text{ V}$, $V_{\text{VSP}} = 1.7\text{ V}$ $R_{\text{F-IMAX}} = 150\text{ k}\Omega$ and $\text{MFR_SPEC_12}[7] = 1\text{b}$; or $\text{MFR_SPEC_12}[7:4] = 1111\text{b}$ | 900 | 1000 | 1100 | |

6.8 Typical Characteristics

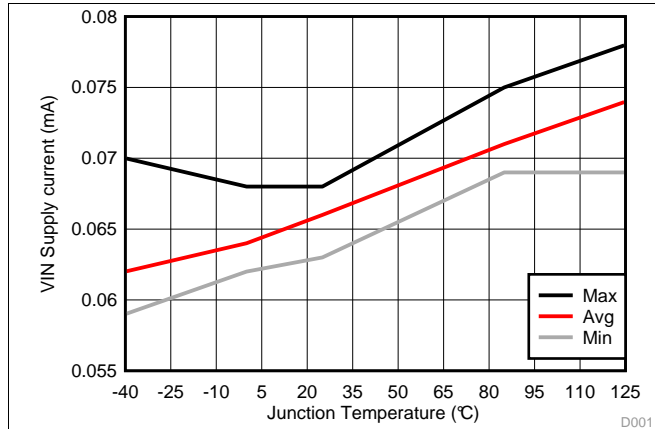


Figure 1. VIN Supply Current vs Junction Temperature

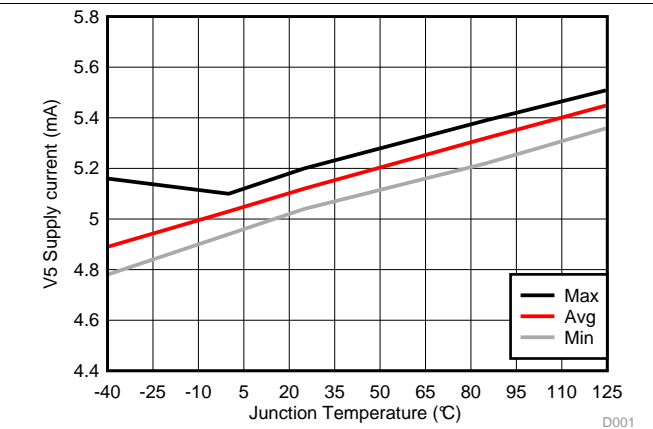


Figure 2. V5 Supply Current vs Junction Temperature

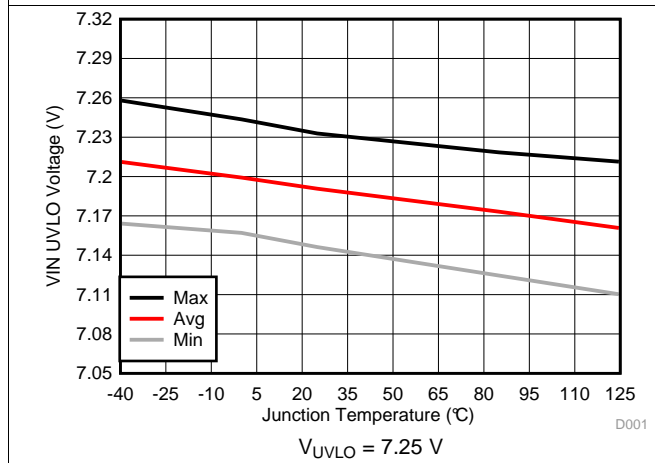


Figure 3. VIN UVLO Voltage vs Junction Temperature

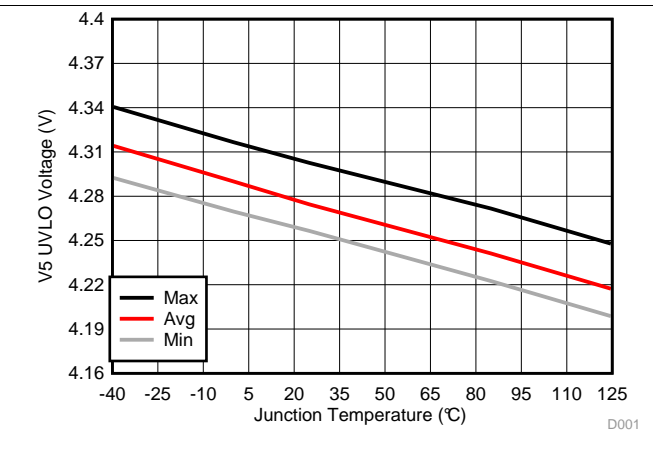


Figure 4. V5 UVLO Voltage vs Junction Temperature

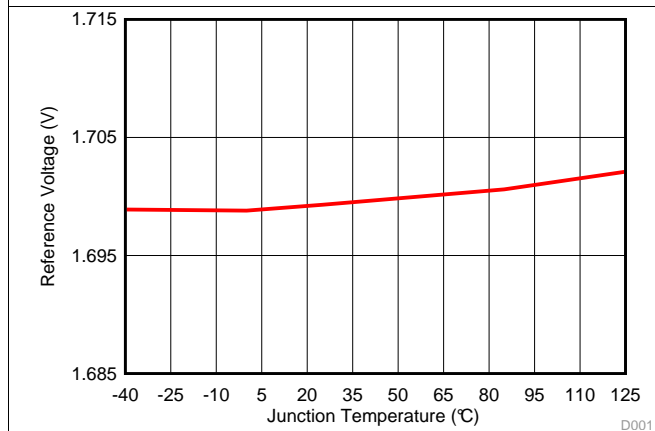


Figure 5. Reference Voltage vs Junction Temperature

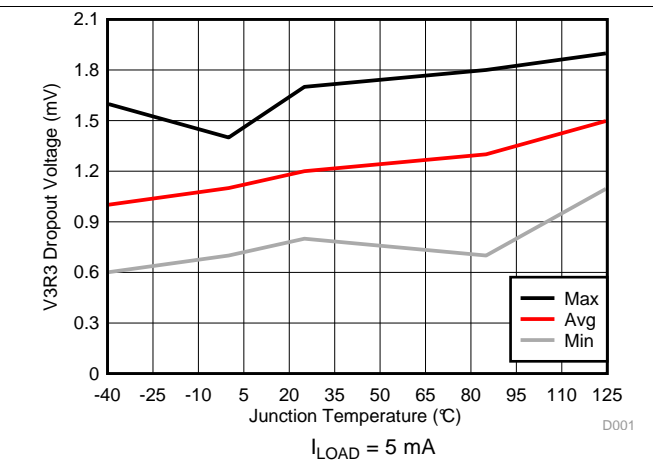


Figure 6. V3R3 Load Regulation vs Junction Temperature

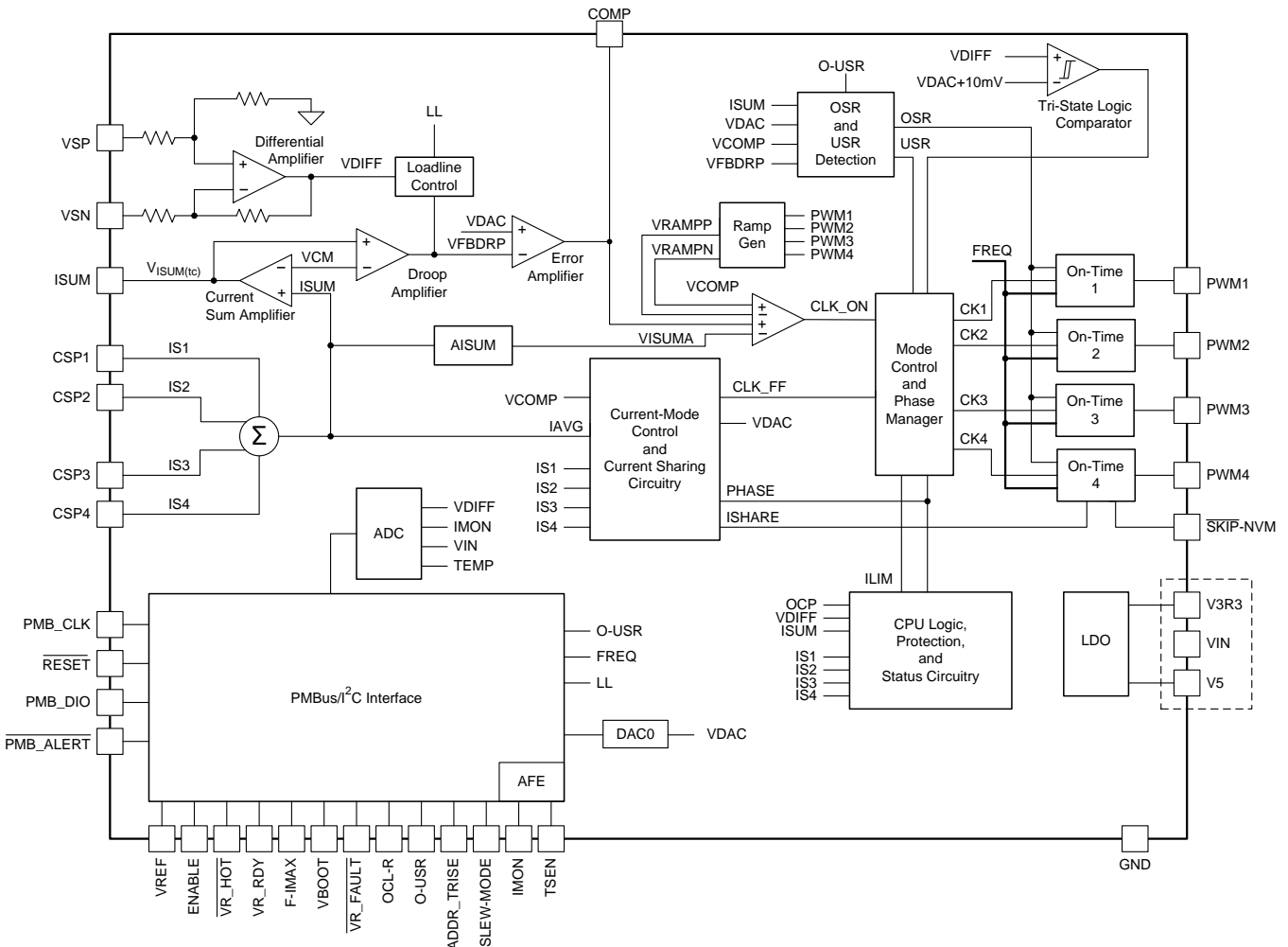
7 Detailed Description

7.1 Overview

The TPS53647 device is a DCAP+ mode adaptive on-time controller.

The output voltage is set using a DAC that outputs a reference in accordance with the 8-bit VID code defined in [Table 1](#). In adaptive on-time converters, the controller varies the on-time as a function of input and output voltage to maintain a nearly constant frequency during steady-state conditions. In conventional voltage-mode constant on-time converters, each cycle begins when the output voltage crosses to a fixed reference level. However, in the TPS53647 device, the cycle begins when the current feedback reaches an error voltage level which corresponds to the amplified voltage difference between the DAC voltage and the feedback output voltage with droop. In the case of multi-phase operations, the current feedback from all the phases is summed, and is amplified using the ISUM pin to adjust the load-line. Also zero-load line operation can be easily configured with external resistor or internal NVM selection.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 V3R3 LDO

V3R3 is an LDO output generated from V5. It is used as internal digital circuit supply and 1-uF to 4.7-uF ceramic decoupling capacitor to GND pin is recommended.

When V5 exceeds $V_{V5UVLOH}$ (4.25 V typically), V3R3 begins to ramp up. The startup time for V3R3 is approximately 600 μ s as shown in Figure 7.

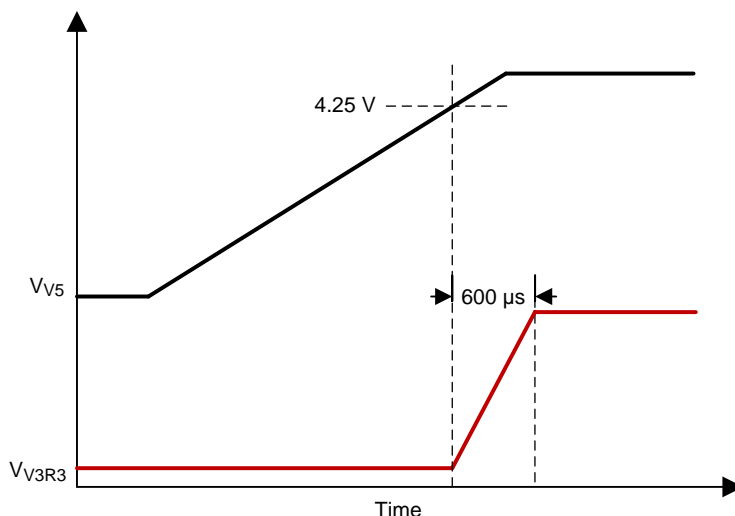


Figure 7. V3R3 Startup Waveform

After V3R3 has reached its operational level, the TPS53647 begins to initialize the internal circuit and reads the pinstrap configurations. This pinstrap reading completes in approximately 1.2 ms, and can communicate to the PMBus 1.5 ms after V3R3 powers up.

NOTE

This device does not require a high ENABLE signal in order for the V3R3 LDO to start up.

Use V3R3 as pull-up voltage for CSPx (to disable phases), ENABLE, VR_RDY, $\overline{VR_HOT}$, and $\overline{VR_FAULT}$. Because the V3R3 maximum current capability is approximately 5 mA, choose pull-up resistances carefully.

Directly tie CSP4, CSP3, or CSP2 to the V3R3 pin according to Table 3 to disable the corresponding phase.

Feature Description (continued)

7.3.2 PWM Operation

As shown in the [Functional Block Diagram](#), in 4-phase continuous conduction mode, the device operates as described in [Figure 8](#).

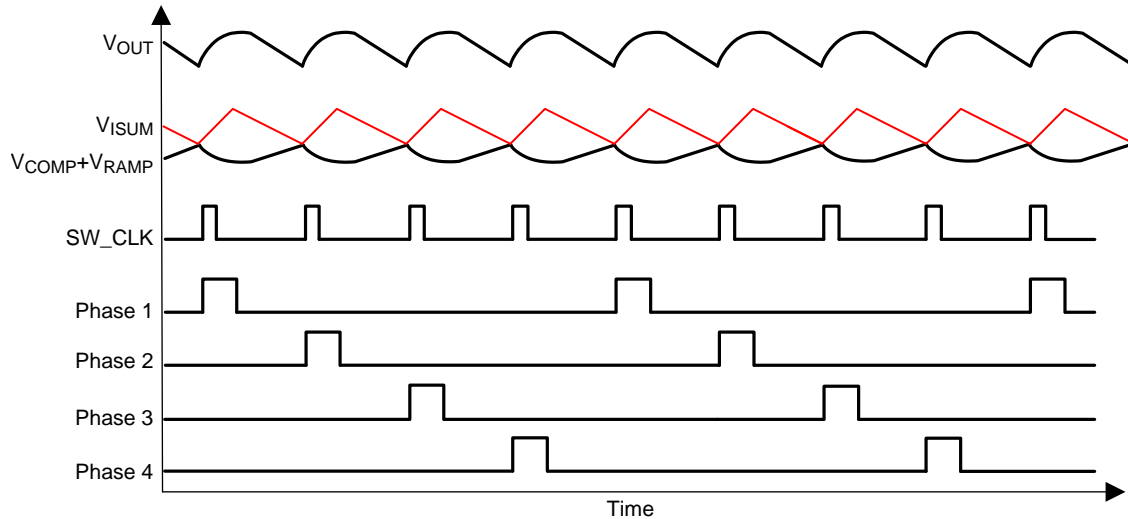


Figure 8. D-CAP+ Mode Basic Waveforms

Starting with the condition that the high-side FETs are off and the low-side FETs are on, the summed current feedback (V_{ISUM}) is higher than the summed error amplifier output (V_{COMP}) and the internal ramp signal (V_{RAMP}). I_{SUM} falls until it hits $V_{COMP}+V_{RAMP}$, which contains a component of the output ripple voltage. The PWM comparator senses where the two waveforms cross and triggers the on-time generator. This generates the internal SW_CLK. Each SW_CLK corresponds to one switching ON pulse for one phase.

In case of single-phase operation, every SW_CLK generates a switching pulse on the same phase. Also, V_{ISUM} corresponds to just a single-phase inductor current.

In case of multi-phase operation, the SW_CLK gets distributed to each of the phases in a cycle. This approach of using the summed inductor current and cyclically distributing the ON pulses to each phase automatically gives the required interleaving of $360 / n$, where n is the number of phases.

7.3.3 Current Sense and IMON Calculation

The TPS53647 device provides independent channels of current feedback for every phase to increase the system accuracy and reduce the dependence of circuit performance on layout compared to an externally summed architecture. The current sensing signals are from TI smart power stages (at 5mV/A) (ex: CSD95372BQ5MC) and are already temperature-compensated. The pins CSP1, CSP2, CSP3, and CSP4 are used for the individual phases of the phase current sensing.

The sensed currents are then summed together and generate a current output to IMON pin. A resistor is connected to IMON pin to generate the V_{IMON} voltage.

$$V_{IMON} = \left(\frac{\sum_{1}^{x=n} V_{CSPx}}{n} - V_{REF} \right) \times n \times \frac{R_{IMON}}{35 \text{ k}\Omega}$$

where

- V_{CSPx} is the voltage of CSPx pin
 - n is the number of active phases
 - R_{IMON} is the value of resistor between the IMON pin and GND in $\text{k}\Omega$
- (1)

Then the V_{IMON} voltage translates to a digital IMON reading as shown in [Equation 2](#).

Feature Description (continued)

$$I_{\text{IMON}} = \frac{I_{\text{MAX}} \times V_{\text{IMON}}}{0.85}$$

where

- 0.85 is the voltage correlated to I_{MAX} (2)

When V_{IMON} is 0.85 V, the IMON reading should be equal to I_{MAX} .

The digital IMON then can be reported to the system by using PMBus command READ_IOUT.

7.3.4 Setting the Load-Line (DROOP)

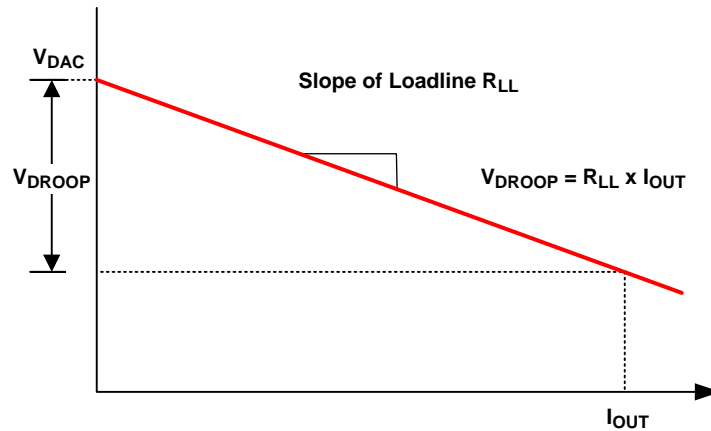


Figure 9. Load Line

A resistor between the ISUM pin and the VREF pin sets the load line in non-zero load line mode.

$$V_{\text{DROOP}} = R_{\text{LL}} \times I_{\text{OUT}} = g_{\text{M}(\text{isum})} \times R_{\text{ISUM}} \times R_{\text{CS}} \times \frac{1}{6} \times I_{\text{OUT}}$$

where

- $g_{\text{M}(\text{isum})}$ is the gain of the internal I_{SUM} amplifier, (500 μS typical)
- R_{ISUM} is the value of resistor between the ISUM pin and the VREF pin to adjust the load line
- R_{CS} is the effective current sense resistance of TI smart power stages, (5 m Ω for CSD95372BQ5MC)
- I_{OUT} is the load current (3)

A desired zero load-line can be implemented by putting a 0 Ω between ISUM and VREF pins or by shorting the ISUM and VREF pins directly.

7.3.5 Load Transitions

When there is a sudden load increase, the output voltage immediately drops. The TPS53647 device reacts to this drop in a rising voltage on the COMP pin. This rise forces the PWM pulses to come in sooner and more frequently which causes the inductor current to rapidly increase. As the inductor current reaches the new load current, the device reaches a steady-state operating condition and the PWM switching resumes the steady-state frequency.

When there is a sudden load release, the output voltage flies high. The TPS53647 device reacts to this rise in a falling voltage on the COMP pin. This drop forces the PWM pulses to be delayed until the inductor current reaches the new load current. At that point, the switching resumes and steady-state switching continues.

Please note in [Figure 10](#) and [Figure 11](#), the ripples on V_{OUT} , V_{RAMP} , and V_{COMP} voltages are not shown for simplicity.

Feature Description (continued)

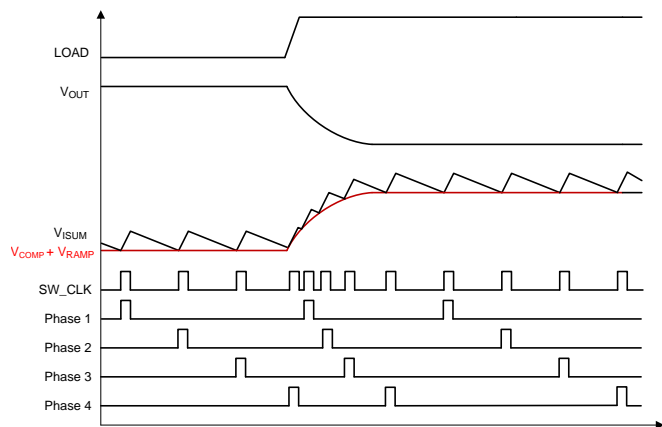


Figure 10. Load Insertion

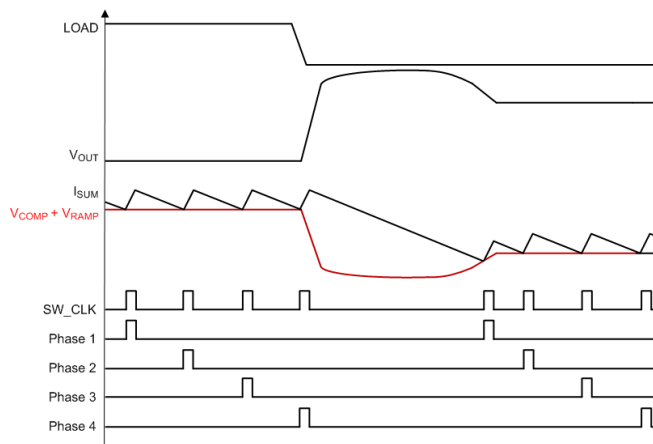


Figure 11. Load Release

7.3.6 Overshoot Reduction (OSR)

The problem of overshoot in low duty-cycle synchronous buck converters is well known, and results from the output inductor having a small voltage (V_{OUT}) with which to respond to a transient load release.

For simplicity, Figure 12 shows a single phase converter. In an ideal converter, with typical input voltage of 12 V and a 1.0-V output, the inductor has 11.0 V (12 V – 1.0 V) to respond to a transient load increase, but only 1.0 V to respond once the load releases.

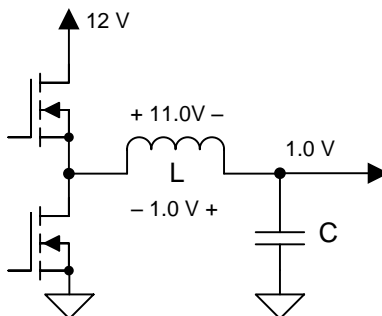


Figure 12. Representative Schematic of Synchronous Buck Converter Circuit

With the Overshoot Reduction (OSR) feature enabled, when the summed voltage of V_{OUT} and V_{DROOP} exceeds the DAC voltage V_{DAC} by the OSR value specified in the [Electrical Characteristics](#) table, the PWM pulses immediately become tri-state to turn off both the high-side and low-side FETs. When the low-side FETs are turned OFF, the energy in the inductor is partially dissipated by the body diodes. Please note the ON pulse width can be also truncated immediately regardless of the load transient timing, and this feature can further reduce the overshoot when compared to the conventional constant on-time controllers as shown in [Figure 13](#).

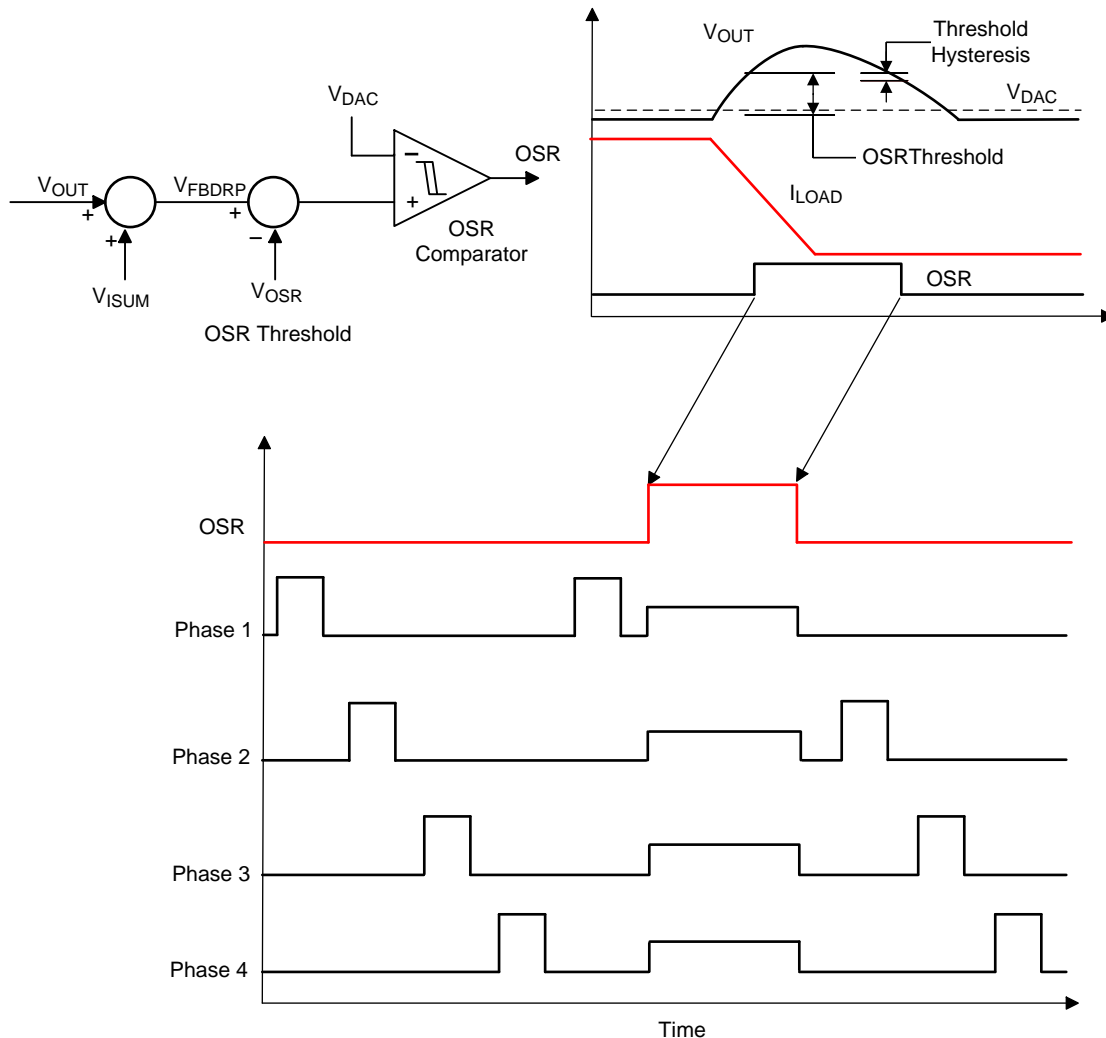
Feature Description (continued)


Figure 13. Performance for a Load Transient Release with OSR Enabled

7.3.7 Undershoot Reduction (USR)

When the transient load increase becomes quite large, it becomes difficult to meet the energy demanded by the load especially at lower input voltages. Then it is necessary to quickly increase the energy in the inductors during the transient load increase. This is achieved in TPS53647 by enabling pulse overlapping. In order to maintain the interleaving of the multi-phase configuration and yet be able to have pulse-overlapping during load-insertion, the Undershoot Reduction (USR) mode is entered only when necessary. This mode is entered when the difference between DAC voltage and the summed voltage of V_{OUT} and V_{DROOP} exceeds the USR voltage level specified in the [Electrical Characteristics](#) table.

The waveforms in [Figure 14](#) indicate the performance with USR. It can be seen that it is possible to eliminate undershoot by enabling USR. This allows reduced output capacitance to be used and still meets the specification.

When the transient condition is over, the interleaving of the phases is resumed.

Feature Description (continued)

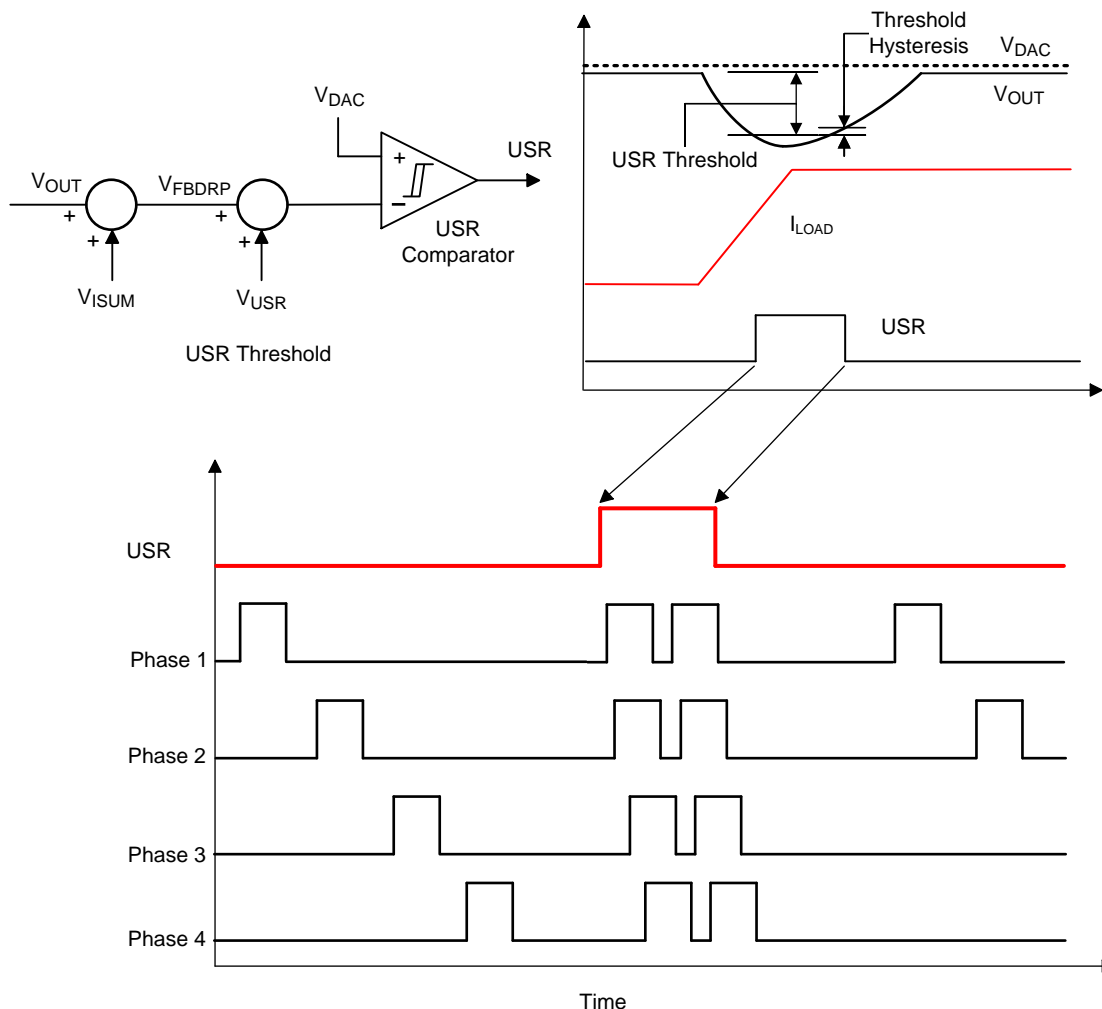
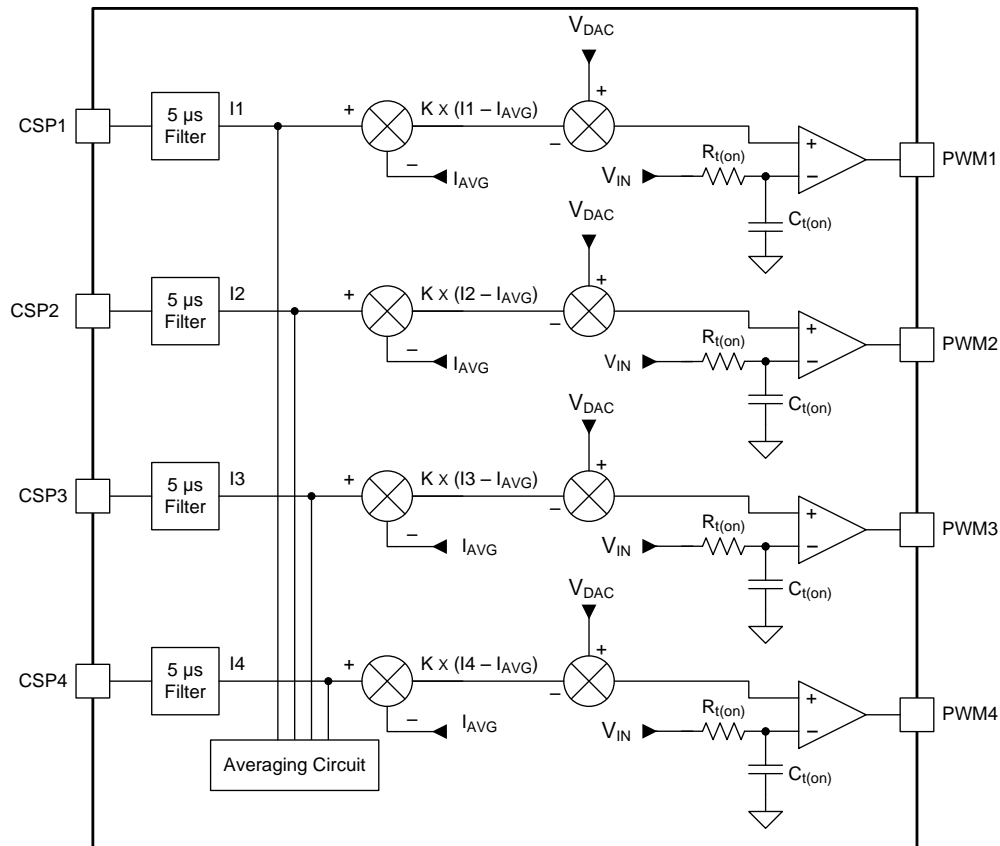


Figure 14. Performance for a Load Transient Step-up With USR Enabled

7.3.8 AutoBalance™ Current Sharing

The basic mechanism for current sharing is to sense the average phase current, then adjust the pulse width of each phase to equalize the current in each phase as shown in Figure 15. The PWM comparator (not shown) starts a pulse when the feedback voltage meets the reference. The V_{IN} voltage charges $C_{t(on)}$ through $R_{t(on)}$. The pulse terminates when the voltage at $C_{t(on)}$ matches the on-time reference, which normally equals the DAC voltage (V_{DAC}).

The circuit operates in the following fashion. First assume that the 5- μ s averaged value from each phase current are equal. In this case, the PWM modulator terminates at V_{DAC} , and the normal pulse width is delivered to the system. If $I_1 > I_{AVG}$, then an offset is subtracted from V_{DAC} , and the pulse width for Phase 1 is shortened to reduce the phase current in Phase 1 for balancing. If $I_1 < I_{AVG}$, then a longer pulse is generated to increase the phase current in Phase 1 to achieve current balancing.

Feature Description (continued)

Figure 15. AutoBalance Current Sharing Circuit Detail
7.3.9 Phase Overlap

During steady state operation, the on-pulses of each phase cannot overlap. Overlapping limits the duty cycle of the application. The duty cycle of the converter cannot exceed $1/n$ (where n is the phase number). The device allows phase overlapping during a transient period, during the USR trigger period.

7.3.10 VID

The DAC voltage V_{DAC} can be changed according to [Table 1](#).

The slew rate for a change is set by the resistor at SLEW-MODE pin, as defined in the [Electrical Characteristics](#) table.

Table 1. VID Table

| VID Hex VALUE | VR12.0 VOLTAGE (V) | VR12.5 VOLTAGE (V) |
|---------------|--------------------|--------------------|
| 00 | 0 | 0 |
| 01 | 0.25 | 0.50 |
| 02 | 0.255 | 0.51 |
| 03 | 0.26 | 0.52 |
| 04 | 0.265 | 0.53 |
| 05 | 0.27 | 0.54 |
| 06 | 0.275 | 0.55 |
| 07 | 0.28 | 0.56 |
| 08 | 0.285 | 0.57 |
| 09 | 0.29 | 0.58 |
| 0A | 0.295 | 0.59 |
| 0B | 0.30 | 0.60 |
| 0C | 0.305 | 0.61 |
| 0D | 0.31 | 0.62 |
| 0E | 0.315 | 0.63 |
| 0F | 0.32 | 0.64 |
| 10 | 0.325 | 0.65 |
| 11 | 0.33 | 0.66 |
| 12 | 0.335 | 0.67 |
| 13 | 0.34 | 0.68 |
| 14 | 0.345 | 0.69 |
| 15 | 0.35 | 0.70 |
| 16 | 0.355 | 0.71 |
| 17 | 0.36 | 0.72 |
| 18 | 0.365 | 0.73 |
| 19 | 0.37 | 0.74 |
| 1A | 0.375 | 0.75 |
| 1B | 0.38 | 0.76 |
| 1C | 0.385 | 0.77 |
| 1D | 0.39 | 0.78 |
| 1E | 0.395 | 0.79 |
| 1F | 0.40 | 0.80 |
| 20 | 0.405 | 0.81 |
| 21 | 0.41 | 0.82 |
| 22 | 0.415 | 0.83 |
| 23 | 0.42 | 0.84 |
| 24 | 0.425 | 0.85 |
| 25 | 0.43 | 0.86 |
| 26 | 0.435 | 0.87 |
| 27 | 0.44 | 0.88 |
| 28 | 0.445 | 0.89 |
| 29 | 0.45 | 0.90 |
| 2A | 0.455 | 0.91 |
| 2B | 0.46 | 0.92 |
| 2C | 0.465 | 0.93 |
| 2D | 0.47 | 0.94 |
| 2E | 0.475 | 0.95 |

Table 1. VID Table (continued)

| VID Hex VALUE | VR12.0 VOLTAGE (V) | VR12.5 VOLTAGE (V) |
|---------------|--------------------|--------------------|
| 2F | 0.48 | 0.96 |
| 30 | 0.485 | 0.97 |
| 31 | 0.49 | 0.98 |
| 32 | 0.495 | 0.99 |
| 33 | 0.50 | 1.00 |
| 34 | 0.505 | 1.01 |
| 35 | 0.51 | 1.02 |
| 36 | 0.515 | 1.03 |
| 37 | 0.52 | 1.04 |
| 38 | 0.525 | 1.05 |
| 39 | 0.53 | 1.06 |
| 3A | 0.535 | 1.07 |
| 3B | 0.54 | 1.08 |
| 3C | 0.545 | 1.09 |
| 3D | 0.55 | 1.10 |
| 3E | 0.555 | 1.11 |
| 3F | 0.56 | 1.12 |
| 40 | 0.565 | 1.13 |
| 41 | 0.57 | 1.14 |
| 42 | 0.575 | 1.15 |
| 43 | 0.58 | 1.16 |
| 44 | 0.585 | 1.17 |
| 45 | 0.59 | 1.18 |
| 46 | 0.595 | 1.19 |
| 47 | 0.60 | 1.20 |
| 48 | 0.605 | 1.21 |
| 49 | 0.61 | 1.22 |
| 4A | 0.615 | 1.23 |
| 4B | 0.62 | 1.24 |
| 4C | 0.625 | 1.25 |
| 4D | 0.63 | 1.26 |
| 4E | 0.635 | 1.27 |
| 4F | 0.64 | 1.28 |
| 50 | 0.645 | 1.29 |
| 51 | 0.65 | 1.30 |
| 52 | 0.655 | 1.31 |
| 53 | 0.66 | 1.32 |
| 54 | 0.665 | 1.33 |
| 55 | 0.67 | 1.34 |
| 56 | 0.675 | 1.35 |
| 57 | 0.68 | 1.36 |
| 58 | 0.685 | 1.37 |
| 59 | 0.69 | 1.38 |
| 5A | 0.695 | 1.39 |
| 5B | 0.70 | 1.40 |
| 5C | 0.705 | 1.41 |
| 5D | 0.71 | 1.42 |

Table 1. VID Table (continued)

| VID Hex VALUE | VR12.0 VOLTAGE (V) | VR12.5 VOLTAGE (V) |
|---------------|--------------------|--------------------|
| 5E | 0.715 | 1.43 |
| 5F | 0.72 | 1.44 |
| 60 | 0.725 | 1.45 |
| 61 | 0.73 | 1.46 |
| 62 | 0.735 | 1.47 |
| 63 | 0.74 | 1.48 |
| 64 | 0.745 | 1.49 |
| 65 | 0.75 | 1.50 |
| 66 | 0.755 | 1.51 |
| 67 | 0.76 | 1.52 |
| 68 | 0.765 | 1.53 |
| 69 | 0.77 | 1.54 |
| 6A | 0.775 | 1.55 |
| 6B | 0.78 | 1.56 |
| 6C | 0.785 | 1.57 |
| 6D | 0.79 | 1.58 |
| 6E | 0.795 | 1.59 |
| 6F | 0.80 | 1.60 |
| 70 | 0.805 | 1.61 |
| 71 | 0.81 | 1.62 |
| 72 | 0.815 | 1.63 |
| 73 | 0.82 | 1.64 |
| 74 | 0.825 | 1.65 |
| 75 | 0.83 | 1.66 |
| 76 | 0.835 | 1.67 |
| 77 | 0.84 | 1.68 |
| 78 | 0.845 | 1.69 |
| 79 | 0.85 | 1.70 |
| 7A | 0.855 | 1.71 |
| 7B | 0.86 | 1.72 |
| 7C | 0.865 | 1.73 |
| 7D | 0.87 | 1.74 |
| 7E | 0.875 | 1.75 |
| 7F | 0.88 | 1.76 |
| 80 | 0.885 | 1.77 |
| 81 | 0.89 | 1.78 |
| 82 | 0.895 | 1.79 |
| 83 | 0.90 | 1.80 |
| 84 | 0.905 | 1.81 |
| 85 | 0.91 | 1.82 |
| 86 | 0.915 | 1.83 |
| 87 | 0.92 | 1.84 |
| 88 | 0.925 | 1.85 |
| 89 | 0.93 | 1.86 |
| 8A | 0.935 | 1.87 |
| 8B | 0.94 | 1.88 |
| 8C | 0.945 | 1.89 |

Table 1. VID Table (continued)

| VID Hex VALUE | VR12.0 VOLTAGE (V) | VR12.5 VOLTAGE (V) |
|---------------|--------------------|--------------------|
| 8D | 0.95 | 1.90 |
| 8E | 0.955 | 1.91 |
| 8F | 0.96 | 1.92 |
| 90 | 0.965 | 1.93 |
| 91 | 0.97 | 1.94 |
| 92 | 0.975 | 1.95 |
| 93 | 0.98 | 1.96 |
| 94 | 0.985 | 1.97 |
| 95 | 0.99 | 1.98 |
| 96 | 0.995 | 1.99 |
| 97 | 1.00 | 2.00 |
| 98 | 1.005 | 2.01 |
| 99 | 1.01 | 2.02 |
| 9A | 1.015 | 2.03 |
| 9B | 1.02 | 2.04 |
| 9C | 1.025 | 2.05 |
| 9D | 1.03 | 2.06 |
| 9E | 1.035 | 2.07 |
| 9F | 1.04 | 2.08 |
| A0 | 1.045 | 2.09 |
| A1 | 1.05 | 2.10 |
| A2 | 1.055 | 2.11 |
| A3 | 1.06 | 2.12 |
| A4 | 1.065 | 2.13 |
| A5 | 1.07 | 2.14 |
| A6 | 1.075 | 2.15 |
| A7 | 1.08 | 2.16 |
| A8 | 1.085 | 2.17 |
| A9 | 1.09 | 2.18 |
| AA | 1.095 | 2.19 |
| AB | 1.10 | 2.20 |
| AC | 1.105 | 2.21 |
| AD | 1.11 | 2.22 |
| AE | 1.115 | 2.23 |
| AF | 1.12 | 2.24 |
| B0 | 1.125 | 2.25 |
| B1 | 1.13 | 2.26 |
| B2 | 1.135 | 2.27 |
| B3 | 1.14 | 2.28 |
| B4 | 1.145 | 2.29 |
| B5 | 1.15 | 2.30 |
| B6 | 1.155 | 2.31 |
| B7 | 1.16 | 2.32 |
| B8 | 1.165 | 2.33 |
| B9 | 1.17 | 2.34 |
| BA | 1.175 | 2.35 |
| BB | 1.18 | 2.36 |

Table 1. VID Table (continued)

| VID Hex VALUE | VR12.0 VOLTAGE (V) | VR12.5 VOLTAGE (V) |
|---------------|--------------------|--------------------|
| BC | 1.185 | 2.37 |
| BD | 1.19 | 2.38 |
| BE | 1.195 | 2.39 |
| BF | 1.20 | 2.40 |
| C0 | 1.205 | 2.41 |
| C1 | 1.21 | 2.42 |
| C2 | 1.215 | 2.43 |
| C3 | 1.22 | 2.44 |
| C4 | 1.225 | 2.45 |
| C5 | 1.23 | 2.46 |
| C6 | 1.235 | 2.47 |
| C7 | 1.24 | 2.48 |
| C8 | 1.245 | 2.49 |
| C9 | 1.25 | 2.50 |
| CA | 1.255 | n/a |
| CB | 1.26 | n/a |
| CC | 1.265 | n/a |
| CD | 1.27 | n/a |
| CE | 1.275 | n/a |
| CF | 1.28 | n/a |
| D0 | 1.285 | n/a |
| D1 | 1.29 | n/a |
| D2 | 1.295 | n/a |
| D3 | 1.30 | n/a |
| D4 | 1.305 | n/a |
| D5 | 1.31 | n/a |
| D6 | 1.315 | n/a |
| D7 | 1.32 | n/a |
| D8 | 1.325 | n/a |
| D9 | 1.33 | n/a |
| DA | 1.335 | n/a |
| DB | 1.34 | n/a |
| DC | 1.345 | n/a |
| DD | 1.35 | n/a |

Table 1. VID Table (continued)

| VID Hex VALUE | VR12.0 VOLTAGE (V) | VR12.5 VOLTAGE (V) |
|---------------|--------------------|--------------------|
| DE | 1.355 | n/a |
| DF | 1.36 | n/a |
| E0 | 1.365 | n/a |
| E1 | 1.37 | n/a |
| E2 | 1.375 | n/a |
| E3 | 1.38 | n/a |
| E4 | 1.385 | n/a |
| E5 | 1.39 | n/a |
| E6 | 1.395 | n/a |
| E7 | 1.40 | n/a |
| E8 | 1.405 | n/a |
| E9 | 1.41 | n/a |
| EA | 1.415 | n/a |
| EB | 1.42 | n/a |
| EC | 1.425 | n/a |
| ED | 1.43 | n/a |
| EE | 1.435 | n/a |
| EF | 1.44 | n/a |
| F0 | 1.445 | n/a |
| F1 | 1.45 | n/a |
| F2 | 1.455 | n/a |
| F3 | 1.46 | n/a |
| F4 | 1.465 | n/a |
| F5 | 1.47 | n/a |
| F6 | 1.475 | n/a |
| F7 | 1.48 | n/a |
| F8 | 1.485 | n/a |
| F9 | 1.49 | n/a |
| FA | 1.495 | n/a |
| FB | 1.50 | n/a |
| FC | 1.505 | n/a |
| FD | 1.51 | n/a |
| FE | 1.515 | n/a |
| FF | 1.52 | n/a |

7.3.11 PWM and $\overline{\text{SKIP}}$ Signals

The PWM and $\overline{\text{SKIP}}$ -NVM signals are output from the controller to drive the TI smart power stages. Both signals are 3.3-V logic based. The PWM signal is logic high to turn on the high-side MOSFET and logic low to turn on the low-side MOSFET. When both high-side and low-side MOSFETs are expected to be OFF, the PWM signal is driven to tri-state condition (1.7 V). The $\overline{\text{SKIP}}$ -NVM pin is asserted low during the soft-start period.

7.3.12 TSEN (Thermal Sense) Pin

TI smart power stage (ex: CSD95372BQ5MC) senses the die temperature and sends out the temperature information as a voltage through the TAO pin. In a multi-phase application, the TAO pin of the TI smart power stages are connected and then tied to the TSEN pin of the TPS53647 device. In this case, the device reports the temperature of the hottest power stage. The reported temperature can be calculated as shown in Equation 4.

$$\text{TEMP} = \frac{(V_{\text{TSEN}} - 0.6)}{0.008}$$

where

- TEMP is the sensed temperature in °C
- V_{TSEN} is the voltage at TSEN pin

(4)

NOTE

The maximum temperature that can be sensed is 127.9 °C. If the TSEN voltage (V_{TSEN}) is higher than the voltage associated to 127.9 °C, the device continues to report 127.9 °C.

TSEN signal is also used as an indicator for power stage fault. When an internal fault occurs in the TI smart power stage (CSD95372BQ5MC), the power stage pulls the TAO pin high. In the default configuration, if the TSEN voltage is higher than 2.5 V, the TPS53647 device senses the fault and turns off both the high-side and the low-side MOSFETS. There is also an option to disable power stage fault as described in MFR_SPECIFIC_07[3].

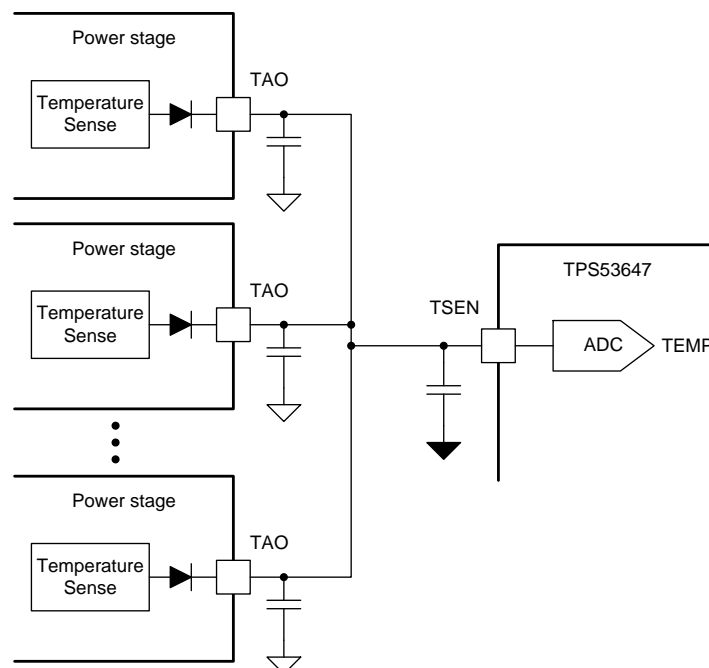


Figure 16. Temperature Sense

7.3.13 RESET Function

During adaptive voltage scaling (AVS) operation, the voltage may become falsely adjusted to be out of ASIC operating range. The RESET function returns the voltage to the VBOOT voltage. When the voltage is out of ASIC operating range, the ASIC issues a RESET signal to the TPS53647 device, as shown in Figure 17. The device senses this signal and after a delay of greater than 1 μs, it sets an internal RESET_FAULT signal and sets VOUT_COMMAND to VBOOT. The device pulls the output voltage to the VBOOT level with the slew rate set by SLEW-MODE pin, as shown in Figure 18.

When the RESET pin signal goes high, the internal RESET_FAULT signal goes low.

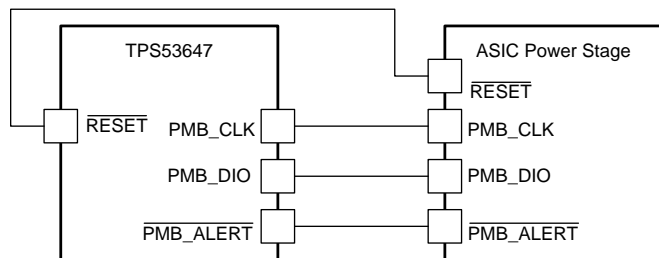


Figure 17. RESET Pin Connection

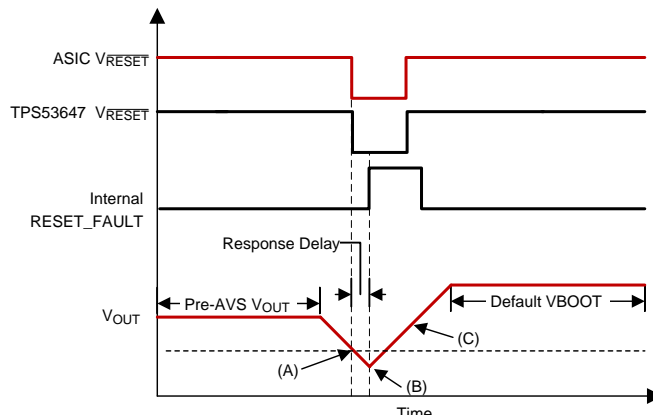


Figure 18. Reset Function

7.3.14 Input UVLO

The TPS53647 device continuously monitors the input voltage through the VIN pin. If the input voltage is lower than the UVLO low threshold, the device turns off. If VIN rises higher than the UVLO high threshold, the controller turns on again (if both V5 and ENABLE are high). The hysteresis is approximately 1.05 V.

Table 2. Input Undervoltage Lockout (UVLO)

| VIN UVLO SETTING | TURN-ON VOLTAGE (V) | TURN-OFF VOLTAGE (V) |
|---------------------------------|---------------------|----------------------|
| MFR_SPEC_16[1:0] = 00 | 4.5 | 3.5 |
| MFR_SPEC_16[1:0] = 01 (Default) | 7.25 | 6.25 |
| MFR_SPEC_16[1:0] = 10 | 9.0 | 8.0 |
| MFR_SPEC_16[1:0] = 11 | 10.3 | 9.3 |

7.3.15 V5 Pin Undervoltage Lockout (UVLO)

The TPS53647 device also monitors V5 pin voltage. If the voltage is lower than V_{V5UVLOL} (4.05 V typical), the controller turns off. If V5 voltage comes back to be higher than V_{V5UVLOH} (4.25 V typical), the controller turns back on (if both VIN and ENABLE are high).

7.3.16 Output Undervoltage Protection (UVP)

The output undervoltage protection in the TPS53647 device is called tracking UVP. When the output voltage drops below (VDAC – V_{DROOP} – V_{RDYL}), the controller drives the PWM into a tri-state condition so that both high-side and low-side MOSFETs turn off. After a hiccup delay (22-ms typical), the device attempts to restart to VBOOT voltage. If the UVP condition continues, the UVP occurs again and the process repeats.

7.3.17 Overvoltage Protection (OVP)

The OVP condition is detected when the output voltage $V_{OUT} > V_{DAC} +$ tracking OVP offset (V_{OVPT5} for VR12.5 or V_{OVPT0} for VR12.0), which is called tracking OVP. In this case the controller drives the VR_RDY pin to inactive (low state) and drives all PWM signals to logic low which turns on the low-side MOSFET to discharge the output. However the OVP threshold is blanked during a V_{DAC} change. In order to continually protect the load, there is second OVP level (fixed OVP). The second OVP level is fixed at V_{OVPH5} (VR12.5) or V_{OVPH0} (VR12.0) is active during V_{DAC} change. If the fixed OVP condition is detected, the device drives the VR_RDY pin to inactive (logic low) and drives the PWM signals to logic low in order to turn on the low-side MOSFET. The controller remains in this state until the ENABLE or V5 is re-cycled.

When ENABLE is low, and output voltage is higher than V_{OVFPF} (2.75 V typical), the OVP condition is detected, which is called Pre-bias OVP. The device then drives the PWM signals to logic low. The device latches the pre-bias OVP. The latch can be cleared only by recycling V5.

7.3.18 Overcurrent Limit (OCL) and Overcurrent Protection (OCP)

The TPS53647 device includes a valley-current-based limit function by using a per-phase OCL comparator. A resistor connected between the OCL-R pin and the VREF pin generates the OCL comparison threshold.

Using the valley current limit, the OCL current level can be selected using [Equation 5](#). To set the per-phase OCL threshold, subtract half of the ripple current from the maximum average current and select the OCL threshold specified in the table equal or slight lower than I_{OCL} .

$$I_{OCL} = K \times \left(\frac{I_{MAX}}{n} \right) - \left(\frac{I_{RIPPLE}}{2} \right)$$

where

- K is the maximum operating margin percentage
 - n is the number of active phases
 - I_{RIPPLE} is the ripple current
- (5)

This instantaneous current sense voltage V_{CSPX} is compared to the OCL threshold. If the current sense voltage at OCL comparator goes above the OCL threshold, the device delays the next ON pulse until the current sense voltage drops below the OCL threshold. In this case, the output voltage continues to drop until the UVP threshold is reached.

Another overcurrent protection (OCP) is based on the current sensed through IMON pin of the device. When the digitized IMON is higher than OC_FAULT_LIMIT (1.25x I_{MAX} by default), the controller turns off both high-side and low-side MOSFETS and enters into hiccup mode until the overcurrent condition is removed.

7.3.19 Over Temperature Protection (OTP)

When the sensed temperature through TSEN pin is higher than the over temperature fault threshold OTP_{THLD} (125°C by default), the controller turns off high-side and low-side MOSFETS. The power stages cool down and TSEN voltage drops. When the sensed temperature is 15°C (OTP_{HYS}) lower than the over temperature fault threshold, the controller restarts to the VBOOT voltage.

7.3.20 $\overline{VR_HOT}$ and $\overline{VR_FAULT}$ Indication

When the sensed temperature is higher than the maximum temperature specification T_{MAX} , (110°C by default), the device pulls the $\overline{VR_HOT}$ pin low. This adjustment provides a warning signal to the load.

NOTE

Only the PMBus interface can establish the maximum temperature (T_{MAX}) setting. NVM does not store this setting.

$\overline{VR_FAULT}$ is used as an indication of severe fault. $\overline{VR_FAULT}$ will be pulled low when the below fault occurs:

- Input Overcurrent Fault
- Over Temperature Fault
- Overvoltage Fault
- Power Stage Fault ($V_{TSEN} > 2.5V$)

7.4 Device Functional Modes

Table 3. Maximum Operating Phase Numbers

| CSP1 | CSP2 | CSP3 | CSP4 | MAXIMUM ACTIVE PHASES |
|-------|-------|-------|-------|-----------------------|
| IOUT1 | V3R3 | n/a | n/a | 1 |
| IOUT1 | IOUT2 | V3R3 | n/a | 2 |
| IOUT1 | IOUT2 | IOUT3 | V3R3 | 3 |
| IOUT1 | IOUT2 | IOUT3 | IOUT4 | 4 |

7.5 Programming

7.5.1 User Selections

When $\overline{\text{SKIP-NVM}}$ pin is connected to GND with $\leq 20\text{-k}\Omega$ resistor, the resistors connected to $\overline{\text{O-USR}}$, F-IMAX, SLEW-MODE, OCL-R, VBOOT and ADDR-TRISE determine the associated configurations. If $\overline{\text{SKIP-NVM}}$ pin is connected to GND with $\geq 100\text{-k}\Omega$ resistor, these configurations are determined by NVM settings. Please note the address setting is determined only by the resistors on the ADDR-TRISE pin and cannot be set by NVM. When the V3R3 pin powers up, the following information is latched for normal operations, and can be changed via the PMBus interface. The [Electrical Characteristics](#) table defines the values of the selections.

In general, the NVM provides more selection than pinstrap configurations. For example, pinstrap for switching frequency offers 3-bit, 8 selections, which correlates to MFR_SPEC_12<6:4>. Alternatively, NVM provides 4-bit, 16 selections.

7.5.1.1 Switching Frequency

The resistor from F-IMAX pin to GND sets the switching frequency from 300 kHz to 1 MHz. See the [Electrical Characteristics](#) table for the resistor settings corresponding to each frequency selection. Please note that the operating frequency is a quasi-fixed frequency in the sense that the ON time is fixed based on the input voltage (at the VIN pin) and output voltage (set by VID). The OFF time varies based on various factors such as load and power-stage components.

7.5.1.2 IMAX Information

The max current information of the load(IMAX) can be set by the voltage on the F-IMAX pin. See the [Electrical Characteristics](#) table for the details. The default OCP fault trigger level is 125% of IMAX.

7.5.1.3 Boot Voltage

The boot voltage is the controller voltage at start-up to before any output voltage change by the VOUT_COMMAND. If there is no further output voltage adjustment, the output voltage remains at the boot voltage level.

The resistor from the VBOOT pin to GND and the voltage level on this pin set 7 high bits of the boot voltage. The lowest bit is set by the ADDR-TRISE pin. See the [Electrical Characteristics](#) table for the resistor settings corresponding to boot voltage selections.

7.5.1.4 Per-Phase Overcurrent Limit (OCL) Level

The resistor from the OCL-R pin to GND and the voltage level on this pin set the per-phase OCL level. See the [Electrical Characteristics](#) table for the details.

7.5.1.5 Overshoot Reduction (OSR) and Undershoot Reduction (USR) Levels

The resistor from the O-USR pin to GND and the voltage on O-USR pin set the OSR and USR levels. See the [Electrical Characteristics](#) table for details.

Programming (continued)

7.5.1.6 Slew Rate Selection

The V_{OUT} change slew rate is set by the resistor from the SLEW-MODE pin to GND. See the [Electrical Characteristics](#) table for details.

7.5.1.7 Mode Selections

The TPS53647 device supports different operating modes, including VR12.0/VR12.5, phase interleaving mode, dynamic phase shedding, and zero load-line. The voltage on SLEW-MODE pin sets the desired operating modes.

7.5.1.8 Soft Start Slew Rate and PMBus Addresses

The resistor from the ADDR-TRISE pin to GND and the voltage on ADDR-TRISE pin set the slew rate of soft start and the address of PMBus interface. See the [Electrical Characteristics](#) table for details.

7.5.1.9 Ramp Selection

The internal ramp can be set by the voltage on the OCL-R pin. See the [Electrical Characteristics](#) table for details.

7.5.1.10 Maximum Active Phase Numbers

The maximum active phase numbers can be selected by connecting CSP2, CSP3 or CSP4 to the V3R3. See [Table 3](#) for details. The device latches this configuration when V3R3 powers up.

Programming (continued)

7.5.1.11 Pinstrap Mode Settings

summarizes the functions controlled with pin-strap resistors. For details of each setting please refer to the [Electrical Characteristics](#) table. For more information on VID encoding see the [VID](#) section.

Table 4. Pinstrap Mode Summary

| FUNCTION | PIN | | DESCRIPTION |
|----------------------|------------|-----|---|
| | NAME | NO. | |
| Slew Rate | SLEW-MODE | 29 | Voltage divider to VREF pin. A pin-strap resistor ($R_{\text{SLEW-MODE}}$) connected between this pin and GND sets one of eight possible slew rates. |
| Mode | SLEW-MODE | 29 | The voltage level ($V_{\text{SLEW-MODE}}$) sets 4-bit operation modes. -Bit 7 for DAC mode (1 for VR12.0; 0 for VR12.5). -Bit 6 for the 4-phase interleaving mode (1 for 1/3 and 2/4 two phase interleaving; 0 for 4 phase interleaving individually). -Bit 4 for enabling dynamic phase add or drop (1 for enable; 0 for disable). -Bit 3 sets zero load-line (1 for zero load-line; 0 for non-zero load-line) The device latches these settings when V3R3 powers up. |
| Overshoot reduction | O-USR | 30 | Voltage divider to VREF pin. A pin-strap resistor ($R_{\text{O-USR}}$) connected between this pin and GND selects 1 of 7 OSR thresholds or OFF. |
| Undershoot reduction | O-USR | 30 | The voltage level ($V_{\text{O-USR}}$) sets 1 of 7 USR levels or OFF. The device latches these settings when V3R3 powers up. |
| Voltage boot | VBOOT | 31 | Voltage divider to VREF pin. A pin-strap resistor (R_{VBOOT}) connected between this pin and GND sets 3 bits (B[3:1]). The voltage level (V_{BOOT}) sets 4 bits (B[7:4]). The total 7 bit sets 7 of 8 bits of VID of VBOOT(B[7:1]). The device latches these settings when V3R3 powers up. |
| | ADDR-TRISE | 28 | Voltage divider to VREF pin. A pin-strap resistor ($R_{\text{ADDR-TRISE}}$) connected between this pin and GND sets 3-bits. -Bit 2 and Bit 1 set the rise slew rate (TRISE). -Bit 0 Selects the LSB of BOOT voltage. The voltage ($V_{\text{ADDR-TRISE}}$) sets 4 bits PMBus address. The device latches these settings when V3R3 powers up. |
| Rise slew rate | ADDR-TRISE | 28 | Voltage divider to VREF pin. A pin-strap resistor ($R_{\text{ADDR-TRISE}}$) connected between this pin and GND sets 3-bits. -Bit 2 and Bit 1 set the rise slew rate (TRISE). -Bit 0 Selects the LSB of BOOT voltage. -The voltage ($V_{\text{ADDR-TRISE}}$) sets 4 bits PMBus address. The device latches these settings when V3R3 powers up |
| Frequency | F-IMAX | 32 | Voltage divider to VREF pin. A pin-strap resistor ($R_{\text{F-IMAX}}$) connected between this pin and GND sets the operating frequency of the controller. |
| Current limit | F-IMAX | 32 | The voltage level ($V_{\text{F-IMAX}}$) sets the maximum operating current of the converter. The IMAX value is an 8-bit A/D where $V_{\text{F-IMAX}} = V_{\text{VREF}} \times \text{IMAX} / 255$. Both are latched at V3R3 power-up. |
| Overcurrent limit | OCL-R | 1 | Voltage divider to VREF pin. A pin-strap resistor ($R_{\text{OCL-R}}$) connected between this pin and GND and the voltage level ($V_{\text{OCL-R}}$) selects one of 16 OCL levels (per phase current-limit). |
| Ramp | OCL-R | 1 | $V_{\text{OCL-R}}$ sets one of four RAMP levels. The device latches these settings when the V3R3 pin powers up. |

7.5.1.12 NVM Default Settings

Table 5 lists the default settings in NVM where the shaded rows denote register functions that are configured by associated pins in pinstrap mode.

Table 5. NVM Default Settings

| REGISTER | FUNCTION | DEFAULT VALUES | | | | | | | | |
|-----------------------|----------------------|----------------|-------|-------|-------|-------|-------|-------|-------|---|
| | | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | |
| MFR_SPECIFIC_13 [2:0] | Slew Rate | — | | | | | 0 | 0 | 1 | |
| MFR_SPECIFIC_13 [7:3] | Mode | 1 | 0 | 0 | 0 | 1 | — | | | |
| MFR_SPECIFIC_09 [2:0] | OSR | — | | | | | 1 | 1 | 1 | |
| MFR_SPECIFIC_09 [6:4] | USR | — | 1 | 1 | 1 | — | | | | |
| MFR_SPECIFIC_11 [7:0] | VBOOT | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | |
| MFR_SPECIFIC_12 [1:0] | TRISE | — | | | | | | 0 | 0 | |
| MFR_SPECIFIC_12[7:4] | Frequency | 0 | 0 | 1 | 0 | — | | | | |
| MFR_SPECIFIC_10 [7:0] | IMAX | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | |
| MFR_SPECIFIC_00 [3:0] | OCL | — | | | | 1 | 0 | 0 | 0 | |
| MFR_SPECIFIC_14[2:0] | RAMP | — | | | | | 1 | 1 | 0 | |
| MFR_SPECIFIC_07 [0] | Soft-start slew rate | — | | | | | | | 0 | |
| MFR_SPECIFIC_07 [1] | OSR_TRISTATE | — | | | | | | 0 | — | |
| MFR_SPECIFIC_07 [2] | SLEW_FAST | — | | | | | 0 | — | | |
| MFR_SPECIFIC_16 [1:0] | VIN UVLO | — | | | | | | 0 | 1 | |
| MFR_SPECIFIC_15 [3] | DPS_TH_LOW | — | | | | 0 | — | | | |
| MFR_SPECIFIC_15 [2:0] | DPS_TH_HIGH | — | | | | | 0 | 0 | 1 | |
| MFR_SPECIFIC_22 [2:0] | UV OFFSET | — | | | | | 0 | 1 | 1 | |
| MFR_SPECIFIC_05 [7:0] | VOUT OFFSET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| MFR_ID | — | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | |
| MFR_MODEL | | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | |
| MFR_REVISION [3:0] | | — | | | | | 0 | 0 | 0 | 0 |
| MFR_DATE | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

7.5.1.13 4-Phase Application

Figure 19 shows the diagram for a 4-Phase application with smart power stage (CSD95372BQ5MC) and pinstrap configurations. Figure 20 shows the diagram for a 4-Phase application with smart power stage (CSD95372BQ5MC) and NVM configurations.

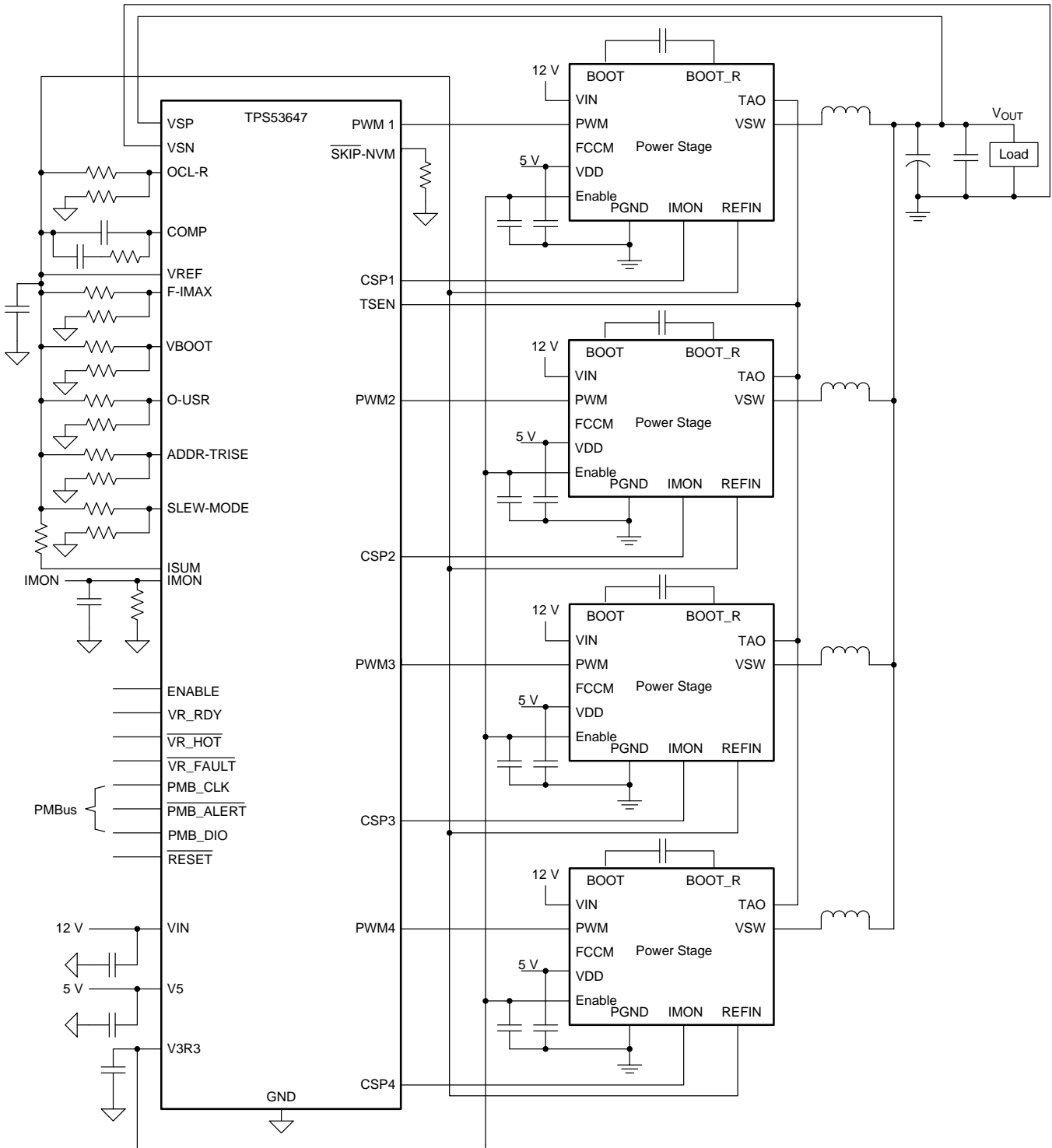


Figure 19. 4-Phase Application with Smart Power Stage (CSD95372BQ5MC)

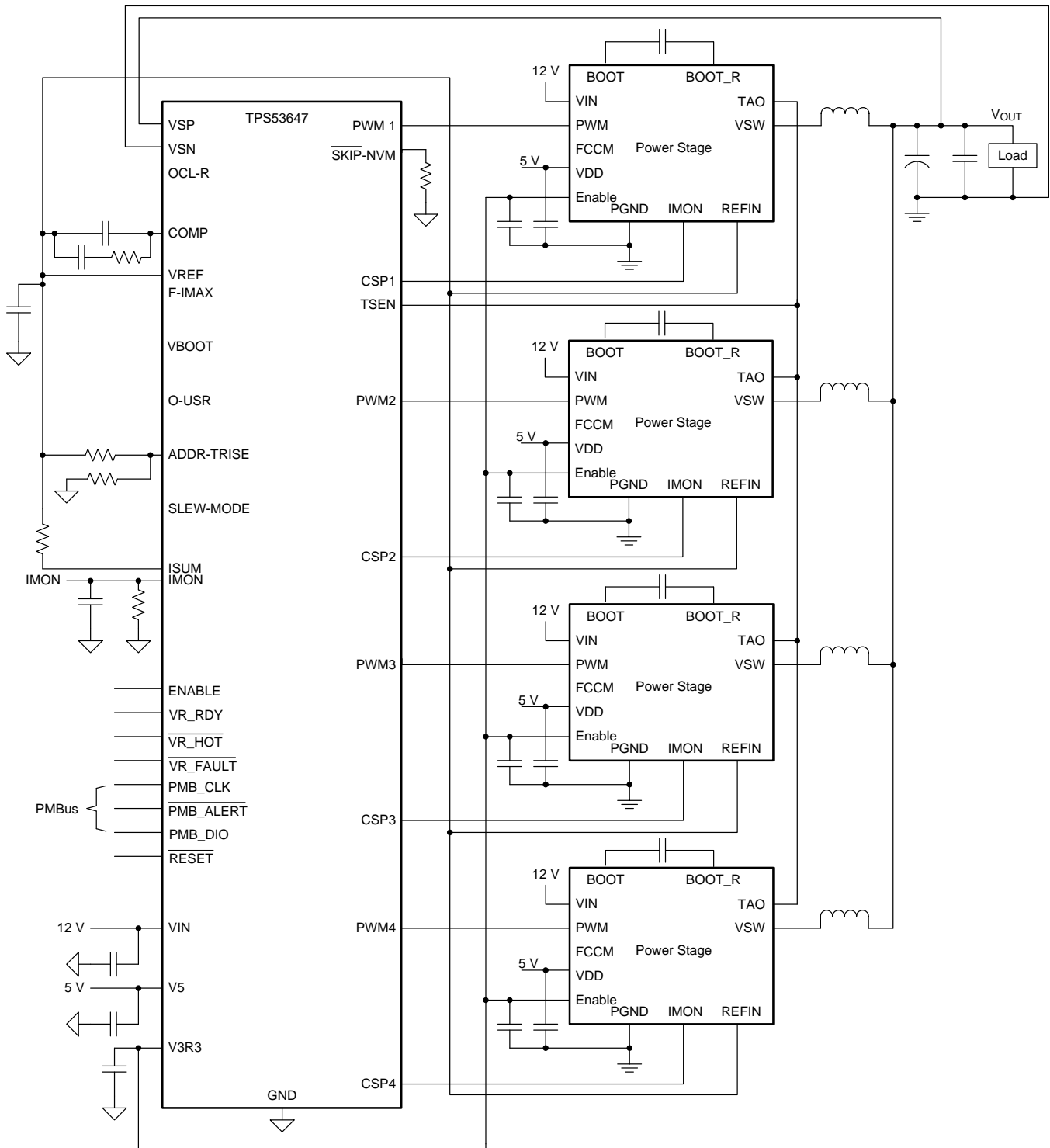


Figure 20. 4-Phase Application with Smart Power Stage (CSD95372BQ5MC) and NVM Configuration

7.5.2 Supported Protections and Fault Reports

The TPS53647 device supports different types of fault protections, and the warning or fault reports can be found in the corresponding PMBus registers. The TPS53647 also supports $\overline{\text{VR_FAULT}}$ to indicate catastrophic faults to the system. If the fault causes the controller to latch-off, then V5 or EN re-cycling is required to clear the latched faults. Only V5 recycling can clear PRE_OVF.

Table 6. Supported Protections and Fault Reports

| FAULT NAME | DESCRIPTIONS | LATCH-OFF | ALERT | REPORT |
|--------------------|--|-----------|---|--------|
| VOLTAGE | | | | |
| PRE_OVF | $V_{OUT} > V_{OVPPF}$ | Y | $\overline{VR_FAULT}$ $\overline{PMB_ALERT}$ | PMBus |
| OVF | $V_{OUT} > VID + V_{OVPT5/0}$ OR $V_{OUT} > V_{OVPF5}$ | Y | $\overline{VR_FAULT}$ $\overline{PMB_ALERT}$ | PMBus |
| UVF | $V_{OUT} < VID - V_{RDYL} - V_{DROOP}$ | N | $\overline{PMB_ALERT}$ | PMBus |
| VIN_OVF | $V_{VIN} > VIN_OV_FAULT_LIMIT$ when the controller is enabled | N | $\overline{PMB_ALERT}$ | PMBus |
| VIN_UVF | $V_{VIN} < V_{INUVLO}$ when the controller is enabled | N | $\overline{PMB_ALERT}$ | PMBus |
| CURRENT | | | | |
| OCF | $I_{OUT} \geq I_{OUT_OC_FAULT_LIMIT}$ | N | $\overline{PMB_ALERT}$ | PMBus |
| OCW | $I_O \geq I_{OUT_OC_WARN_LIMIT}$ | N | $\overline{PMB_ALERT}$ | PMBus |
| IOCF | $I_{IN} \geq I_{IN_OC_FAULT_LIMIT}$ | Y | $\overline{VR_FAULT}$ $\overline{PMB_ALERT}$ | PMBus |
| IOCW | $I_{IN} \geq I_{IN_OC_WARN_LIMIT}$ | N | $\overline{PMB_ALERT}$ | PMBus |
| TEMPERATURE | | | | |
| OTF | $T_{sen} \geq OT_FAULT_LIMIT$ | N | $\overline{VR_FAULT}$ $\overline{PMB_ALERT}$ | PMBus |
| OTW | $T_{sen} \geq OT_WARNING_LIMIT$ | N | $\overline{PMB_ALERT}$ | PMBus |
| TMAX_F | $T_{sen} \geq T_{MAX}$ | N | $\overline{VR_HOT}$ | |
| TS_VREFF | TSEN pin short to VREF | Y | $\overline{PMB_ALERT}$ | PMBus |
| TS_GND | TSEN pin short to GND | Y | $\overline{PMB_ALERT}$ | PMBus |
| TS_PS | $V_{TSEN} > 2.5 V$ | Y | $\overline{VR_FAULT}$ $\overline{PMB_ALERT}$ | PMBus |

7.5.3 Supported PMBus Address and Commands Summary

7.5.3.1 Address Selection

The TPS53647 device has a dedicated pin (ADDR-TRISE) for determining the address for the PMBus communication. The device supports a total of 16 possible addresses. See the [Electrical Characteristics](#) table for details.

7.5.3.2 Commands Summary

The TPS53647 device supports only PMBus command sets listed in [Table 7](#). In pinstrap mode, the default state of all the configuration registers (shaded rows in [Table 5](#)) should be detected from pinstrap settings, but users can overwrite the settings via PMBus after the power-up sequence is complete. In NVM mode, the default values can be found in the register descriptions.

Table 7. Supported PMBus Commands

| CODE | COMMAND NAME | TYPE | DESCRIPTION: PMBus Command | FACTORY DEFAULT VALUE |
|------|------------------------|-----------|--|-----------------------|
| 01h | OPERATION | R/W Byte | Turn the unit on and off in conjunction with the input from the ENABLE pin. Set the output voltage to the upper or lower MARGIN voltages. | 00h |
| 02h | ON_OFF_CONFIG | R/W Byte | Configures the combination of CONTROL pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when power is applied. | 17h |
| 03h | CLEAR_FAULTS | Send Byte | Clears any faults bits that have been set if the fault is no longer present. At the same time, simultaneously clears all bits in all status registers and negates the PMB_ALERT signal output if it is asserted. | NONE |
| 10h | WRITE_PROTECT | R/W Byte | Used to control writing to the PMBus device. Can be used to prevent unwanted writes to the device. | 00h |
| 11h | STORE_DEFAULT_ALL | Send Byte | Store the settings to the NVM. | NONE |
| 12h | RESTORE_DEFAULT_ALL | Send Byte | Restore the settings from the NVM. | NONE |
| 19h | CAPABILITY | Read Byte | Provides a way for the host to determine the capabilities of the PMBus device. | B0h |
| 20h | VOUT_MODE | Read Byte | Read-Only VOUT Mode Indicator. | 21h |
| 21h | VOUT_COMMAND | R/W Word | Causes the device to set its output voltage to the commanded value. | VBOOT |
| 24h | VOUT_MAX | R/W Word | Sets the upper limit on the output voltage the unit can command regardless of any other commands or combinations. Provides a safeguard against a user accidentally setting the output voltage to a possibly destructive level. | 00FFh |
| 25h | VOUT_MARGIN_HIGH | R/W Word | Loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to "Margin High." | 0000h |
| 26h | VOUT_MARGIN_LOW | R/W Word | Loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to "Margin Low." | 0000h |
| 39h | IOUT_CAL_OFFSET | R/W Word | compensate for offset errors in READ_VOUT command. | 0000h |
| 41h | VOUT_OV_FAULT_RESPONSE | Read Byte | Instructs the device on what action to take in response to an output overvoltage fault. | 80h |
| 45h | VOUT_UV_FAULT_RESPONSE | Read Byte | Instructs the device on what action to take in response to an output undervoltage fault. | BAh |
| 46h | IOUT_OC_FAULT_LIMIT | R/W Word | Sets the value of the output current, in amperes, that causes the overcurrent detector to indicate an overcurrent fault condition. | 125% IMAX |
| 47h | IOUT_OC_FAULT_RESPONSE | Read Byte | Instructs the device on what action to take in response to an output overcurrent fault. | FAh |
| 4Ah | IOUT_OC_WARN_LIMIT | R/W Word | Sets the value of the output current that causes an output overcurrent warning condition. | IMAX |
| 4Fh | OT_FAULT_LIMIT | R/W Word | Sets the temperature, in degree Celsius, that causes an over-temperature fault condition. | 007Dh |
| 50h | OT_FAULT_RESPONSE | Read Byte | Instructs the device on what action to take in response to an output over-temperature fault. | F8h |
| 51h | OT_WARN_LIMIT | R/W Word | Sets the temperature, in degrees Celsius, that causes an over-temperature warning condition. | 005Fh |
| 55h | VIN_OV_FAULT_LIMIT | R/W Word | Sets the input voltage, in volts, that causes an overvoltage fault condition. | 000Fh |
| 5Bh | IIN_OC_FAULT_LIMIT | R/W Word | Sets the input current, in amperes, that causes an overcurrent fault condition. | 00FFh |

Table 7. Supported PMBus Commands (continued)

| CODE | COMMAND NAME | TYPE | DESCRIPTION: PMBus Command | FACTORY DEFAULT VALUE |
|------|-----------------------|------------|--|------------------------------------|
| 5Ch | IIN_OC_FAULT_RESPONSE | Read Byte | Instructs the device on what action to take in response to an input overcurrent fault. | C0h |
| 5Dh | IIN_OC_WARN_LIMIT | R/W Word | Sets the input current, in amperes, that causes an overcurrent warning condition. | 0019h |
| 78h | STATUS_BYTE | Read Byte | Single byte status indicator | Dependent on the Startup Condition |
| 79h | STATUS_WORD | Read Word | Full 2-byte status indicator | Dependent on the Startup Condition |
| 7Ah | STATUS_VOUT | Read Byte | Output voltage fault status detail | Dependent on the Startup Condition |
| 7Bh | STATUS_IOUT | Read Byte | Output current fault status detail | Dependent on the Startup Condition |
| 7Ch | STATUS_INPUT | Read Byte | Input voltage and current fault status detail | Dependent on the Startup Condition |
| 7Dh | STATUS_TEMPERATURE | Read Byte | Temperature fault status detail | Dependent on the Startup Condition |
| 7Eh | STATUS_CML | Read Byte | Communication, memory, and logic fault status detail | Dependent on the Startup Condition |
| 80h | STATUS_MFR_SPECIFIC | Read Byte | Manufacturer specific fault status detail | Dependent on the Startup Condition |
| 88h | READ_VIN | Read Word | Read input voltage, in volts. | |
| 89h | READ_IIN | Read Word | Read input current, in amperes. | |
| 8Bh | READ_VOUT | Read Word | Read output voltage, in volts. | |
| 8Ch | READ_IOUT | Read Word | Read output current, in amperes. | |
| 8Dh | READ_TEMPERATURE_1 | Read Word | Read temperature, in degrees Celsius. | |
| 96h | READ_POUT | Read Word | Read output power, in watts. | |
| 97h | READ_PIN | Read Word | Read input power, in watts. | |
| 98h | PMBUS_REVISION | Read Byte | PMBus Revision Information | 11h |
| 99h | MFR_ID | Read Block | Loads the unit with the text character that contains the manufacturer's ID. | 5401h |
| 9Ah | MFR_MODEL | Read Block | Loads the unit with the text character that contains the model number of the manufacturer. | 4701h |
| 9Bh | MFR_REVISION | Read Block | Loads the unit with the text character that contains the revision number of the manufacturer. | |
| 9Dh | MFR_DATE | Read Block | Loads the unit with the text character that contains the device's date of manufacture. | |
| A4h | MFR_VOUT_MIN | R/W Word | Sets a low limit on the output voltage that the device can command regardless of any other commands or combinations. (VID data format) | 0000h |
| D0h | MFR_SPECIFIC_00 | R/W Byte | Selects the threshold for the per-phase current limit. (Fixed at PMBus control) | Pin strap: OCL-R pin NVM: 08h |
| D1h | MFR_SPECIFIC_01 | R/W Byte | Selects the averaging time for telemetry reporting. | 50h |
| D4h | MFR_SPECIFIC_04 | Read Word | Returns the actual, measured output voltage in volts. | |
| D5h | MFR_SPECIFIC_05 | R/W Byte | Used to trim the output voltage. | NVM: 00h |
| D7h | MFR_SPECIFIC_07 | R/W Byte | Additional functional bits setting. | NVM: 02h |
| D8h | MFR_SPECIFIC_08 | R/W Byte | Sets the droop as a percentage of the loadline. | 04h |
| D9h | MFR_SPECIFIC_09 | R/W Byte | Sets the threshold for OSR and USR control. | Pin strap: O-USR pin NVM: 77h |

Table 7. Supported PMBus Commands (continued)

| CODE | COMMAND NAME | TYPE | DESCRIPTION: PMBus Command | FACTORY DEFAULT VALUE |
|------|-----------------|-----------|---|---|
| DAh | MFR_SPECIFIC_10 | R/W Byte | Sets the maximum operating current, I _{MAX} . | Pin strap: F-IMAX pin NVM: 78h |
| DBh | MFR_SPECIFIC_11 | R/W Byte | Sets the boot voltage, V _{BOOT} . | Pin strap: VBOOT pin NVM: 97h |
| DCh | MFR_SPECIFIC_12 | R/W Byte | Sets the switching frequency and the rise time (t _{RISE}) settings. | Pin strap: F-IMAX and ADDR-TRISE pins NVM: 20h |
| DDh | MFR_SPECIFIC_13 | R/W Byte | Sets the slew rate and other operation modes. | Pin strap: SLEW-MODE pin NVM: 89h |
| DEh | MFR_SPECIFIC_14 | R/W Byte | Sets the ramp amplitude in mV. | Pin strap: OCL-R pin NVM: 06h |
| DFh | MFR_SPECIFIC_15 | R/W Byte | Sets the threshold for dynamic phase shedding as a percentage of the OCL. | NVM: 01h |
| E0h | MFR_SPECIFIC_16 | R/W Byte | Sets the threshold for the input voltage UVLO. | NVM: 01h |
| E4h | MFR_SPECIFIC_20 | R/W Byte | Sets the maximum number of operational phase numbers on the fly. | Hardware Specific |
| FCh | MFR_SPECIFIC_44 | Read Word | Returns DEVICE_CODE information | 01F0h |

7.6 Register Maps

7.6.1 PMBus Description

7.6.1.1 PMBus General

Timing and electrical characteristics of the PMBus can be found in the *PMB Power Management Protocol Specification, Part 1, revision 1.1* available at <http://PMBus.org>. The TPS53647 device supports both the 100-kHz and 400-kHz bus timing requirements. The TPS53647 device does not stretch pulses on the PMBus when communicating with the master device.

Communication over the TPS53647 device PMBus interface can support the packet error checking (PEC) scheme if desired. If the master supplies CLK pulses for the PEC byte, PEC is used. If the CLK pulses are not present before a STOP, the PEC is not used.

The TPS53647 device supports a subset of the commands in the PMBus 1.1 specification. Most of the controller parameters can be programmed using the PMBus and stored as defaults for later use. All commands that require data input or output use the literal format. The exponent of the data words is fixed at a reasonable value for the command and altering the exponent is not supported. Direct format data input or output is not supported by the TPS53647 device. See the [Supported PMBus Commands](#) section for specific details.

The TPS53647 device also supports the SMBALERT response protocol. The SMBALERT response protocol is a mechanism by which a slave (the TPS53647 device) can alert the bus master that it wants to talk. The master processes this event and simultaneously accesses all slaves on the bus (that support the protocol) through the alert response address. Only the slave that caused the alert acknowledges this request. The host performs a modified receive byte operation to get the slave's address. At this point, the master can use the PMBus status commands to query the slave that caused the alert. For more information on the SMBus alert response protocol, see the System Management Bus (SMBus) [specification](#).

The TPS53647 device contains non-volatile memory that is used to store configuration settings and scale factors. The settings programmed into the device are not automatically saved into this non-volatile memory though. The STORE_DEFAULT_ALL command must be used to commit the current settings to non-volatile memory as device defaults. The settings that are capable of being stored in non-volatile memory are noted in their detailed descriptions.

7.6.1.2 PMBus Connections

The TPS53647 device can operate in either standard mode (100kbit/s) or fast mode (400kbit/s). Connection for the PMBus interface should follow the High Power DC specifications given in *Section 3.1.3 of the System Management Bus (SMBus) Specification V2.0* for the 400-kHz bus speed or the Low Power DC specifications in *Section 3.1.2*. The complete SMBus specification is available from the SMBus website, smbus.org.

7.6.1.3 Supported Data Formats

The TPS53647 device supports both linear and VID data formats. The linear data format is used for all telemetry reporting data, and VID formatting for certain other commands. (see the [Supported PMBus Commands](#) section for more details on which command supports each data type). Examples of commands that support VID formatting include VOUT_MODE (Read-only Byte) and VOUT_COMMAND (Read/Write Word). An example of each can be seen below in [Figure 21](#) and [Figure 22](#).

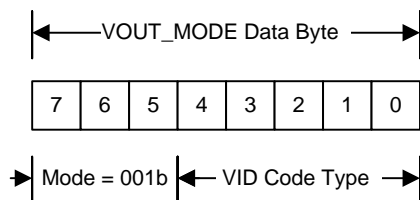


Figure 21. VOUT_MODE Data Byte for VID Mode

Register Maps (continued)

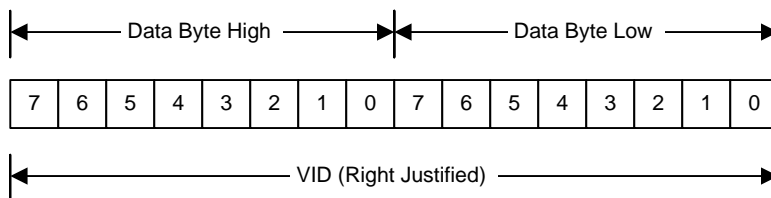


Figure 22. VOUT_COMMAND Data Bytes for VID Mode

The Linear Data Format is a two byte value with:

- An 11-bit, two's complement mantissa, and
- A 5-bit, two's complement exponent (scaling factor).

The format of the two bytes is shown in Figure 23.

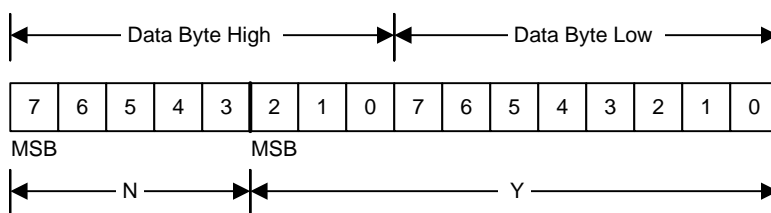


Figure 23. Linear Data Format Data Bytes

The relation between Y, N, and the *real world* value is as shown in Equation 6.

$$X = Y \times 2^N$$

where

- X is the *real world* value
- Y is an 11-bit, two's complement integer
- N is a 5-bit, two's complement integer

(6)

Note that devices that use the Linear format must accept and be able to process any value of N.

7.6.1.4 PMBus Command Format

The TPS53647 device is a PMBus-compliant device. Figure 24 through Figure 35 show the major communication protocols used. For full details on the PMBus communication protocols, please visit <http://pmbus.org>.

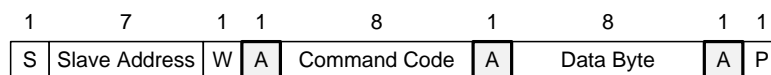


Figure 24. Write Byte Protocol

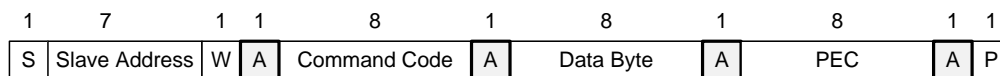


Figure 25. Write Byte Protocol with PEC

Register Maps (continued)

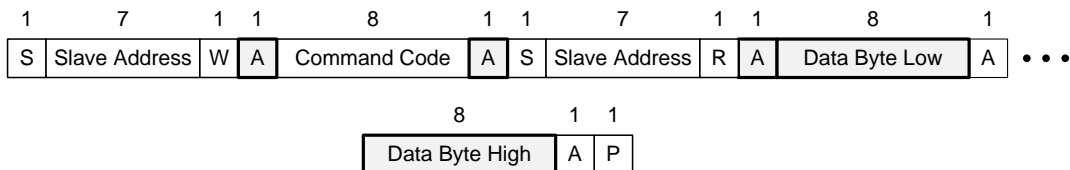


Figure 26. Write Word Protocol

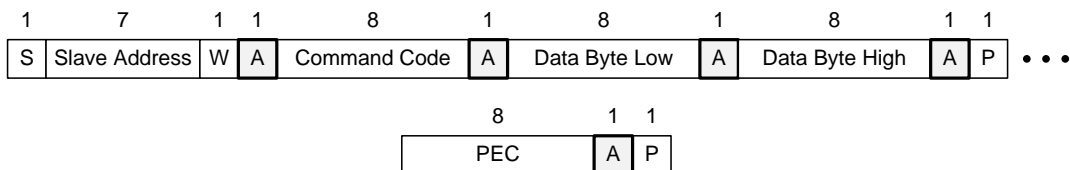


Figure 27. Write Word Protocol with PEC

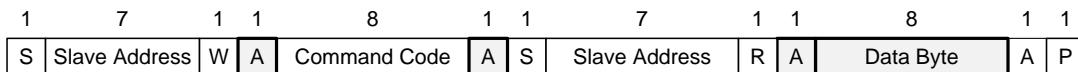


Figure 28. Read Byte Protocol

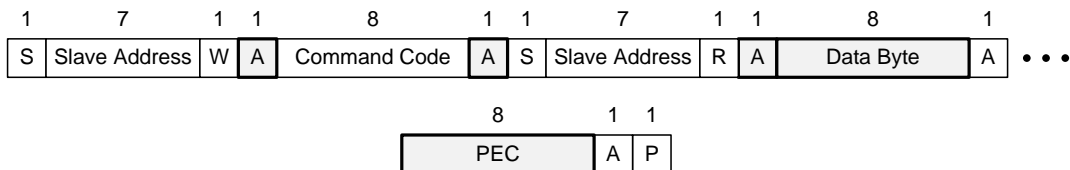


Figure 29. Read Byte Protocol with PEC

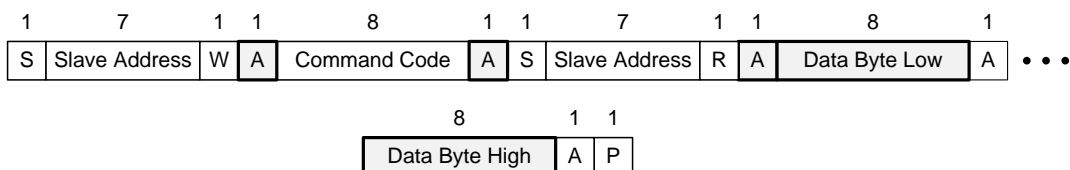


Figure 30. Read Word Protocol

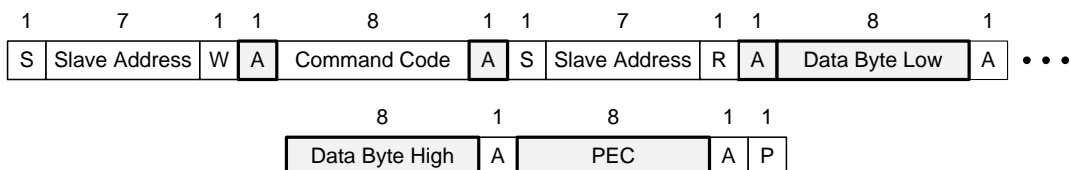
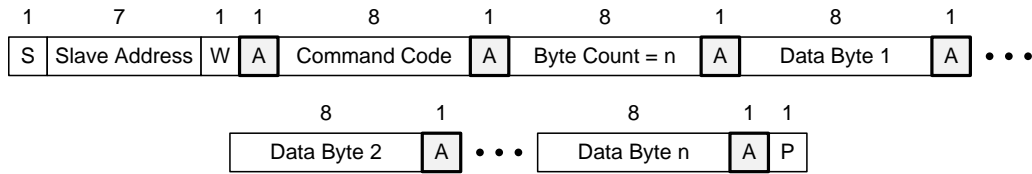
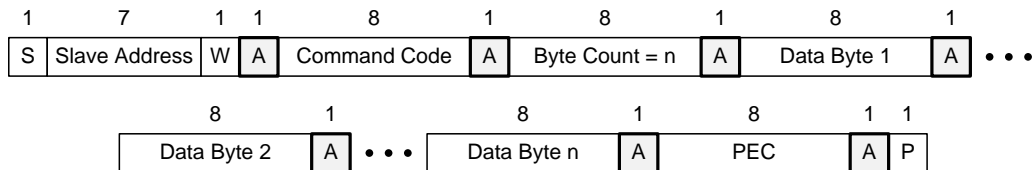
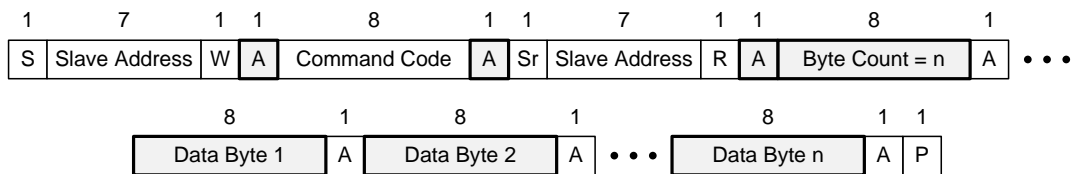
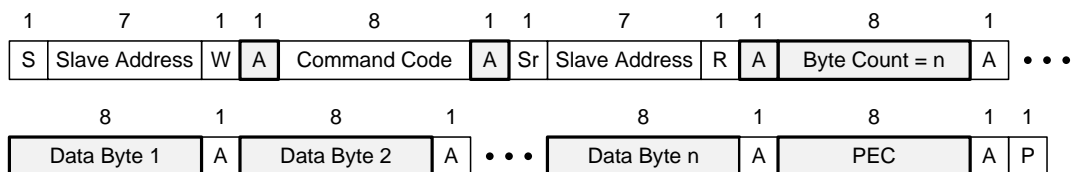


Figure 31. Read Word Protocol with PEC

Register Maps (continued)

Figure 32. Block Write Protocol

Figure 33. Block Write Protocol with PEC

Figure 34. Block Read Protocol

Figure 35. Block Read Protocol with PEC

Register Maps (continued)

7.6.2 PMBus Functionality

7.6.2.1 PMBus Address

The TPS53647 device has a dedicated pin (ADDR-TRISE) for determining the address for the PMBus communication. The device supports a total of 16 possible addresses as listed in the [Electrical Characteristics](#) table.

7.6.2.2 Pin Strap Settings

The TPS53647 device supports only PMBus command sets listed in the [Electrical Characteristics](#) table. In pinstrap mode, the default state of all the configuration registers should be detected from pin strap settings, but users can overwrite the settings via PMBus after the power-up sequence is complete. The pin strap settings can be found in the [Electrical Characteristics](#) table.

7.6.2.3 Supported PMBus Commands

The TPS53647 device supports the following commands from the PMBus 1.1 specification.

7.6.2.3.1 OPERATION (01h)

| | |
|--------------------|---|
| Format | N/A |
| Description | The OPERATION command is used to turn the device output on or off in conjunction with the input from the ENABLE pin. It is also used to set the output voltage to the upper or lower MARGIN levels. |
| Default | 00h |

Figure 36. OPERATION Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----------|----------|---|---|---|--------------|---|
| ON_OFF | SOFT_OFF | OPMARGIN | | | | IIN_OC_VRHOT | |
| R/W | R-0 | R/W | | | | R/W | |

Table 8. OPERATION Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|----------|------|-------|-----|---|
| 7 | ON_OFF | R/W | 0 | — | The On/Off bit is used to enable the IC via PMBus. The necessary condition for this bit to be effective is that the CMD bit in the ON_OFF CONFIG register is set high. However, the CMD bit being high is not a sufficient condition to enable the IC via the On bit, as specified below: 0: (Default) The device output is not enabled via PMBus. 1: The device output is enabled if: a. The supply voltage VIN is greater than the VIN_UVLO threshold, the cmd bit is high, and b. The bit CP in the ON_OFF CONFIG register is low, or c. The bit CP is high and the ENABLE pin is asserted. |
| 6 | SOFT_OFF | R | 0 | — | This bit is not supported and always set to 0 on this device. 0: No Soft off 1: Not Supported. |
| 5-2 | OPMARGIN | R/W | 0 | — | If Margin Low is enabled, load the value from the VOUT_MARGIN_LOW register. If Margin High is enabled, load the value from the VOUT_MARGIN_HIGH register. 00xx: Turn off VOUT margin function 0101: Turn on VOUT margin low and ignore fault 0110: Turn on VOUT margin low and act on fault 1001: Turn on VOUT margin high and ignore fault 1010: Turn on VOUT margin high and act on fault |

Table 8. OPERATION Register Field Descriptions (continued)

| Bit | Field | Type | Reset | NVM | Description |
|-----|--------------|------|-------|-----|--|
| 1-0 | IIN_OC_VRHOT | R/W | 00 | — | This bit sets the option of asserting $\overline{\text{VRHOT}}$ when IIN_OC_WARN_LIMIT is detected. 01: $\overline{\text{VRHOT}}$ assertion ON with IIN_OC_WARN_LIMIT detection others: $\overline{\text{VRHOT}}$ assertion OFF with IIN_OC_WARN_LIMIT detection |

7.6.2.3.2 ON_OFF_CONFIG (02h)

Format N/A

Description The ON_OFF_CONFIG command configures the combination of CONTROL pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when power is applied.

Default 17h

Figure 37. ON_OFF_CONFIG Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|-----|-----|-----|-----|-----|
| Reserved | | | PU | CMD | CP | PL | SP |
| R-000 | | | R-1 | R/W | R/W | R-1 | R-1 |

Table 9. ON_OFF_CONFIG Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|----------|------|-------|-----|--|
| 7-5 | Reserved | R | 000 | — | Always set to 0. |
| 4 | PU | R | 1 | — | This bit is not supported and always set to 1 on this device. 0: Not supported. 1: Device will act on ENABLE pin assertion and/or ON_OFF bit (OPERATION<7>). |
| 3 | CMD | R/W | 0 | — | The CMD bit controls how the device responds to the OPERATION<7> bit. 0: (Default) Device ignores the ON_OFF OPERATION<7> bit. 1: Device responds to the ON_OFF OPERATION<7> bit. |
| 2 | CP | R/W | 1 | — | The CP bit controls how the device responds to the ENABLE pin 0: Device ignores the ENABLE pin, and ON/OFF is controlled only by the OPERATION command 1: Device responds to the ENABLE pin. |
| 1 | PL | R | 1 | — | This bit is not supported and always set to 1 on this device. 0: Not supported. 1: ENABLE pin has active high polarity. |
| 0 | SP | R | 1 | — | This bit is not supported and always set to 1 on this device. 0: Not supported. 1: Turn off output as fast as possible. |

7.6.2.3.3 CLEAR_FAULTS (03h)
Format N/A

Description Clears any faults bits that have been set. At the same time, simultaneously clears all bits in all status registers and negates the PMB_ALERT signal output if it is asserted.

The CLEAR_FAULTS command does not cause a unit that has latched off for a condition to restart. If the fault remains present when the bit is cleared, the fault bit is reset and the host notified by the usual means.

Default NONE

Figure 38. CLEAR_FAULTS Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|-----|-----|-----|-----|-----|-----|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| — | — | — | — | — | — | — | — |

Table 10. CLEAR_FAULTS Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|-------|------|-------|-----|--|
| 7-0 | N/A | — | — | — | No data bytes are sent, only the command code is sent. |

7.6.2.3.4 WRITE_PROTECT (10h)
Format N/A

Description The WRITE_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command has one data byte as described below.

NOTE: Invalid data written to WRITE_PROTECT[7:5] causes the 'CML' bit in the STATUS_BYTE and the 'US_DATA' bit in the STATUS_CML registers to be set. Invalid data also results in no write protection.

Default 00h

Figure 39. WRITE_PROTECT Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|----------|---|---|---|---|
| bit7 | bit6 | bit5 | Reserved | | | | |
| R/W | R/W | R/W | R-0 0000 | | | | |

Table 11. WRITE_PROTECT Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|----------|------|--------|-----|---|
| 7 | bit7 | R/W | 0 | — | 0: (Default) See Table 12 . 1: Disable all writes except for the WRITE_PROTECT command (bit5 and bit6 must be 0 to be valid). |
| 6 | bit6 | R/W | 0 | — | 0: (Default) See Table 12 . 1: Disable all writes except for the WRITE_PROTECT and OPERATION commands (bit5 and bit7 must be 0 to be valid). |
| 5 | bit5 | R/W | 0 | — | 0: (Default) See Table 12 . 1: Disable all writes except for the WRITE_PROTECT, OPERATION, and ON_OFF_CONFIG commands (bit6 and bit7 must be 0 to be valid). |
| 4:0 | Reserved | R | 0 0000 | — | Always set to 0. |

Table 12. WRITE_PROTECT Data Byte Values

| Data Byte Value | Action |
|-----------------|---|
| 1000 0000 | Disables all writes except to the WRITE_PROTECT command. |
| 0100 0000 | Disables all writes except to the WRITE_PROTECT and OPERATION commands. |
| 0010 0000 | Disables all writes to the WRITE_PROTECT, OPERATION, ON_OFF_CONFIG and VOUT_COMMAND commands. |
| 0000 0000 | Enable writes to all commands |
| Others | Invalid data. |

7.6.2.3.5 STORE_DEFAULT_ALL (11h)

Format N/A

Description The STORE_DEFAULT_ALL command instructs the PMBus device to copy the entire contents of the Operating Memory to the matching locations in the non-volatile Default Store memory. Any items in the Operating Memory that do not have matching locations in the Default Store are ignored.

Following a STORE_DEFAULT_ALL command, the following registers return to the default values regardless of the values in the Operating Memory:

- OC_FAULT_LIMIT returns to 125% \times IMAX,
- OC_WARN_LIMIT returns to IMAX,
- VOUT_COMMAND returns to VBOOT,
- VOUT_MAX returns to 00FFh (1.52V in VR12.0 mode and 3.04 V in VR12.5 mode)

Default NONE

Figure 40. STORE_DEFAULT_ALL Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|-----|-----|-----|-----|-----|-----|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| — | — | — | — | — | — | — | — |

Table 13. STORE_DEFAULT_ALL Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|-------|------|-------|-----|--|
| 7:0 | N/A | — | — | — | No data bytes are sent, only the command code is sent. |

7.6.2.3.6 RESTORE_DEFAULT_ALL (12h)

Format N/A

Description The RESTORE_DEFAULT_ALL command instructs the PMBus device to copy the entire contents of the non-volatile Default Store memory to the matching locations in the Operating Memory. The values in the Operating Memory are overwritten by the value retrieved from the Default Store. Any items in Default Store that do not have matching locations in the Operating Memory are ignored.

Default NONE

Figure 41. RESTORE_DEFAULT_ALL Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|-----|-----|-----|-----|-----|-----|
| N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| — | — | — | — | — | — | — | — |

Table 14. RESTORE_DEFAULT_ALL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 7:0 | N/A | — | — | No data bytes are sent, only the command code is sent. |

7.6.2.3.7 CAPABILITY (19h)

| | |
|--------------------|--|
| Format | N/A |
| Description | This command provides a way for a host system to determine some key capabilities of this PMBus device. |
| Default | B0h |

Figure 42. CAPABILITY Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|------|---|----------|----------|---|---|---|
| PEC | SPD | | PMBALERT | Reserved | | | |
| R-1 | R-01 | | R-1 | R-0000 | | | |

Table 15. CAPABILITY Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|----------|------|-------|-----|--|
| 7 | PEC | R | 1 | — | Packet Error Checking is supported. 1: Default |
| 6:5 | SPD | R | 01 | — | Maximum supported bus speed is 400 kHz. 01: Default |
| 4 | PMBALERT | R | 1 | — | This device does have a PMBALERT pin and does support the SMBus Alert Response Protocol. 1: Default |
| 3:0 | Reserved | R | 0000 | — | Always set to 0. |

7.6.2.3.8 VOUT_MODE (20h)

| | |
|--------------------|---|
| Format | VID |
| Description | The PMBus specification dictates that the data word for the VOUT_MODE command is one byte that consists of a 3-bit Mode and 5-bit parameter, as shown below. This command is read-only. If the host sends a VOUT_MODE command for writing, the device will reject the command and declare a communication fault for invalid data and respond as described in <i>PMBus specification II</i> section 10.2.2. |
| Default | 21h |

Figure 43. VOUT_MODE Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---|---|----------------|---|---|---|---|
| DATA_MODE | | | DATA_PARAMETER | | | | |
| R-001 | | | R | | | | |

Table 16. VOUT_MODE Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|----------------|------|--------|-----|--|
| 7:5 | DATA_MODE | R | 001 | — | 001: VID mode. |
| 4:0 | DATA_PARAMETER | R | 0 0001 | — | 00010: For VR12.5 Mode 00001: For VR12.0 Mode |

7.6.2.3.9 VOUT_COMMAND (21h)

Format VID

Description VOUT_COMMAND causes the device to set its output voltage to the commanded value with two data bytes. These data bytes consist of a right-justified VID code with VID0 in bit 0 of the lower data byte, VID1 in bit 1 of the lower byte and so forth. The VID table mapping is determined by the selected VID protocols (VR12.0 or VR12.5) from SLEW_MODE pin or MFR_SPECIFIC_13.

Default VBOOT

Figure 44. VOUT_COMMAND Register

| | | | | | | | |
|-------------|----|----|----|----|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | | | | | | | |
| R-0000 0000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VOUT | | | | | | | |
| R/W | | | | | | | |

Table 17. VOUT_COMMAND Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|------|----------|------|-----------|-----|---|
| 15:8 | Reserved | R | 0000 0000 | — | Always set to 0. |
| 7:0 | VOUT | R/W | | — | Used to set the commanded VOUT. Cannot be set to a level above the value set by VOUT_MAX. |

7.6.2.3.10 VOUT_MAX (24h)

Format VID

Description The VOUT_MAX command sets an upper limit on the output voltage that the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level. The device detects that an attempt has been made to program the output to a voltage greater than the value set by the VOUT_MAX command. This will then be treated as a warning condition and not a fault condition. If an attempt is made to program the output voltage higher than the limit set by this command, the device responds as follows:

- The commanded output voltage is set to VOUT_MAX,
- The OTHER bit is set in the STATUS_BYTE,
- The VOUT bit is set in the STATUS_WORD,
- The VOUT_MAX warning bit is set in the STATUS_VOUT register, and
- The device notifies the host (asserts PMBUS_ALERT).

The data bytes are two bytes, which are in right-justified VID format. The VID table mapping determined by the selected VID protocols (VR12.0 or VR12.5) from the SLEW_MODE pin or MFR_SPECIFIC_13.

Default 00FFh .

Figure 45. VOUT_MAX Register

| | | | | | | | |
|-------------|----|----|----|----|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | | | | | | | |
| R-0000 0000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VOUT_MAX | | | | | | | |

| |
|-----|
| R/W |
|-----|

Table 18. VOUT_MAX Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|------|----------|------|--------------|-----|---|
| 15:8 | Reserved | R | 0000 0000 | — | Always set to 0. |
| 7:0 | VOUT_MAX | R/W | 1111 1111 | — | Used to set the maximum VOUT of the device. |

7.6.2.3.11 VOUT_MARGIN_HIGH (25h)
Format VID

Description The VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to *Margin High*. The data bytes are two bytes, which are in right-justified VID format. The VID table mapping determined by the selected VID protocols from the SLEW_MODE pin or MFR_SPECIFIC_13.

Default 0000h

Figure 46. VOUT_MARGIN_HIGH Register

| | | | | | | | |
|------------------|----|----|----|----|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | | | | | | | |
| R-0000 0000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VOUT_MARGIN_HIGH | | | | | | | |
| R/W | | | | | | | |

Table 19. VOUT_MARGIN_HIGH Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|------|------------------|------|--------------|-----|---|
| 15:8 | Reserved | R | 0000 0000 | — | Always set to 0. |
| 7:0 | VOUT_MARGIN_HIGH | R/W | 0000 0000 | — | Used to set the value for the VOUT Margin High. |

7.6.2.3.12 VOUT_MARGIN_LOW (26h)
Format VID

Description The VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to *Margin Low*. The data bytes are two bytes, which are in right-justified VID format. The VID table mapping determined by the selected VID protocols from the SLEW_MODE pin or MFR_SPECIFIC_13.

Default 0000h

Figure 47. VOUT_MARGIN_LOW Register

| | | | | | | | |
|-----------------|----|----|----|----|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | | | | | | | |
| R-0000 0000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VOUT_MARGIN_LOW | | | | | | | |
| R/W | | | | | | | |

Table 20. VOUT_MARGIN_LOW Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|------|-----------------|------|--------------|-----|--|
| 15:8 | Reserved | R | 0000 0000 | — | Always set to 0. |
| 7:0 | VOUT_MARGIN_LOW | R/W | 0000 0000 | — | Used to set the value for the VOUT Margin Low. |

7.6.2.3.13 IOUT_CAL_OFFSET (39h)

Format Linear

Description The IOUT_CAL_OFFSET command sets the value of compensation for offset errors in the READ_IOUT command, in amperes.

Default 0000h

Figure 48. IOUT_CAL_OFFSET Register

| | | | | | | | |
|--------------------|----|----|----|--------------------|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| IOCAL_OFS_EXPONENT | | | | IOCAL_OFS_MANTISSA | | | |
| R/W | | | | R/W | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IOCAL_OFS_MANTISSA | | | | | | | |
| R/W | | | | | | | |

Table 21. IOUT_CAL_OFFSET Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-------|--------------------|------|-------|-----|--|
| 15:11 | IOCAL_OFS_EXPONENT | R/W | | — | 5-bit, two's complement exponent (scaling factor). |
| 10:0 | IOCAL_OFS_MANTISSA | R/W | | — | 11-bit, two's complement mantissa. |

7.6.2.3.14 VOUT_OV_FAULT_RESPONSE (41h)

Format N/A

Description The VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an output overvoltage fault. Upon triggering the overvoltage fault, the controller is latched off, and the following actions are taken:

- Set the VOUT_OV_FAULT bit in the STATUS_BYTE,
- Set the VOUT bit in the STATUS_WORD,
- Set the VOUT_OV_FAULT bit in the STATUS_VOUT register, and
- The device notifies the host (asserts PMB_ALERT).

Default \sim filter="filter4, filter5"80hfilter="filter6"9Ah! \sim 80h

Figure 49. VOUT_OV_FAULT_RESPONSE Register

| | | | | | | | |
|------------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VOUT_OV_FAULT_RESPONSE | | | | | | | |
| R-1000 0000 | | | | | | | |

Table 22. VOUT_OV_FAULT_RESPONSE Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|----------------------------|------|--------------|-----|--|
| 7:0 | VOUT_OV_FAULT_RESPO NSE | R | 1000 0000 | — | Upon triggering the overvoltage fault, the controller will shut the device down immediately and will not attempt to restart. The output remains disabled until the fault is cleared. |

7.6.2.3.15 VOUT_UV_FAULT_RESPONSE (45h)

Format N/A

Description The VOUT_UV_FAULT_RESPONSE instructs the device on what action to take in response to an output undervoltage fault. Upon triggering the undervoltage fault, the following actions are taken:

- Set the OTHER bit in the STATUS_BYTE,
- Set the VOUT bit in the STATUS_WORD,
- Set the VOUT_UV_FAULT bit in the STATUS_VOUT register, and
- The device notifies the host (asserts $\overline{\text{PMB_ALERT}}$).

Default BAh

Figure 50. VOUT_UV_FAULT_RESPONSE Register

| | | | | | | | |
|------------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VOUT_UV_FAULT_RESPONSE | | | | | | | |
| R-1011 1010 | | | | | | | |

Table 23. VOUT_UV_FAULT_RESPONSE Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|------------------------|------|-----------|-----|---|
| 7:0 | VOUT_UV_FAULT_RESPONSE | R | 1011 1010 | — | Upon triggering the undervoltage fault, the controller will shut the device down immediately and will attempt to restart after a 22 ms delay. |

7.6.2.3.16 IOUT_OC_FAULT_LIMIT (46h)

Format Linear

Description The IOUT_OC_FAULT_LIMIT command sets the value of the output current, in amperes, that causes an overcurrent fault condition. Upon triggering the overcurrent fault, the following actions are taken:

- Set the IOUT_OC_FAULT bit in the STATUS_BYTE,
- Set the IOUT bit in the STATUS_WORD,
- Set the IOUT_OC_FAULT bit in the STATUS_IOUT register, and
- The device notifies the host (asserts $\overline{\text{PMB_ALERT}}$).

Default 125% IMAX

Figure 51. IOUT_OC_FAULT_LIMIT Register

| | | | | | | | |
|--------------------|----|----|----|----|--------------------|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| OCF_LIMIT_EXPONENT | | | | | OCF_LIMIT_MANTISSA | | |
| R/W | | | | | R/W | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OCF_LIMIT_MANTISSA | | | | | | | |
| R/W | | | | | | | |

Table 24. IOUT_OC_FAULT_LIMIT Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-------|--------------------|------|-------|-----|--|
| 15:11 | OCF_LIMIT_EXPONENT | R/W | | — | 5-bit, two's complement exponent (scaling factor). |
| 10:0 | OCF_LIMIT_MANTISSA | R/W | | — | 11-bit, two's complement mantissa. |

7.6.2.3.17 IOUT_OC_FAULT_RESPONSE (47h)
Format N/A

Description The IOUT_OC_FAULT_RESPONSE instructs the device on what action to take in response to an output overcurrent fault. Upon triggering the overcurrent fault, the controller is latched off, and the following actions are taken:

- Set the IOUT_OC_FAULT bit in the STATUS_BYTE,
- Set the IOUT bit in the STATUS_WORD,
- Set the IOUT_OC_FAULT bit in the STATUS_IOUT register, and
- The device notifies the host (asserts $\overline{\text{PMB_ALERT}}$).

Default FAh

Figure 52. IOUT_OC_FAULT_RESPONSE Register

| | | | | | | | |
|------------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IOUT_OC_FAULT_RESPONSE | | | | | | | |
| R-1111 1010 | | | | | | | |

Table 25. IOUT_OC_FAULT_RESPONSE Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|------------------------|------|--------------|-----|--|
| 7:0 | IOUT_OC_FAULT_RESPONSE | R | 1111 1010 | — | Upon triggering the overcurrent fault, the controller immediately shuts down the device and attempts to restart after a 22 ms delay. |

7.6.2.3.18 IOUT_OC_WARN_LIMIT (4Ah)
Format Linear

Description The IOUT_OC_WARN_LIMIT command sets the value of the output current, in amperes, that causes an output overcurrent warning condition. Upon triggering the overcurrent warning, the following actions are taken:

- Set the OTHER bit in the STATUS_BYTE,
- Set the IOUT bit in the STATUS_WORD,
- Set the IOUT OC Warning bit in the STATUS_IOUT register, and
- The device notifies the host (asserts PMB_ALERT).

Default IMAX

Figure 53. IOUT_OC_WARN_LIMIT Register

| | | | | | | | |
|--------------------|----|----|----|----|--------------------|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| OCW_LIMIT_EXPONENT | | | | | OCW_LIMIT_MANTISSA | | |
| R/W | | | | | R/W | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OCW_LIMIT_MANTISSA | | | | | | | |
| R/W | | | | | | | |

Table 26. IOUT_OC_WARN_LIMIT Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-------|--------------------|------|-------|-----|--|
| 15:11 | OCW_LIMIT_EXPONENT | R/W | | — | 5-bit, two's complement exponent (scaling factor). |
| 10:0 | OCW_LIMIT_MANTISSA | R/W | | — | 11-bit, two's complement mantissa. |

7.6.2.3.19 OT_FAULT_LIMIT (4Fh)
Format Linear

Description The OT_FAULT_LIMIT command sets the value of the temperature limit, in degrees Celsius, that causes an over-temperature fault condition. The default value is 125C°. Upon triggering the over-temperature fault, the following actions are taken:

- Set the TEMPERATURE bit in the STATUS_BYTE,
- Set the OT_FAULT bit in the STATUS_TEMPERATURE register, and
- The device notifies the host (asserts PMB_ALERT and VR_FAULT).

Default 007Dh

Figure 54. OT_FAULT_LIMIT Register

| | | | | | | | |
|-------------------|----|----|----|----|-------------------|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| OT_LIMIT_EXPONENT | | | | | OT_LIMIT_MANTISSA | | |
| R/W | | | | | R/W | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OT_LIMIT_MANTISSA | | | | | | | |
| R/W | | | | | | | |

Table 27. OT_FAULT_LIMIT Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-------|-------------------|------|------------------|-----|--|
| 15:11 | OT_LIMIT_EXPONENT | R/W | 0000 0 | — | 5-bit, two's complement exponent (scaling factor). |
| 10:0 | OT_LIMIT_MANTISSA | R/W | 000 0111 1101 | — | 11-bit, two's complement mantissa. |

7.6.2.3.20 OT_FAULT_RESPONSE (50h)

Format N/A

Description The OT_FAULT_RESPONSE instructs the device on what action to take in response to an over-temperature fault. Upon triggering the over-temperature fault, the controller shuts off and attempts to restart when the temperature reduces by 15C°, and the following actions are taken:

- Set the TEMPERATURE bit in the STATUS_BYTE,
- Set the OT_FAULT bit in the STATUS_TEMPERATURE register, and
- The device notifies the host (asserts PMB_ALERT and VR_FAULT).

Default F8h

Figure 55. OT_FAULT_RESPONSE Register

| | | | | | | | |
|-------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OT_FAULT_RESPONSE | | | | | | | |
| R-1111 1000 | | | | | | | |

Table 28. OT_FAULT_RESPONSE Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|-------------------|------|-----------|-----|---|
| 7:0 | OT_FAULT_RESPONSE | R | 1111 1000 | — | Upon triggering the over-temperature fault, the device will shut down immediately (disables the output), and will restart when the temperature goes 15 degree Celsius below OT_FAULT_LIMIT. |

7.6.2.3.21 OT_WARN_LIMIT (51h)

Format Linear

Description The OT_WARN_LIMIT command sets the temperature, in degrees Celsius, at which it should indicate an over-temperature warning condition. The default value is 95C. Upon triggering the over-temperature warning, the following actions are taken:

- Sets the TEMPERATURE bit in the STATUS_BYTE,
- Sets the OT Warning bit in the STATUS_TEMPERATURE register, and
- The device notifies the host (asserts PMB_ALERT).

Default 005Fh

Figure 56. OT_WARN_LIMIT Register

| | | | | | | | |
|-------------------|----|----|----|----|-------------------|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| OTW_WARN_EXPONENT | | | | | OTW_WARN_MANTISSA | | |
| R/W | | | | | R/W | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OTW_WARN_MANTISSA | | | | | | | |
| R/W | | | | | | | |

Table 29. OT_WARN_LIMIT Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-------|-------------------|------|---------------|-----|--|
| 15:11 | OTW_WARN_EXPONENT | R/W | 0000 0 | — | 5-bit, two's complement exponent (scaling factor). |
| 10:0 | OTW_WARN_MANTISSA | R/W | 000 0101 1111 | — | 11-bit, two's complement mantissa. |

7.6.2.3.22 VIN_OV_FAULT_LIMIT (55h)
Format Linear

Description The VIN_OV_FAULT_LIMIT command sets the value of the input voltage that causes an input overvoltage fault condition. The default value is 17 V in NVM mode and 14 V in pinstrap mode. Upon triggering an input voltage fault, the following actions are taken:

- Sets the OTHER bit in the STATUS_BYTE,
- Sets the INPUT bit in the upper byte of the STATUS_WORD,
- Sets the VIN_OV_FAULT bit in the STATUS_INPUT register, and
- The device notifies the host (asserts PMB_ALERT).

Default ~~0011h~~ **!~000Fh**
Figure 57. VIN_OV_FAULT_LIMIT Register

| | | | | | | | |
|------------------|----|----|----|----|------------------|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VIN_OVF_EXPONENT | | | | | VIN_OVF_MANTISSA | | |
| R/W | | | | | R/W | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VIN_OVF_MANTISSA | | | | | | | |
| R/W | | | | | | | |

Table 30. VIN_OV_FAULT_LIMIT Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-------|------------------|------|---------------|-----|--|
| 15:11 | VIN_OVF_EXPONENT | R/W | 0000 0 | — | 5-bit, two's complement exponent (scaling factor). |
| 10:0 | VIN_OVF_MANTISSA | R/W | 000 0001 0001 | — | 11-bit, two's complement mantissa. |

After a STORE_DEFAULT_ALL command, the controller reads the last two LSB of VIN_OV_FAULT_LIMIT and convert to decimal, and then adds 14 and converts to save into the VIN_OV_FAULT_LIMIT register. For example, when the two LSB are 01b, after STORE_DEFAULT_ALL command, the VIN_OV_FAULT_LIMIT reads 000Fh (15 V).

7.6.2.3.23 IIN_OC_FAULT_LIMIT (5Bh)
Format Linear

Description The IIN_OC_FAULT_LIMIT command sets the value of the input current, in amperes, that causes an input overcurrent fault condition. Upon triggering the overcurrent fault, the following actions are taken:

- Sets the OTHER bit in the STATUS_BYTE,
- Sets the INPUT bit in the STATUS_WORD,
- Sets the IIN_OC_FAULT bit in the STATUS_INPUT register, and
- The device notifies the host (asserts PMB_ALERT).

Default 00FFh

Figure 58. IIN_OC_FAULT_LIMIT Register

| | | | | | | | |
|----------------------|----|----|----|----|----------------------|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| INOCF_LIMIT_EXPONENT | | | | | INOCF_LIMIT_MANTISSA | | |
| R/W | | | | | R/W | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| INOCF_LIMIT_MANTISSA | | | | | | | |
| R/W | | | | | | | |

Table 31. IIN_OC_FAULT_LIMIT Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-------|----------------------|------|---------------|-----|--|
| 15:11 | INOCF_LIMIT_EXPONENT | R/W | 0000 0 | — | 5-bit, two's complement exponent (scaling factor). |
| 10:0 | INOCF_LIMIT_MANTISSA | R/W | 000 1111 1111 | — | 11-bit, two's complement mantissa. |

7.6.2.3.24 IIN_OC_FAULT_RESPONSE (5Ch)

Format N/A

Description The IIN_OC_FAULT_RESPONSE instructs the device on what action to take in response to an input overcurrent fault. Upon triggering the input overcurrent fault, the controller is latched off, and the following actions are taken:

- Sets the OTHER bit in the STATUS_BYTE,
- Sets the INPUT bit in the STATUS_WORD,
- Sets the IIN_OC_FAULT bit in the STATUS_INPUT register, and
- The device notifies the host (asserts $\overline{\text{PMB_ALERT}}$ and $\overline{\text{VR_FAULT}}$).

Default C0h

Figure 59. IIN_OC_FAULT_RESPONSE Register

| | | | | | | | |
|-----------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IIN_OC_FAULT_RESPONSE | | | | | | | |
| R-1100 0000 | | | | | | | |

Table 32. IIN_OC_FAULT_RESPONSE Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|-----------------------|------|-----------|-----|---|
| 7:0 | IIN_OC_FAULT_RESPONSE | R | 1100 0000 | — | Upon triggering the input overcurrent fault, the device will shut down immediately (disables the output), and will not attempt to restart. The output then remains disabled until the fault is cleared. |

7.6.2.3.25 IIN_OC_WARN_LIMIT (5Dh)
Format Linear

Description The IIN_OC_WARN_LIMIT command sets the value of the input current, in amperes, that causes the input overcurrent warning condition. The default setting is 25A. Upon triggering the overcurrent warning, the following actions are taken:

- Sets the OTHER bit in the STATUS_BYTE,
- Sets the INPUT bit in the STATUS_WORD,
- Sets the IIN OC Warning bit in the STATUS_INPUT register, and
- The device notifies the host (asserts PMB_ALERT).

Default 0019h

Figure 60. IIN_OC_WARN_LIMIT Register

| | | | | | | | |
|----------------------|----|----|----|----|----------------------|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| INOCW_LIMIT_EXPONENT | | | | | INOCW_LIMIT_MANTISSA | | |
| R/W | | | | | R/W | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| INOCW_LIMIT_MANTISSA | | | | | | | |
| R/W | | | | | | | |

Table 33. IIN_OC_WARN_LIMIT Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-------|----------------------|------|---------------|-----|--|
| 15:11 | INOCW_LIMIT_EXPONENT | R/W | 0000 0 | — | 5-bit, two's complement exponent (scaling factor). |
| 10:0 | INOCW_LIMIT_MANTISSA | R/W | 000 0001 1001 | — | 11-bit, two's complement mantissa. |

7.6.2.3.26 STATUS_BYTE (78h)
Format N/A

Description The STATUS_BYTE command returns a single byte of information with the a summary of critical faults. The STATUS_BYTE command is the same register as the low byte of the STATUS_WORD command. It should be noted that all faults and warnings trigger the assertion of PMB_ALERT.

Default 00h

Figure 61. STATUS_BYTE Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-----|---------|---------|--------|------|-----|-------|
| BUSY | OFF | VOUT_OV | IOUT_OC | VIN_UV | TEMP | CML | OTHER |
| R-0 | R | R | R | R | R | R | R |

Table 34. STATUS_BYTE Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|---------|------|-------|-----|--|
| 7 | BUSY | R | 0 | — | Not supported and always set to 0 |
| 6 | OFF | R | | — | This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. 0: Raw status indicating the IC is providing power to VOUT. 1: Raw status indicating the IC is not providing power to VOUT. |
| 5 | VOUT_OV | R | | — | Output Over-Voltage Fault Condition 0: Latched flag indicating no VOUT OV fault has occurred. 1: Latched flag indicating a VOUT OV fault occurred |
| 4 | IOUT_OC | R | | — | Output Over-Current Fault Condition 0: Latched flag indicating no IOUT OC fault has occurred. 1: Latched flag indicating an IOUT OC fault has occurred. |
| 3 | VIN_UV | R | | — | Input Under-Voltage Fault Condition 0: Latched flag indicating VIN is above the UVLO threshold. 1: Latched flag indicating VIN is below the UVLO threshold. |
| 2 | TEMP | R | | — | Over-Temperature Fault/Warning 0: Latched flag indicating no OT fault or warning has occurred. 1: Latched flag indicating an OT fault or warning has occurred. |
| 1 | CML | R | | — | Communications, Memory or Logic Fault 0: Latched flag indicating no communication, memory, or logic fault has occurred. 1: Latched flag indicating a communication, memory, or logic fault has occurred. |
| 0 | OTHER | R | | — | Other Fault This bit is used to flag faults not covered with the other bit faults. In this case, UVF or OCW faults are examples of other faults not covered by the bits [6:1] in this register. 0: No fault has occurred 1: A fault or warning not listed in bits [6:1] has occurred. |

7.6.2.3.27 STATUS_WORD (79h)
Format N/A

Description The STATUS_WORD command returns two bytes of information with a summary of critical faults, such as over-voltage, overcurrent, over-temperature, etc. It should be noted that all faults and warnings except VIN_UV trigger the assertion of PMB_ALERT.

NOTE: The STATUS_WORD low byte is the STATUS_BYTE.

Default 0000h

Figure 62. STATUS_WORD Register

| | | | | | | | |
|------|------|---------|---------|--------|------|-------|---------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VOUT | IOUT | INPUT | MFR | PGOOD | FANS | OTHER | UNKNOWN |
| R | R | R | R | R | R-0 | R-0 | R-0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BUSY | OFF | VOUT_OV | IOUT_OC | VIN_UV | TEMP | CML | OTHER |
| R-0 | R | R | R | R | R | R | R |

Table 35. STATUS_WORD Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|---------|------|-------|-----|--|
| 15 | VOUT | R | | — | Output Voltage Fault/Warning 0: Latched flag indicating no VOUT fault or warning has occurred. 1: Latched flag indicating a VOUT fault or warning has occurred. |
| 14 | IOUT | R | | — | Output Current Fault/Warning 0: Latched flag indicating no IOUT fault or warning has occurred. 1: Latched flag indicating an IOUT fault or warning has occurred. |
| 13 | INPUT | R | | — | Input Voltage/Current Fault/Warning 0: Latched flag indicating no VIN or IIN fault or warning has occurred. 1: Latched flag indicating a VIN or IIN fault or warning has occurred. |
| 12 | MFR | R | | — | MFR_SPECIFIC Fault 0: Latched flag indicating no MFR_SPECIFIC fault has occurred. 1: Latched flag indicating a MFR_SPECIFIC fault has occurred. |
| 11 | PGOOD | R | | — | Power Good Status 0: Raw status indicating VRRDY pin is at logic high. 1: Raw status indicating VRRDY pin is at logic low. |
| 10 | FANS | R | 0 | — | Not supported and always set to 0. |
| 9 | OTHER | R | 0 | — | Not supported and always set to 0. |
| 8 | UNKNOWN | R | 0 | — | Not supported and always set to 0. |
| 7 | BUSY | R | 0 | — | See information in Table 34 |
| 6 | OFF | R | | — | |
| 5 | VOUT_OV | R | | — | |
| 4 | IOUT_OC | R | | — | |
| 3 | VIN_UV | R | | — | |
| 2 | TEMP | R | | — | |
| 1 | CML | R | | — | |
| 0 | OTHER | R | | — | |

7.6.2.3.28 STATUS_VOUT (7Ah)

Format N/A
Description The STATUS_VOUT command returns one byte of information relating to the status of the converter's output voltage related faults.
Default 00h

Figure 63. STATUS_VOUT Register

| | | | | | | | |
|----------|----------|----------|----------|-----------|---------|----------|------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VOUT_OVF | VOUT_OVW | VOUT_UVW | VOUT_UVF | VOUT_MAXW | TON_MAX | TOFF_MAX | VOUT_TRACK |
| R | R-0 | R-0 | R | R | R-0 | R-0 | R-0 |

Table 36. STATUS_VOUT Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|------------|------|-------|-----|--|
| 7 | VOUT_OVF | R | | — | Output Over-Voltage Fault 0: Latched flag indicating no VOUT OV fault has occurred. 1: Latched flag indicating a VOUT OV fault has occurred. |
| 6 | VOUT_OVW | R | 0 | — | Not supported and always set to 0. |
| 5 | VOUT_UVW | R | 0 | — | Not supported and always set to 0. |
| 4 | VOUT_UVF | R | | — | Output Under-Voltage Fault 0: Latched flag indicating no VOUT UV fault has occurred. 1: Latched flag indicating a VOUT UV fault has occurred. |
| 3 | VOUT_MAXW | R | | — | VOUT Max Warning 0: Latched flag indicating that no VOUT Max warning has occurred 1: Latched flag indicating that an attempt has been made to set the output voltage to a value higher than allowed by the VOUT_MAX command. |
| 2 | TON_MAX | R | 0 | — | Not supported and always set to 0. |
| 1 | TOFF_MAX | R | 0 | — | Not supported and always set to 0. |
| 0 | VOUT_TRACK | R | 0 | — | Not supported and always set to 0. |

7.6.2.3.29 STATUS_IOUT (7Bh)

Format N/A
Description The STATUS_IOUT command returns one byte of information relating to the status of the converter's output current related faults.
Default 00h

Figure 64. STATUS_IOUT Register

| | | | | | | | |
|----------|------------|----------|----------|------------|-----------|----------|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IOUT_OCF | IOUT_OCUVF | IOUT_OCW | IOUT_UCF | CUR_SHAREF | POW_LIMIT | POUT_OPF | POUT_OPW |
| R | R-0 | R | R-0 | R-0 | R-0 | R-0 | R-0 |

Table 37. STATUS_IOUT Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|----------|------|-------|-----|---|
| 7 | IOUT_OCF | R | | — | Output Over-Current Fault 0: Latched flag indicating no IOUT OC fault has occurred. 1: Latched flag indicating a IOUT OC fault has occurred . |

Table 37. STATUS_IOUT Register Field Descriptions (continued)

| Bit | Field | Type | Reset | NVM | Description |
|-----|------------|------|-------|-----|--|
| 6 | IOUT_OCUVF | R | 0 | — | Not supported and always set to 0. |
| 5 | IOUT_OCW | R | | — | Output Over-Current Warning 0: Latched flag indicating no IOUT OC warning has occurred 1: Latched flag indicating a IOUT OC warning has occurred |
| 4 | IOUT_UCF | R | 0 | — | Not supported and always set to 0. |
| 3 | CUR_SHAREF | R | 0 | — | Not supported and always set to 0. |
| 2 | POW_LIMIT | R | 0 | — | Not supported and always set to 0. |
| 1 | POUT_OPF | R | 0 | — | Not supported and always set to 0. |
| 0 | POUT_OPW | R | 0 | — | Not supported and always set to 0. |

7.6.2.3.30 STATUS_INPUT (7Ch)
Format

N/A

Description

The STATUS_INPUT command returns one byte of information relating to the status of the converter's input voltage and current related faults.

Default

00h

Figure 65. STATUS_INPUT Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| VIN_OVF | VIN_OVW | VIN_UVW | VIN_UVF | VIN_OFF | IIN_OCF | IIN_OCW | PIN_OPW |
| R | R-0 | R-0 | R | R-0 | R | R | R-0 |

Table 38. STATUS_INPUT Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|---------|------|-------|-----|---|
| 7 | VIN_OVF | R | | — | Input Over-Voltage Fault 0: Latched flag indicating no VIN OV fault has occurred. 1: Latched flag indicating a VIN OV fault has occurred. |
| 6 | VIN_OVW | R | 0 | — | Not supported and always set to 0. |
| 5 | VIN_UVW | R | 0 | — | Not supported and always set to 0. |
| 4 | VIN_UVF | R | | — | Input Under-Voltage Fault 0: Latched flag indicating no VIN UV fault has occurred. 1: Latched flag indicating a VIN UV fault has occurred. |
| 3 | VIN_OFF | R | 0 | — | Not supported and always set to 0. |
| 2 | IIN_OCF | R | | — | Input Over-Current Fault 0: Latched flag indicating no IIN OC fault has occurred. 1: Latched flag indicating a IIN OC fault has occurred. |
| 1 | IIN_OCW | R | | — | Input Over-Current Warning 0: Latched flag indicating no IIN OC warning has occurred. 1: Latched flag indicating a IIN OC warning has occurred. |
| 0 | PIN_OPW | R | 0 | — | Not supported and always set to 0. |

7.6.2.3.31 STATUS_TEMPERATURE (7Dh)

| | |
|--------------------|--|
| Format | N/A |
| Description | The STATUS_TEMPERATURE command returns one byte of information relating to the status of the converter's temperature related faults. |
| Default | 00h |

Figure 66. STATUS_TEMPERATURE Register

| | | | | | | | |
|-----|-----|-----|-----|----------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OTF | OTW | UTW | UTF | Reserved | | | |
| R | R | R-0 | R-0 | R-0000 | | | |

Table 39. STATUS_TEMPERATURE Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|----------|------|-------|-----|---|
| 7 | OTF | R | | — | Over-Temperature Fault 0: Latched flag indicating no temperature fault has occurred. 1: Latched flag indicating a temperature fault has occurred. |
| 6 | OTW | R | | — | Over-Temperature Warning 0: Latched flag indicating no temperature warning has occurred. 1: Latched flag indicating a temperature warning has occurred. |
| 5 | UTW | R | 0 | — | Not supported and always set to 0. |
| 4 | UTF | R | 0 | — | Not supported and always set to 0. |
| 3-0 | Reserved | R | 0000 | — | Always set to 0. |

7.6.2.3.32 STATUS_CML (7Eh)

| | |
|--------------------|---|
| Format | N/A |
| Description | The STATUS_CML command returns one byte with contents regarding communication, logic, or memory conditions. |
| Default | 00h |

Figure 67. STATUS_CML Register

| | | | | | | | |
|--------|---------|----------|-----------|-----------|----------|----------|-----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| US_CMD | US_DATA | PEC_FAIL | MEM_FAULT | PRO_FAULT | Reserved | COM_FAIL | CML_OTHER |
| R | R | R | R | R-0 | R-0 | R | R-0 |

Table 40. STATUS_CML Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|-----------|------|-------|-----|---|
| 7 | US_CMD | R | | — | Invalid or Unsupported Command Received 0: Latched flag indicating no invalid or unsupported command has received. 1: Latched flag indicating an invalid or unsupported command has received. |
| 6 | US_DATA | R | | — | Invalid or Unsupported Data Received 0: Latched flag indicating no invalid or unsupported data has received. 1: Latched flag indicating an invalid or unsupported data has received. |
| 5 | PEC_FAIL | R | | — | Packet Error Check Failed 0: Latched flag indicating no packet error check has failed 1: Latched flag indicating a packet error check has failed |
| 4 | MEM_FAULT | R | | — | Memory Error 0: Latched flag indicating that there is no memory error. 1: Latched flag indicating that a memory error, i.e. PMBus controller is trying to write into registers when NVM memory is being programmed. |
| 3 | PRO_FAULT | R | 0 | — | Not supported and always set to 0. |
| 2 | Reserved | R | 0 | — | Always set to 0. |
| 1 | COM_FAIL | R | | — | Other Communication Faults 0: Latched flag indicating no communication fault other than the ones listed in this table has occurred. 1: Latched flag indicating a communication fault other than the ones listed in this table has occurred. |
| 0 | CML_OTHER | R | 0 | — | Not supported and always set to 0. |

7.6.2.3.33 STATUS_MFR_SPECIFIC (80h)

| | |
|--------------------|---|
| Format | N/A |
| Description | The STATUS_MFR_SPECIFIC command returns one byte containing manufacturer-specific faults or warnings. |
| Default | 00h |

Figure 68. STATUS_MFR_SPECIFIC Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|---------|-------------|---|---|----------|----------|-------|
| MFR_FAULT_PS | MFR_PBF | CUR_SH_WARN | | | RST_VOUT | VOUT_MIN | PHFLT |
| R | R | R | | | R | R | R |

Table 41. STATUS_MFR_SPECIFIC Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|--------------|------|-------|-----|---|
| 7 | MFR_FAULT_PS | R | | — | Power State Fault 0: Latched flag indicating no fault from TI power stage has occurred. 1: Latched flag indicating a fault from TI power stage has occurred. |
| 6 | MFR_PBF | R | | — | Pre-Bias Fault 0: Latched flag indicating no pre-bias fault ($V_{OUT} > 2.75V$ at startup) has occurred. 1: Latched flag indicating a pre-bias fault ($V_{OUT} > 2.75V$ at startup) has occurred. |
| 5:3 | CUR_SH_WARN | R | 000 | — | not supported and always set to 0 |
| 2 | RST_VOUT | R | | — | RST_VOUT Fault 0: Latched flag indicating no RST_VOUT fault has occurred. 1: Latched flag indicating a RST_VOUT fault has occurred. |
| 1 | VOUT_MIN | R | | — | VOUT_MIN Fault 0: Latched flag indicating no VOUT_MIN fault has occurred. 1: Latched flag indicating a VOUT_MIN fault has occurred. |
| 0 | PHFLT | R | | — | Phase Fault 0: Latched flag indicating no phase fault (no phase pulse detected) has occurred. 1: Latched flag indicating a phase fault (no phase pulse detected) has occurred. |

7.6.2.3.34 READ_VIN (88h)

Format Linear

Description The READ_VIN command returns the input voltage in volts. Refer to [Equation 6](#) to get the real world value.

Default

Figure 69. READ_VIN Register

| | | | | | | | |
|-------------------|----|----|----|----|-------------------|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| READ_VIN_EXPONENT | | | | | READ_VIN_MANTISSA | | |
| R | | | | | R | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| READ_VIN_MANTISSA | | | | | | | |
| R | | | | | | | |

Table 42. READ_VIN Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-------|-------------------|------|-------|-----|--|
| 15:11 | READ_VIN_EXPONENT | R | | — | 5-bit, two's complement exponent (scaling factor). |
| 10:0 | READ_VIN_MANTISSA | R | | — | 11-bit, two's complement mantissa. |

7.6.2.3.35 READ_IIN (89h)

Format Linear

Description The READ_IIN command returns the input current in amperes. Refer to [Equation 6](#) to get the real world value.

Default

Figure 70. READ_IIN Register

| | | | | | | | |
|-------------------|----|----|----|----|-------------------|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| READ_IIN_EXPONENT | | | | | READ_IIN_MANTISSA | | |
| R | | | | | R | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| READ_IIN_MANTISSA | | | | | | | |
| R | | | | | | | |

Table 43. READ_IIN Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-------|-------------------|------|-------|-----|--|
| 15:11 | READ_IIN_EXPONENT | R | | — | 5-bit, two's complement exponent (scaling factor). |
| 10:0 | READ_IIN_MANTISSA | R | | — | 11-bit, two's complement mantissa. |

7.6.2.3.36 READ_VOUT (8Bh)
Format VID

Description The READ_VOUT command returns the actual, measured output voltage.

Default

Another command, MFR_READ_VOUT (D4h), returns the measured output voltage in linear format.

Figure 71. READ_VOUT Register

| | | | | | | | |
|---------------|----|----|----|----|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| READ_VOUT_VID | | | | | | | |
| R | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| READ_VOUT_VID | | | | | | | |
| R | | | | | | | |

Table 44. READ_VOUT Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|------|---------------|------|-------|-----|--------------------|
| 15:0 | READ_VOUT_VID | R | | — | 16-bit, VID format |

7.6.2.3.37 READ_IOUT (8Ch)
Format Linear

Description The READ_IOUT command returns the output current in amperes. Refer to [Equation 6](#) to get the real world value.

Default
Figure 72. READ_IOUT Register

| | | | | | | | |
|--------------------|----|----|----|----|--------------------|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| READ_IOUT_EXPONENT | | | | | READ_IOUT_MANTISSA | | |
| R | | | | | R | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| READ_IOUT_MANTISSA | | | | | | | |
| R | | | | | | | |

Table 45. READ_IOUT Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-------|--------------------|------|-------|-----|--|
| 15:11 | READ_IOUT_EXPONENT | R | | — | 5-bit, two's complement exponent (scaling factor). |
| 10:0 | READ_IOUT_MANTISSA | R | | — | 11-bit, two's complement mantissa. |

7.6.2.3.38 READ_TEMPERATURE_1 (8Dh)

Format Linear

Description The READ_TEMPERATURE_1 command returns the temperature in degrees Celsius. Refer to [Equation 6](#) to get the real world value.

Default

Figure 73. READ_TEMPERATURE_1 Register

| | | | | | | | |
|----------------------|----|----|----|----|----------------------|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| READ_TEMP_1_EXPONENT | | | | | READ_TEMP_1_MANTISSA | | |
| R | | | | | R | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| READ_TEMP_1_MANTISSA | | | | | | | |
| R | | | | | | | |

Table 46. READ_TEMPERATURE_1 Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-------|----------------------|------|-------|-----|--|
| 15:11 | READ_TEMP_1_EXPONENT | R | | — | 5-bit, two's complement exponent (scaling factor). |
| 10:0 | READ_TEMP_1_MANTISSA | R | | — | 11-bit, two's complement mantissa. |

7.6.2.3.39 READ_POUT (96h)
Format Linear

Description The READ_POUT command returns the output power in watts. Refer to [Equation 6](#) to get the real world value.

Default
Figure 74. READ_POUT Register

| | | | | | | | |
|--------------------|----|----|----|----|--------------------|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| READ_POUT_EXPONENT | | | | | READ_POUT_MANTISSA | | |
| R | | | | | R | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| READ_POUT_MANTISSA | | | | | | | |
| R | | | | | | | |

Table 47. READ_POUT Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-------|--------------------|------|-------|-----|--|
| 15:11 | READ_POUT_EXPONENT | R | | — | 5-bit, two's complement exponent (scaling factor). |
| 10:0 | READ_POUT_MANTISSA | R | | — | 11-bit, two's complement mantissa. |

7.6.2.3.40 READ_PIN (97h)

Format Linear

Description The READ_PIN command returns the input power in watts. Refer to [READ_PIN \(97h\)](#) to get the real world value.

Default

Figure 75. READ_PIN Register

| | | | | | | | |
|-------------------|----|----|----|----|-------------------|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| READ_PIN_EXPONENT | | | | | READ_PIN_MANTISSA | | |
| R | | | | | R | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| READ_PIN_MANTISSA | | | | | | | |
| R | | | | | | | |

Table 48. READ_PIN Register Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-------|-------------------|------|-------|-----|--|
| 15:11 | READ_PIN_EXPONENT | R | | — | 5-bit, two's complement exponent (scaling factor). |
| 10:0 | READ_PIN_MANTISSA | R | | — | 11-bit, two's complement mantissa. |

7.6.2.3.41 PMBus_REVISION (98h)

Format N/A

Description The PMBus_REVISION command returns the revision of the PMBus to which the device is compliant.

Default 11h

Figure 76. PMBus_REVISION Register

| | | | | | | | |
|-------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PMBUS_REV | | | | | | | |
| R-0001 0001 | | | | | | | |

Table 49. PMBus_REVISION Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|-----------|------|-----------|-----|---|
| 7:0 | PMBUS_REV | R | 0001 0001 | — | Compliant to revision 1.1 of the PMBus specification. |

7.6.2.3.42 MFR_ID (99h)

Format N/A

Description The MFR_ID command loads the unit with the text character that contains the manufacturer's ID.

Default ~~!~~~ NVM: 5401h! **~5401h**

Figure 77. MFR_ID Register

| | | | | | | | |
|-------------|----|----|----|----|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| MFR_ID_BW | | | | | | | |
| R/W | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MFR_ID_HC | | | | | | | |
| R-0000 0001 | | | | | | | |

Table 50. MFR_ID Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|------|-----------|------|-----------|-----|-------------------|
| 15:8 | MFR_ID_BW | R/W | | Yes | PMBus Block Write |
| 7:0 | MFR_ID_HC | R | 0000 0001 | — | Hard Coded to 01h |

7.6.2.3.43 MFR_MODEL (9Ah)

| | |
|--------------------|--|
| Format | N/A |
| Description | The MFR_MODEL command loads the unit with the text character that contains the model number of the manufacturer. |
| Default | NVM: 4701h |

Figure 78. MFR_MODEL Register

| | | | | | | | |
|--------------|----|----|----|----|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| MFR_MODEL_BW | | | | | | | |
| R/W | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MFR_MODEL_HC | | | | | | | |
| R-0000 0001 | | | | | | | |

Table 51. MFR_MODEL Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|------|--------------|------|-----------|-----|-------------------|
| 15:8 | MFR_MODEL_BW | R/W | | Yes | PMBus Block Write |
| 7:0 | MFR_MODEL_HC | R | 0000 0001 | — | Hard Coded to 01h |

7.6.2.3.44 MFR_REVISION (9Bh)

| | |
|--------------------|--|
| Format | N/A |
| Description | The MFR_REVISION command loads the unit with the text character that contains the revision number of the manufacturer. This is typically done once at the time of manufacture. |
| Default | |

Figure 79. MFR_REVISION Register

| | | | | | | | |
|------------------|----|----|----|-----------------|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| MFR_REVISION_HC1 | | | | MFR_REVISION_BW | | | |
| R-0000 | | | | R/W | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MFR_REVISION_HC2 | | | | | | | |
| R-0000 0001 | | | | | | | |

Table 52. MFR_REVISION Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-------|------------------|------|-----------|-----|-------------------|
| 15:12 | MFR_REVISION_HC1 | R | 0001 | — | Hard Coded to 0h |
| 11:8 | MFR_REVISION | R/W | | Yes | PMBus Block Write |
| 7:0 | MFR_REVISION_HC2 | R | 0000 0001 | — | Hard Coded to 01h |

7.6.2.3.45 MFR_DATE (9Dh)

Format N/A

Description The MFR_DATE command loads the unit with the text character that identifies the device's date of manufacture. This is typically done once at the time of manufacture.

Default

Figure 80. MFR_DATE Register

| | | | | | | | |
|-------------|----|----|----|----|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| MFR_DATE_BW | | | | | | | |
| R/W | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MFR_DATE_HC | | | | | | | |
| R-0000 0001 | | | | | | | |

Table 53. MFR_DATE Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|------|-------------|------|-----------|-----|--------------------|
| 15:8 | MFR_DATE_BW | R/W | | Yes | PMBus Block Write |
| 7:0 | MFR_DATE_HC | R | 0000 0001 | — | Hard Coded to 01h. |

7.6.2.3.46 MFR_VOUT_MIN (A4h)

Format VID

Description The MFR_VOUT_MIN command sets an lower limit on the output voltage that the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly non-operational level. The device detects that an attempt has been made to program the output to a voltage lower than the value set by the MFR_VOUT_MIN command. The device treats this detection as a warning condition and not a fault condition. If an attempt is made to program the output voltage lower than the limit set by this command, the device responds as follows:

- The commanded output voltage is set to MFR_VOUT_MIN,
- The OTHER bit is set in the STATUS_BYTE,
- The VOUT bit is set in the STATUS_WORD,
- The MFR_VOUT_MIN warning bit is set in the STATUS_VOUT register, and
- The device notifies the host (asserts PMBUS_ALERT).

The data bytes are two bytes, which are in right-justified VID format. The VID table mapping determined by the selected VID protocols (VR12.0 or VR12.5) from the SLEW_MODE pin or MFR_SPECIFIC_13.

Default 0000h

Figure 81. MFR_VOUT_MIN Register

| | | | | | | | |
|--------------|----|----|----|----|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0000 0000 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MFR_VOUT_MIN | | | | | | | |
| R/W | | | | | | | |

Table 54. MFR_VOUT_MIN Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|------|--------------|------|-----------|-----|-----------------------|
| 15:8 | RESERVED | R | 0000 0000 | — | Hard coded to 00h |
| 7:0 | MFR_VOUT_MIN | R/W | 0000 0000 | — | Minimum value for VID |

7.6.2.3.47 MFR_SPECIFIC_00 (Per-Phase Overcurrent Limit) (D0h)

Format N/A

Description The MFR_SPECIFIC_00 command sets the valley-current threshold for the per-phase overcurrent limit. The settings can override the default setting from the OCL-R pin.

Default Pin strap: OCL-R pin
NVM: 08h

Figure 82. MFR_SPECIFIC_00 (Per-Phase Overcurrent Limit) Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|-----|---|---|---|
| Reserved | | | | OCL | | | |
| R-0000 | | | | R/W | | | |

Table 55. MFR_SPECIFIC_00 (Per-Phase Overcurrent Limit) Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|----------|------|--------|-----|--|
| 7:4 | Reserved | R | R-0000 | — | Always set to 0. |
| 3:0 | OCL | R/W | | Yes | 0000: 24A 0001: 27A 0010: 30A 0011: 33A 0100: 36A 0101: 39A 0110: 42A 0111: 45A 1000: 48A 1001: 51A 1010: 54A 1011: 57A 1100: 60A 1101: 63A 1110: 66A 1111: 69A |

7.6.2.3.48 MFR_SPECIFIC_01 (Telemetry Averaging Time) (D1h)

Format

Description The MFR_SPECIFIC_01 command sets the averaging time for telemetry reporting.

Default 50h

Figure 83. MFR_SPECIFIC_01 (Telemetry Averaging Time) Register

| | | | | | | | |
|----------|------------|---|---|----------|-----------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | FILTER_PIN | | | Reserved | FILTER_IV | | |
| R-0 | R/W | | | R-00 | R/W | | |

Table 56. MFR_SPECIFIC_01 (Telemetry Averaging Time) Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|------------|------|-------|-----|--|
| 7 | Reserved | R | 0 | — | Always set to 0. |
| 6:4 | FILTER_PIN | R/W | 101 | — | Averaging Time for Input Power Reporting 000: Bypass. 001: 2 ms 010: 5.5 m 011: 11.5 m 100: 19 ms 101: 50 ms 110: 100 ms 111: 225 ms |
| 3:2 | Reserved | R | 00 | — | Always set to 0. |
| 1:0 | FILTER_IV | R/W | 00 | — | Averaging Time for Current and Voltage Reporting 00: Bypass. 01: .5 ms 10: 1 ms 11: 2.5 ms |

7.6.2.3.49 MFR_SPECIFIC_04 (Read VOUT) (D4h)

Format Linear

Description The MFR_SPECIFIC_04 command returns the actual, measured output voltage in volts. Refer to [Equation 6](#) to get the real world value, where n= -9.

Default

Figure 84. MFR_SPECIFIC_04 (Read VOUT) Register

| | | | | | | | |
|----------------------|----|----|----|----|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| MFR_SPEC_04_MANTISSA | | | | | | | |
| R | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MFR_SPEC_04_MANTISSA | | | | | | | |
| R | | | | | | | |

Table 57. MFR_SPECIFIC_04 (Read VOUT) Register Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|------|----------------------|------|-------|-----|--|
| 15:0 | MFR_SPEC_04_MANTISSA | R | | — | Unsigned 16-bit mantissa with an exponent value of n=-9. |

7.6.2.3.50 MFR_SPECIFIC_05 (VOUT Trim) (D5h)

| | |
|--------------------|---|
| Format | Signed Two's Complement |
| Description | The MFR_SPECIFIC_05 command is used to trim the VR output voltage in volts. LSB resolution is 5 mV/10 mV based on the selected VR12.0/VR12.5. |
| Default | NVM: 00h |

Figure 85. MFR_SPECIFIC_05 (VOUT Trim) Register

| | | | | | | | |
|-----------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VOUT_VID_OFFSET | | | | | | | |
| R/W | | | | | | | |

Table 58. MFR_SPECIFIC_05 (VOUT Trim) Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|-----------------|------|-------|-----|--|
| 7:0 | VOUT_VID_OFFSET | R/W | | Yes | Sets the VR output trim voltage. 01111111: 0.635 V in VR12.0 and 1.27V in VR12.5 01111110: 0.630 V in VR12.0 and 1.26 V in VR12.5 00000001: 0.005 V in VR12.0 and 0.01 V in VR12.5 00000000: 0 V 11111111: –0.005 V in VR12.0 and –0.01 V in VR12.5 10000001: –0.635 V in VR12.0 and –1.27 V in VR12.5 10000000: –0.640 V in VR12.0 and –1.28 V in VR12.5 |

7.6.2.3.51 MFR_SPECIFIC_07 (Additional Function Bits) (D7h)

| | |
|--------------------|--|
| Format | N/A |
| Description | The MFR_SPECIFIC_07 command sets the additional function bits. |
| Default | NVM: 02h |

Figure 86. MFR_SPECIFIC_07 (Additional Function Bits) Register

| | | | | | | | |
|----------|---|---|---|---|-----------|--------------|----------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | SLEW_FAST | OSR_TRISTATE | SST_TIME |
| R-0000 0 | | | | | R/W | | |

Table 59. MFR_SPECIFIC_07 (Additional Function Bits) Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|--------------|------|--------|-----|--|
| 7:3 | Reserved | R | 000 00 | — | Always set to 0. |
| 2 | SLEW_FAST | R/W | | Yes | Fast Slew Mode Enable/Disable 0: Default slew rate selected by MFR_SPECIFIC_13[2:0] 1: Add 1.36 mV/μs to the selected slew rate |
| 1 | OSR_TRISTATE | R/W | | Yes | Body Braking Enable/Disable 0: Enable OSR pulse truncation without body braking 1: Enable OSR pulse truncation with body braking |
| 0 | SST_TIME | R/W | | Yes | Soft Slew Rate Selection 0: soft start slew rate dependent on TRISE 1: 1/16 of the selected slew rate for soft-start |

7.6.2.3.52 MFR_SPECIFIC_08 (Droop) (D8h)

Format N/A
Description The MFR_SPECIFIC_08 command sets the load line as percentage of the default one. For example, if slope is set as 1mohm = 100%, then 0.5mohm = 50%
Default 04h

Figure 87. MFR_SPECIFIC_08 (Droop) Register

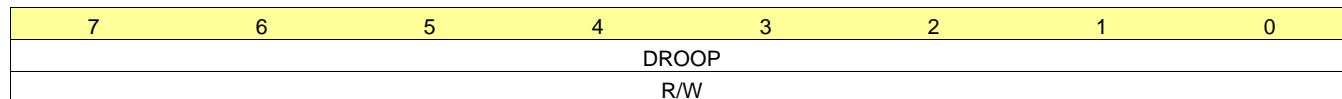


Table 60. MFR_SPECIFIC_08 (Droop) Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|-------|------|--------------|-----|---|
| 7:0 | DROOP | R/W | 0000 0100 | — | 0000 0000: 0% 0000 0001: 25% 0000 0010: 50% 0000 0011: 75% 0000 0100: 100% 0001 0000: 80% 0010 0000: 85% 0011 0000: 90% 0100 0000: 95% 0101 0000: 105% 0110 0000: 110% 0111 0000: 115% 1000 0000: 120% 1001 0000: 125% 1010 0000: 150% 1011 0000: 175% Others: 100% |

7.6.2.3.53 MFR_SPECIFIC_09 (OSR/USR) (D9h)

| | |
|--------------------|--|
| Format | N/A |
| Description | The MFR_SPECIFIC_09 command sets the threshold for OSR and USR control. The setting can override the default setting from the O-USR pin. |
| Default | Pin strap: O-USR pin NVM: 77h |

Figure 88. MFR_SPECIFIC_09 (OSR/USR) Register

| | | | | | | | |
|----------|-----|---|---|----------|-----|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | USR | | | Reserved | OSR | | |
| R-0 | R/W | | | R-0 | R/W | | |

Table 61. MFR_SPECIFIC_09 (OSR/USR) Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|----------|------|-------|-----|---|
| 7 | Reserved | R | 0 | — | Always set to 0. |
| 6:4 | USR | R/W | | Yes | Undershoot Reduction 000: 20 mV 001: 30 mV 010: 60 mV 011: 80 mV 100: 100 mV 101: 120 mV 110: 140 mV 111: USR off |
| 3 | Reserved | R | 0 | — | Always set to 0. |
| 2:0 | OSR | R/W | | Yes | Overshoot Reduction 000: 30 mV 001: 40 mV 010: 60 mV 011: 80 mV 100: 100 mV 101: 120 mV 110: 140 mV 111: OSR off |

7.6.2.3.54 MFR_SPECIFIC_10 (Maximum Operating Current) (DAh)

| | |
|--------------------|---|
| Format | N/A |
| Description | The MFR_SPECIFIC_10 command sets the maximum operating current (IMAX, unit: A) of the converter. The setting can override the default setting from the F-IMAX pin |
| Default | Pin strap: F-IMAX pin NVM: 78h |

Figure 89. MFR_SPECIFIC_10 (Maximum Operating Current) Register

| | | | | | | | |
|------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IMAX | | | | | | | |
| R/W | | | | | | | |

Table 62. MFR_SPECIFIC_10 (Maximum Operating Current) Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|-------|------|-------|-----|--------------------------------|
| 7:0 | IMAX | R/W | | Yes | Set maximum operating current. |

7.6.2.3.55 MFR_SPECIFIC_11 (VBOOT) (DBh)

| | |
|--------------------|---|
| Format | VID |
| Description | The MFR_SPECIFIC_11 command sets the boot voltage in 8-bit VID format. The setting can override the default setting from the VBOOT pin. |
| Default | Pin strap: VBOOT pin NVM: 97h |

Figure 90. MFR_SPECIFIC_11 (VBOOT) Register

| | | | | | | | |
|-------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VBOOT | | | | | | | |
| R/W | | | | | | | |

Table 63. MFR_SPECIFIC_11 (VBOOT) Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|-------|------|-------|-----|---|
| 7:0 | VBOOT | R/W | | Yes | Set the boot voltage according to the selected VID table. |

7.6.2.3.56 MFR_SPECIFIC_12 (Switching Frequency and TRISE) (DCh)

Format N/A

Description The MFR_SPECIFIC_12 command sets the switching frequency and the soft start rise slew rate. The settings can override the default setting from the F-IMAX.

Default Pin strap: F-IMAX pin
NVM: 20h

Figure 91. MFR_SPECIFIC_12 (Switching Frequency and TRISE) Register

| | | | | | | | |
|-----|---|---|----------|---|---|-------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FSW | | | Reserved | | | TRISE | |
| R/W | | | R-0 | | | R/W | |

Table 64. MFR_SPECIFIC_12 (Switching Frequency and TRISE) Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|----------|------|-------|-----|---|
| 7:4 | FSW | R/W | | Yes | Switching Frequency 0000: 300 kHz 0001: 400 kHz 0010: 500 kHz 0011: 600 kHz 0100: 700 kHz 0101: 800 kHz 0110: 900 kHz 0111: 1000 kHz 1000: 350 kHz 1001: 450 kHz 1010: 550 kHz 1011: 650 kHz 1100: 750 kHz 1101: 850 kHz 1110: 950 kHz 1111: 1000 kHz |
| 3:2 | Reserved | R | 0 | — | Always set to 0. |
| 1:0 | TRISE | R/W | | Yes | Soft start rise slew rate in terms of VOUT slew rate 00: 1 01: 1/2 10: 1/4 11: 1/8 |

7.6.2.3.57 MFR_SPECIFIC_13 (Slew Rate and Other Operation Modes) (DDh)

Format N/A

Description The MFR_SPECIFIC_13 command sets the slew rates and the operation modes. The settings can override the default setting from the SLEW-MODE pin.

Default Pin strap: SLEW-MODE pin
NVM: 89h

Figure 92. MFR_SPECIFIC_13 (Slew Rate and Other Operation Modes) Register

| | | | | | | | |
|-----------|--------|----------|--------|---------|------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VR12_MODE | PI_SET | Reserved | DPS_EN | ZLL_SET | SLEW | | |
| R/W | R/W | R/W | R/W | R/W | R/W | | |

Table 65. MFR_SPECIFIC_13 (Slew Rate and Other Operation Modes) Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|-----------|------|-------|-----|--|
| 7 | VR12_MODE | R/W | | Yes | VR12 Mode 0: VR12.5. 1: VR12.0. |
| 6 | PI_SET | R/W | | Yes | Phase Interleaving 0: 4 phase interleaving individually. 1: 1/3 and 2/4 two phase interleaving |
| 5 | Reserved | R/W | | Yes | Not used, write or read has no effect |
| 4 | DPS_EN | R/W | | Yes | Dynamic Phase Shedding Enable 0: Disable dynamic phase shedding. 1: Enable dynamic phase shedding. |
| 3 | ZLL_SET | R/W | | Yes | Load Line 0: Non-zero load line 1: Zero load line |
| 2:0 | SLEW | R/W | | Yes | Slew Rate 000: 0.34 mV/μs 001: 0.68 mV/μs 010: 1.02 mV/μs 011: 1.36 mV/μs 100: 1.7 mV/μs 101: 2.04 mV/μs 110: 2.38 mV/μs 111: 2.74 mV/μs |

7.6.2.3.58 MFR_SPECIFIC_14 (Ramp Height) (DEh)

| | |
|--------------------|--|
| Format | N/A |
| Description | The MFR_SPECIFIC_14 command sets the ramp amplitude for compensations. The settings can override the default setting from the OCL-R pin. |
| Default | Pin strap: OCL-R pin NVM: 06h |

Figure 93. MFR_SPECIFIC_14 Register

| | | | | | | | |
|----------|---|---|---|---|------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | RAMP | | |
| R-0000 0 | | | | | R/W | | |

Table 66. MFR_SPECIFIC_14 Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|----------|------|-------|-----|--|
| 7:3 | Reserved | R | 0 | — | Always set to 0. |
| 2:0 | RAMP | R/W | | Yes | Ramp Amplitude 000: 20 mV _{PP} 001: 40 mV _{PP} 010: 60 mV _{PP} 011: 80 mV _{PP} 100: 100 mV _{PP} 101: 120 mV _{PP} 110: 150 mV _{PP} 111: 200 mV _{PP} |

7.6.2.3.59 MFR_SPECIFIC_15 (Dynamic Phase Shedding Thresholds) (DFh)

| | |
|--------------------|---|
| Format | N/A |
| Description | The MFR_SPECIFIC_15 command sets the threshold for the dynamic phase shedding. Use 4 x overcurrent limit (OCL) as 100% load condition |
| Default | NVM: 01h |

Figure 94. MFR_SPECIFIC_15 (Dynamic Phase Shedding Thresholds) Register

| | | | | | | | |
|----------|---|---|---|------------|-------------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | DPS_TH_LOW | DPS_TH_HIGH | | |
| R-0000 | | | | R/W | R/W | | |

Table 67. MFR_SPECIFIC_15 (Dynamic Phase Shedding Thresholds) Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|-------------|------|-------|-----|---|
| 7:4 | Reserved | R | 0000 | — | Always set to 0. |
| 3 | DPS_TH_LOW | R/W | | Yes | Switch from 2 Phase to 1 Phase Operation 0: Disable decreasing to 1 phase operation. 1: 10% load. |
| 2:0 | DPS_TH_HIGH | R/W | | Yes | Switch from 4 Phase to 2 Phase Operation 000: 15% load. 001: 20% load. 010: 25% load. 011: 30% load. Others: 35% load. |

7.6.2.3.60 MFR_SPECIFIC_16 (VIN UVLO) (E0h)

| | |
|--------------------|---|
| Format | N/A |
| Description | The MFR_SPECIFIC_16 command sets the threshold for the VIN Undervoltage Lockout (UVLO). |
| Default | NVM: 01h |

Figure 95. MFR_SPECIFIC_16 (VIN UVLO) Register

| | | | | | | | |
|-----------|---|---|---|---|---|----------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | | VIN_UVLO | |
| R-00 0000 | | | | | | R/W | |

Table 68. MFR_SPECIFIC_16 (VIN UVLO) Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|----------|------|---------|-----|--|
| 7:2 | Reserved | R | 00 0000 | — | Always set to 0. |
| 1:0 | VIN_UVLO | R/W | 01 | Yes | Input Voltage UVLO 00: 4.5 V 01: 7.25 V 10: 9.0 V 11: 10.3 V |

7.6.2.3.61 MFR_SPECIFIC_20 (Maximum Operational Phase Number) (E4h)

| | |
|--------------------|--|
| Format | N/A |
| Description | The MFR_SPECIFIC_20 command sets the maximum operational phase numbers on-the-fly. If the maximum operational phase number is set higher than the available phase numbers specified by hardware, then the operational phase number remains unchanged, and the STAUTS_MFR_SPECIFIC<3> is set while asserting PMB_ALERT. |
| Default | Hardware Specific |

Figure 96. MFR_SPECIFIC_20 (Maximum Operational Phase Number) Register

| | | | | | | | |
|----------|---|---|---|---|-----------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | PHASE_NUM | | |
| R-0 0000 | | | | | R/W | | |

Table 69. MFR_SPECIFIC_20 (Maximum Operational Phase Number) Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|-----------|------|--------|-----|---|
| 7:3 | Reserved | R | 0 0000 | — | Always set to 0. |
| 2:0 | PHASE_NUM | R/W | | — | Phase Number 000: 1-phase operation. 001: 2-phase operation. 010: 3-phase operation. 011: 4-phase operation. 100: 5-phase operation. 101: 6-phase operation. Others: |

7.6.2.3.62 MFR_SPECIFIC_22 (VOUT_UV_FAULT_threshold) (E6h)

| | |
|--------------------|---|
| Format | N/A |
| Description | The MFR_SPECIFIC_22 command sets the value of VOUT undervoltage threshold. UVP threshold = VOUT_COMMAND - Load Line * Iout - VOUT_UVF_OFFSET |
| Default | NVM: 03h |

Figure 97. MFR_SPECIFIC_22 (VOUT_UV_FAULT_threshold) Register

| | | | | | | | |
|----------|---|---|---|---|--------------------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | VOUT_UVF_THRESHOLD | | |
| R-0 0000 | | | | | R/W | | |

Table 70. MFR_SPECIFIC_22 (VOUT_UV_FAULT_threshold) Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|-----|-----------------|------|--------|-----|---|
| 7:3 | Reserved | R | 0 0000 | — | Always set to 0. |
| 2:0 | VOUT_UVF_OFFSET | R/W | | Yes | VOUT UVF threshold 000: 50 mV 001: 100 mV 010: 150 mV 011: 200 mV 100: 250 mV 101: 300 mV 110: 325 mV 111: 400 mV |

7.6.2.3.63 MFR_SPECIFIC_44 (DEVICE_CODE) (FCh)
Format
Description The MFR_SPECIFIC_44 command reads back the DEVICE_CODE information.

Default $\sim 01F0h$ $\sim 01F0h$
Figure 98. MFR_SPECIFIC_44 (DEVICE_CODE) Register

| | | | | | | | |
|-------------|----|----|----|----|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DEVICE_CODE | | | | | | | |
| R-0000 0001 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DEVICE_CODE | | | | | | | |
| R-1111 0000 | | | | | | | |

Table 71. MFR_SPECIFIC_44 (DEVICE_CODE) Register Field Descriptions

| Bit | Field | Type | Reset | NVM | Description |
|------|-------------|------|------------------------------|-----|-------------|
| 15:0 | DEVICE_CODE | R | 0000 0001 1111 0000 | — | Device Code |

8 Application and Implementation

8.1 Application Information

The TPS53647 device has a very simple design procedure. Please contact your local Texas Instruments representative to get a copy of our excel-based design tool spreadsheet. This design describes a typical 4-phase, 1 V, 120 A output application with pinstrap mode.

8.2 Typical Application

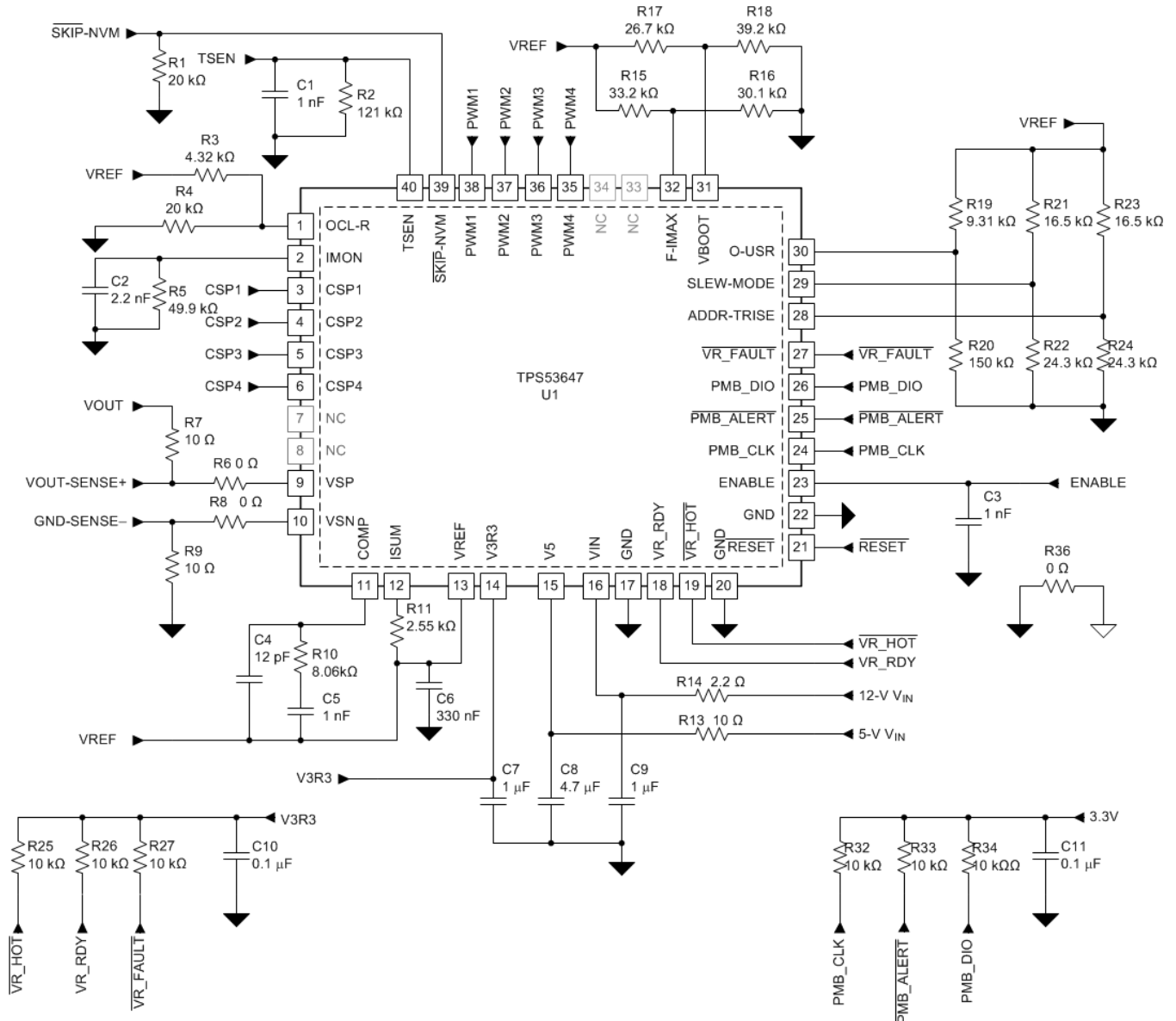


Figure 99. Controller Schematic for a 4-Phase, 1 V, 120 A Application

Typical Application (continued)

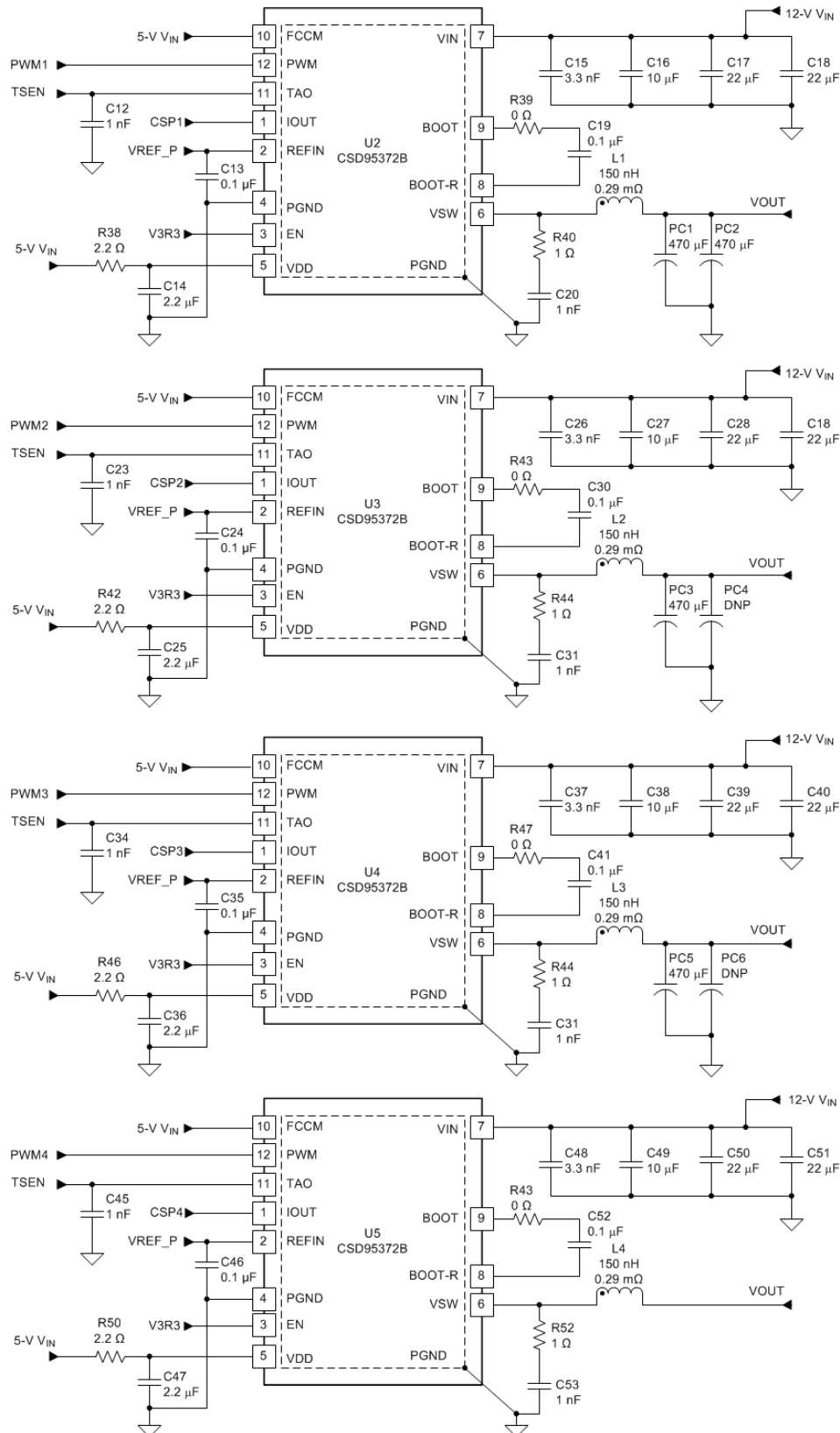


Figure 100. Power Stage Schematic for a 4-Phase, 1V/120A Application

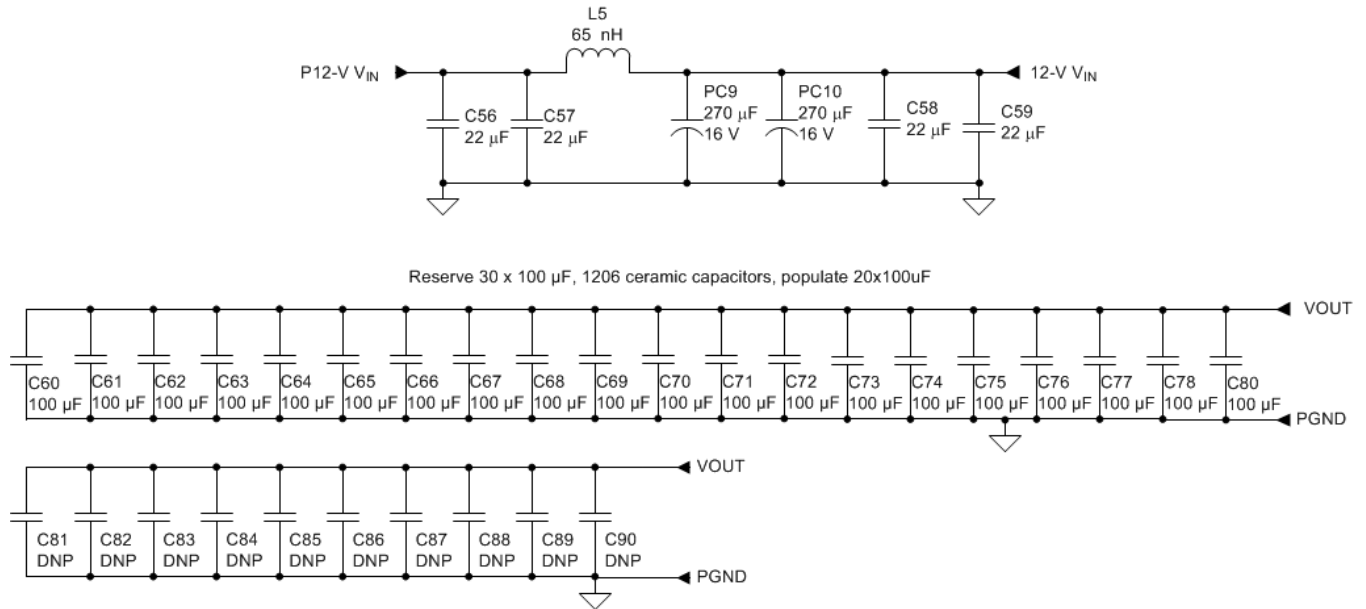


Figure 101. Input and Output Filter for a 4-Phase, 1 V, 120 A Application

8.2.1 Design Requirements

- 4-phase, 1 V, 120 A output
- Number of phases: 4
- Input Voltage 10.8 V – 13.2 V
- I_{max} : 120 A
- Load-line: Zero Load Line
- Boot voltage, V_{BOOT} : 1.0 V
- PMBus Address: 1110001 (bin)

8.2.2 Detailed Design Procedure

For this design, complete the following steps:

1. [Select Switching Frequency](#)
2. [Set the Maximum Output Current](#)
3. [Select the Soft-Start Slew Rate](#)
4. [Select the Operation Mode](#)
5. [Choose Inductor](#)
6. [Select the Per-Phase Valley Current Limit and Ramp Level](#)
7. [Set the Load Line](#)
8. [Set the BOOT Voltage](#)
9. [Set OSR/USR Thresholds for Improving Load Transient Performance](#)
10. [Determine Digital Current Monitor \(IMON\) Gain and Filter Setting](#)
11. [Adjust Compensation Design](#)
12. [Set the PMBus Addresses](#)
13. [Program the Device with the PMBus](#)

8.2.2.1 Select the Switching Frequency

The value of a resistor (R_F) between the F-IMAX pin and GND selects the switching frequency. The frequency is an approximate frequency and is expected to vary based on load and input voltage.

Table 72. Frequency Selection Table

| SELECTION RESISTOR (R_F) VALUE (k Ω) | OPERATING FREQUENCY (f_{sw}) (kHz) |
|---|---|
| 20 | 300 |
| 24 | 400 |
| 30 | 500 |
| 39 | 600 |
| 56 | 700 |
| 75 | 800 |
| 100 | 900 |
| 150 | 1000 |

For this design, choose 500 kHz for the switching frequency. So, $R_F = 30 \text{ k}\Omega$.

8.2.2.2 Set the Maximum Output Current (I_{MAX})

The voltage on the F-IMAX pin sets the maximum output current from the value of the resistors connected from the VREF pin to the F-IMAX pin (R_{IMAX}). Equation 7 shows the maximum output current calculation.

NOTE

The default total overcurrent threshold is 125% of I_{MAX}

$$I_{MAX} = 255 \times \frac{R_F}{(R_F + R_{IMAX})} \quad (7)$$

Use Equation 8 to calculate R_{IMAX} .

$$R_{IMAX} = \frac{R_F \times (255 - I_{MAX})}{I_{MAX}} \quad (8)$$

From Table 72, $R_F = 30 \text{ k}\Omega$. Selecting the closest *standard* resistor value, $R_{IMAX} = 33.2 \text{ k}\Omega$

NOTE

The tolerance of the R_F and R_{IMAX} resistors affect I_{IMAX} value. If the design requires an accurate I_{IMAX} is needed, select an R_F and an R_{IMAX} value with tight tolerance (0.5% or 0.1%).

8.2.2.3 Select the Soft-Start Slew Rate

To select the soft-start slew rate, the first step is to select the output voltage change slew rate. The resistor (R_{SLEW}) (connected between the SLEW-MODE pin and GND) sets the output voltage change slew rate when using VOUT_COMMAND. Table 73 show a summary of these settings. For a minimum 0.68-mV/ μ s slew rate, the resistor $R_{SLEW} = 24.3 \text{ k}\Omega$.

Table 73. Vout Change Slew Rate Selection

| SELECTION RESISTOR $R_{SLEW} \text{ (k}\Omega\text{)}$ | MINIMUM SLEW RATE $\text{(mV}/\mu\text{s)}$ |
|---|---|
| 20 | 0.34 |
| 24 | 0.68 |
| 30 | 1.02 |
| 39 | 1.36 |
| 56 | 1.7 |
| 75 | 2.04 |
| 100 | 2.38 |
| 150 | 2.74 |

After determining the V_{OUT} change slew rate, select the ratio of soft-start rate versus V_{OUT} change slew rate. Select a value for resistor R_{ADDR} (the resistor between ADDR_TRISE pin and GND) to configure this ratio.

Table 74. Soft-Start Slew Rate Selection

| SELECTION RESISTOR $R_{ADDR} \text{ (k}\Omega\text{)}$ | MINIMUM SLEW RATE $\text{(mV}/\mu\text{s)}$ |
|---|---|
| 20 or 24 | 1 |
| 30 or 39 | 1/2 |
| 56 or 75 | 1/4 |
| 100 or 150 | 1/8 |

In this design, the soft-start slew rate is the same as V_{out} change slew rate. So $R_{ADDR}=20k$ or $24k$ is selected. The LSB of BOOT voltage VID determines the value of R_{ADDR} as described in [Set the BOOT Voltage](#). If slower soft start is desired, higher R_{ADDR} can be used to set soft-start slew rate to be 1/2, 1/4 or 1/8 of output voltage change slew rate.

8.2.2.4 Select the Operation Mode

The resistor (R_{MODE}) is connected between the VREF pin and the SLEW-MODE pin. After selecting the value of R_{SLEW} , set the operation mode by choosing the voltage on the SLEW-MODE pin as summarized in [Table 75](#) and the [Electrical Characteristics](#) table. In this design, VR 12.0 mode is selected with 4-phase interleaving, disabled dynamic phase shedding, and zero load-line. As described in the [Select the Soft-Start Slew Rate](#) section, use the value $R_{SLEW} = 24\text{ k}\Omega$, so $R_{MODE} = 16.5\text{ k}\Omega$ to select the desired operating modes.

Table 75. Operation Mode with Resistor Selection

| OPERATION MODES BIT | | BIT DESCRIPTION | |
|---------------------|----------------|----------------------|---|
| Mode bit M_3 | MFR_SPEC_13<7> | VR12 _{MODE} | 0: VR12.5 (Use VR12.5 VID table) |
| | | | 1: VR12.0 (Use VR12.0 VID table) |
| Mode bit M_2 | MFR_SPEC_13<6> | PI _{SET} | 0: 4 phase interleaving individually |
| | | | 1: 1/3 and 2/4 phase interleaving |
| Mode bit M_1 | MFR_SPEC_13<4> | DPS _{EN} | 0: Disable dynamic phase shedding |
| | | | 1: Enable dynamic phase shedding |
| Mode bit M_0 | MFR_SPEC_13<3> | ZLL _{SET} | 0: Non-zero load-line |
| | | | 1: Zero load-line |

8.2.2.5 Choose Inductor

Smaller inductance values yield better transient performance, but also have a higher ripple and lower efficiency. Higher inductance values have the opposite characteristics. It is common practice to limit the ripple current to between 20% and 50% of the maximum per-phase current. In this design example, 40% of the maximum per-phase current is used.

$$I_{P_P} = \left(\frac{I_{MAX}}{n} \right) \times \%V_{RIPPLE} = \left(\frac{120}{4} \right) \times 0.4 = 12\text{ A} \quad (9)$$

$$L = \frac{V \times dT}{I_{P_P}} = \frac{(V_{IN(max)} - V_{OUT}) \times \frac{V_{OUT}}{(f_{SW} \times V_{IN(max)})}}{I_{P_P}} = 154\text{ nH} \quad (10)$$

The inductor with a value of 150 nH and saturation current of $I_{SAT} = 61\text{ A}$ at 100°C is selected for this application. This saturation current level can be used to determine the OCL level. So the I_{OCL} is selected to be 48 A to use in the OCL resistor calculation in [Equation 11](#).

$$I_{OCL} = I_{SAT} - I_{P_P(actual)} = 61 - 12.32 = 48.68\text{ A} \quad (11)$$

8.2.2.6 Select the Per-Phase Valley Current Limit And Ramp Level

The per-phase, valley current limit is selected by the resistor (R_{OCL}) from OCL-R pin to GND as shown in [Table 76](#). The RAMP is set by the voltage on OCL_R pin with resistor (R_{RAMP}) from OCL_R pin to VREF. The current limit is selected so that the output current OCL is higher than the maximum per-phase current to allow sufficient room for current increase during load transient while the peak inductor current is still lower saturation current level.

Table 76. Per-Phase Valley Current Limit vs Resistor Selection

| $V_{OCL}(V)$ | $R_{OCL-R} (k\Omega)$ | PER-PHASE VALLEY CURRENT LIMIT (A) |
|--------------|-----------------------|------------------------------------|
| ≤ 0.85 | 20 | 24 |
| | 24 | 27 |
| | 30 | 30 |
| | 39 | 33 |
| | 56 | 36 |
| | 75 | 39 |
| | 100 | 42 |
| | 150 | 45 |
| ≥ 0.95 | 20 | 48 |
| | 24 | 51 |
| | 30 | 54 |
| | 39 | 57 |
| | 56 | 60 |
| | 75 | 63 |
| | 100 | 66 |
| | 150 | 69 |

Table 77. Ramp Level vs OCL_R Pin Voltage Selection

| $V_{OCL-R} (V)$ | RAMP LEVEL (mV _{p-p}) |
|---|----------------------------------|
| 0.2 \pm 50 mV or 1.0 \pm 50 mV | 40 |
| 0.4 \pm 50 mV or 1.2 \pm 50 mV | 80 |
| 0.6 \pm50 mV or 1.4 \pm50 mV | 150 |
| 0.8 \pm 50mV or 1.6 \pm 50mV | 200 |

In this design example, a 48-A valley current limit is selected, so R_{OCL} is chosen as 20 k Ω .

In this example, a ramp voltage of 150 mV is chosen. The user may chose a lower ramp value to improve transient performance if jitter performance is less of a concern. This value depends on the board layout and individual layout requirements.

Table 76 notes that V_{OCL} must be ≥ 1.0 V. Table 77 shows that for a 150- mV ramp, V_{OCL} must be 1.4 V, therefore the value of the resistor placed between the OCL-R pin and the VREF pin (R_{OCL-R}) should be 4.32 k Ω .

8.2.2.7 Set the Load-Line

The load-line is set by the resistor, R_{ISUM} , from ISUM pin to VREF. Please note a 0 Ω resistor will be used since load line setting is not required for this design example.

The below procedure is provided for applications when a 1.05 m Ω load line is needed.

$$R_{ISUM} = R_{LL} \times \frac{1}{g_{M(isum)} \times R_{CS} \times A_{CS}} = 1.05m\Omega \times \frac{1}{0.5mS \times 5m\Omega \times \frac{1}{6}} = 2.52k\Omega$$

where

- R_{LL} is the desired load-line
- $g_{M(isum)}$ is the ISUM amplifier transconductance
- R_{CS} is the current-sensing gain from the CSD95372B
- A_{CS} is the internal gain

(12)

Because the sensed current from the CSD95372B device is temperature-compensated, a NTC network is not required to achieve a simple application circuit.

8.2.2.8 Set the BOOT Voltage

The resistor, R_{BOOT} , placed between the VBOOT pin and GND as shown in [Table 78](#) sets bit 3, 2, and 1 of the VID of the BOOT voltage. The voltage on VBOOT pin sets bit 7, 6, 5, 4 of the VID of the BOOT voltage. The resistor between the ADDR_TRISE pin and GND sets bit 0 of VID of the BOOT voltage. The BOOT voltage selection also depends on the operation mode selected in the [Select the Operation Mode](#) section. In this design example, 1.0 V is selected as the BOOT voltage in VR12.0 mode, and the VID is 1001 0111, so the $R_{BOOT} = 39$ k Ω , $V_{VBOOT} = 1.009$ V, $R_{ADDR} = 24$ k Ω .

Table 78. Boot Voltage VID Selection (Step 1)

| R_{BOOT} (k Ω) | BOOT VOLTAGE VID |
|--------------------------|------------------|
| | $B_3B_2B_1$ |
| 20 | 000 |
| 24 | 001 |
| 30 | 010 |
| 39 | 011 |
| 56 | 100 |
| 75 | 101 |
| 100 | 110 |
| 150 | 111 |

Table 79. Boot Voltage VID Selection (Step 2)

| V_{VBOOT} (V) | BOOT VOLTAGE VID |
|--|------------------|
| | $B_7B_6B_5B_4$ |
| $V_{VBOOT} \leq 0.053V \pm 20$ mV | 0000 |
| $V_{VBOOT} = 0.159V \pm 20$ mV | 0001 |
| $V_{VBOOT} = 0.226V \pm 20$ mV | 0010 |
| $V_{VBOOT} = 0.372V \pm 20$ mV | 0011 |
| $V_{VBOOT} = 0.478V \pm 20$ mV | 0100 |
| $V_{VBOOT} = 0.584V \pm 20$ mV | 0101 |
| $V_{VBOOT} = 0.691V \pm 20$ mV | 0110 |
| $V_{VBOOT} = 0.797V \pm 20$ mV | 0111 |
| $V_{VBOOT} = 0.903V \pm 20$ mV | 1000 |
| $V_{VBOOT} = 1.009V \pm 20$ mV | 1001 |
| $V_{VBOOT} = 1.116V \pm 20$ mV | 1010 |
| $V_{VBOOT} = 1.222V \pm 20$ mV | 1011 |
| $V_{VBOOT} = 1.328V \pm 20$ mV | 1100 |
| $V_{VBOOT} = 1.434V \pm 20$ mV | 1101 |
| $V_{VBOOT} = 1.541V \pm 20$ mV | 1110 |
| $V_{VBOOT} = 1.615V \pm 10$ mV | 1111 |

Table 80. Boot Voltage VID Selection (Step 3)

| R_{ADDR} (k Ω) | BOOT VOLTAGE VID |
|------------------------------|------------------|
| | B_0 |
| 20 or 30 or 56 or 100 | 0 |
| 24 or 39 or 75 or 150 | 1 |

8.2.2.9 Set OSR/USR Thresholds to Improve Load Transient Performance

The resistor, R_{OSR} connected between the O-USR pin and GND as shown in [Table 81](#) sets the overshoot reduction (OSR) threshold.

Table 81. OSR Threshold vs Resistor Selection

| R_{O-USR} (k Ω) | OSR THRESHOLD (mV) |
|------------------------------|---------------------|
| 20 | 30 |
| 24 | 40 |
| 30 | 60 |
| 39 | 80 |
| 56 | 100 |
| 75 | 120 |
| 100 | 140 |
| 150 | OFF |

The required OSR setting is based on the load-transient performance and the amount of the actual output capacitance. The suggested method is to start with OSR OFF and perform the load transient per the application requirement. If the overshoot can meet the specification with the chosen output capacitance, then the OSR can be kept OFF. So the resistor R_{OSR} can be selected as 150 k Ω . Otherwise the OSR threshold can be lowered by choosing a lower setting from the [Table 81](#) to reduce the overshoot to meet the specifications.

Once R_{OSR} is selected, the Undershoot Reduction (USR) threshold is set by the voltage on the O-USR pin with the resistor, R_{USR} , from the O-USR pin to VREF as shown in [Table 82](#).

Table 82. USR Threshold vs Voltage Selection

| V_{O-USR} (V) | USR THRESHOLD (mV) |
|--|------------------------|
| $V_{O-USR} \leq 0.3$ | 20 |
| $0.35 \leq V_{O-USR} \leq 0.45$ | 30 |
| $0.55 \leq V_{O-USR} \leq 0.65$ | 60 |
| $0.75 \leq V_{O-USR} \leq 0.85$ | 80 |
| $0.95 \leq V_{O-USR} \leq 1.05$ | 100 |
| $1.15 \leq V_{O-USR} \leq 1.25$ | 120 |
| $1.35 \leq V_{O-USR} \leq 1.45$ | 140 |
| $1.55 \leq V_{O-USR} \leq 1.6$ | OFF |

The design procedure for the USR threshold is similar to the OSR setting. The initial setting of the USR threshold is to start with USR OFF, and then perform the load transient test. If the undershoot can meet the requirement, the USR setting can remain OFF. In this design the USR setting is OFF.

8.2.2.10 Digital Current Monitor (IMON) Gain and Filter Setting

To correctly monitor digital current values, the gain of the analog current monitor should be determined by setting the IMON voltage to 0.85 V for maximum output current I_{MAX} . When PMBus host sends the READ_IOUT command, the current information is reported.

R_{IMON} can be determined by using Equation 13

$$R_{IMON} = \frac{0.85 \text{ V}}{I_{MAX} \times R_{CS} \times SF} = \frac{0.85 \text{ V}}{120 \text{ A} \times 5 \text{ m}\Omega \times \left(\frac{1}{35 \text{ k}\Omega}\right)} = 49.58 \text{ k}\Omega$$

where

- R_{IMON} is the desired impedance on the IMON pin
 - I_{MAX} is the total maximum output current
 - R_{CS} is the current sense gain from CSD95372B
 - SF is the internal current gain scaling factor
- (13)

In this design example, $I_{MAX} = 120 \text{ A}$, so the resistance, R_{IMON} , is calculated as 49.58 k Ω . Use the standard value of 49.99k Ω . A capacitor, C_{IMON} usually connected in parallel with R_{IMON} to provide filtering on the IMON signal. In this design, a C_{IMON} value of 2.2 nF is selected.

8.2.2.11 Compensation Design

A type-II compensator is used with the DCAP+ architecture of TPS53647 as shown in Figure 102. $g_{M(comp)}$ is the COMP amplifier transconductance, which is typically 0.5 mS. R_{COMP} determines the gain and the compensation pole and zero locations. C_{COMPS} determines the compensation zero to increase the phase margin, and C_{COMPP} determines the compensation pole to filter out the high-frequency noise. The actual compensator design needs to be adjusted, based on the experimental test results and the bode plot measurements. In this example, $R_{COMP} = 8.06 \text{ k}\Omega$, $C_{COMPS} = 1 \text{ nF}$, and $C_{COMPP} = 12 \text{ pF}$ to put the compensation zero at 19.7 kHz and the compensator pole at 1.65 MHz.

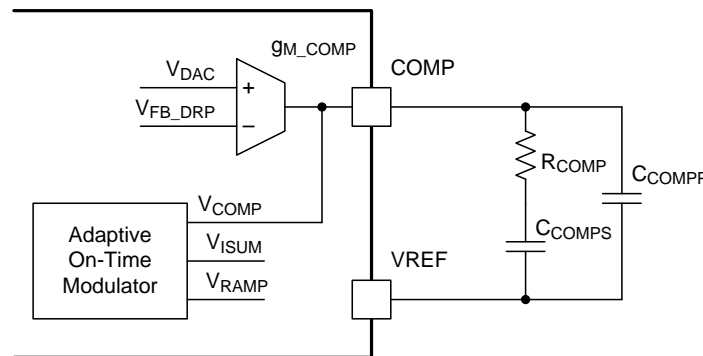


Figure 102. Compensation Circuitry

8.2.2.12 Set PMBus Addresses

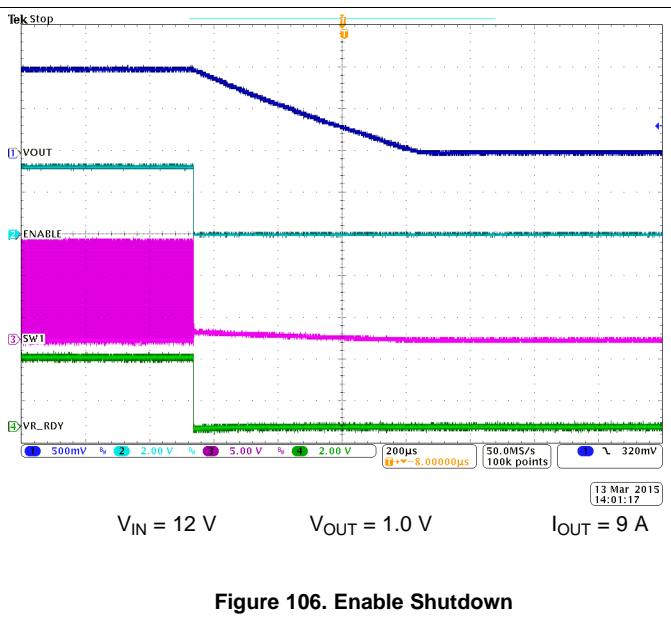
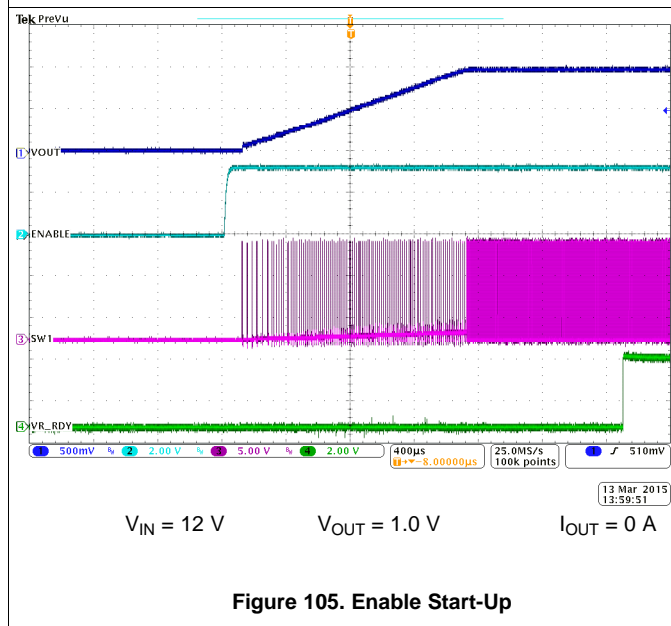
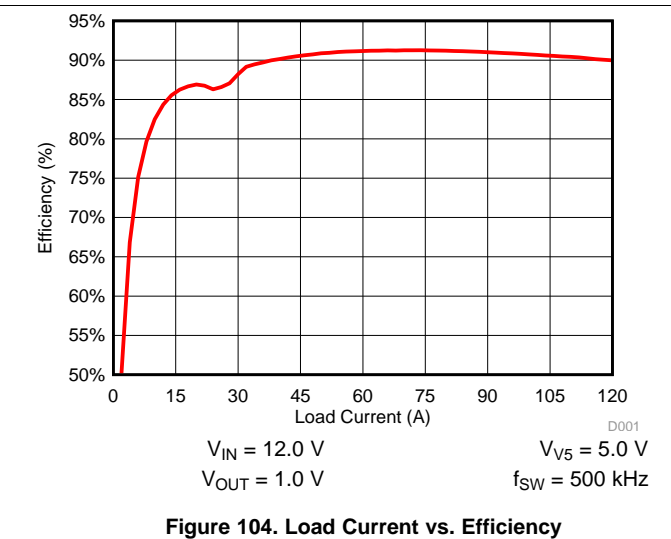
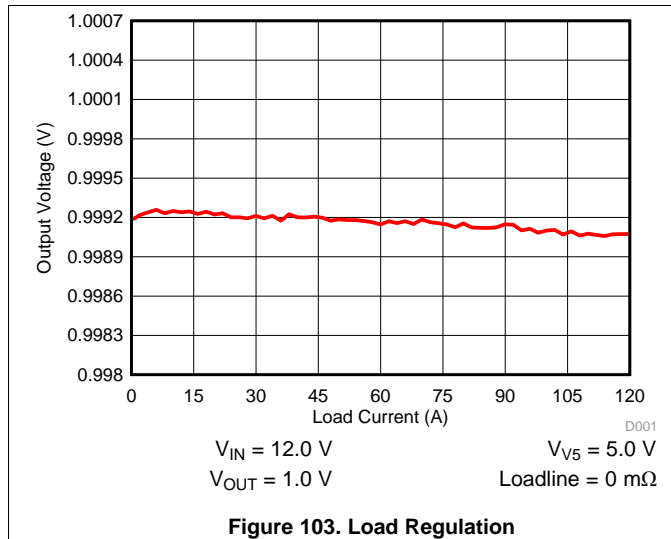
To communicate with system controllers or host with PMBus interfaces, the slave address of the TPS53647 device needs to be set. The voltage on ADDR_TRISE pin sets the PMBus address. Since the resistance of R_{ADDR} is already determined (24 k Ω), The resistance between ADDR_TRISE pin and VREF can be calculated. In this design, PMBUS address of 111 0001 is used. The resistor between ADDR_TRISE and VREF is 16.5 k Ω .

8.2.2.13 Programming the Device with the PMBus

It is optional to use the PMBus interface to program the TPS53647 device since all the settings can be configured externally by using resistors; however, the system controller can override the configurations or can program the device to change the operation modes using the PMBus. The supported PMBus command sets have been introduced in the previous section for the firmware development.

8.2.3 Application Curves

4-Phase, 120-A, full load application



4-Phase, 120-A, full load application

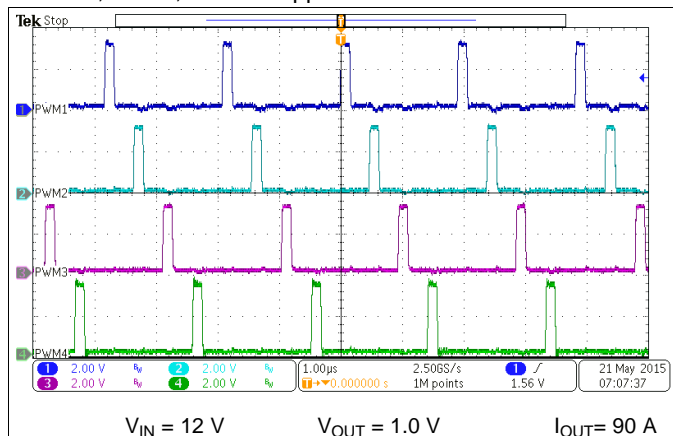


Figure 107. PWM Interleaving

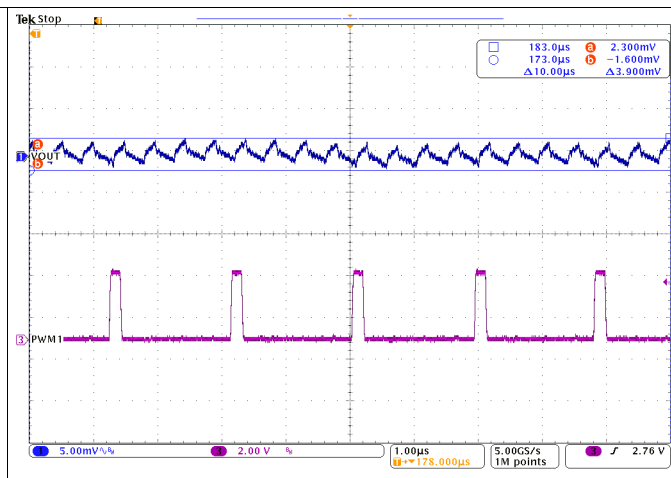


Figure 108. Output Ripple

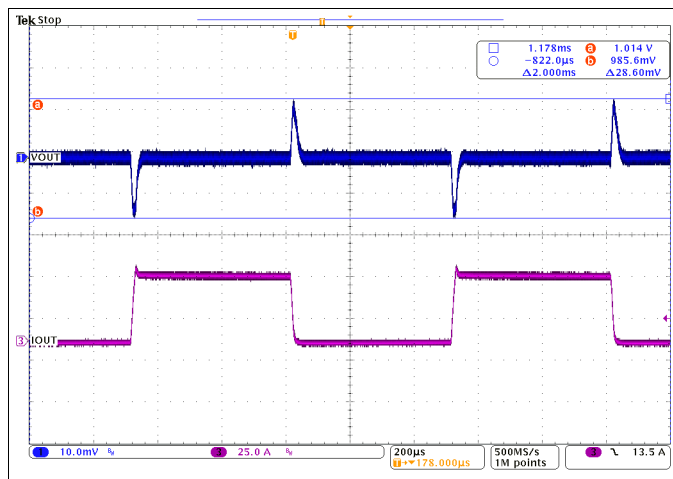


Figure 109. Transient Response

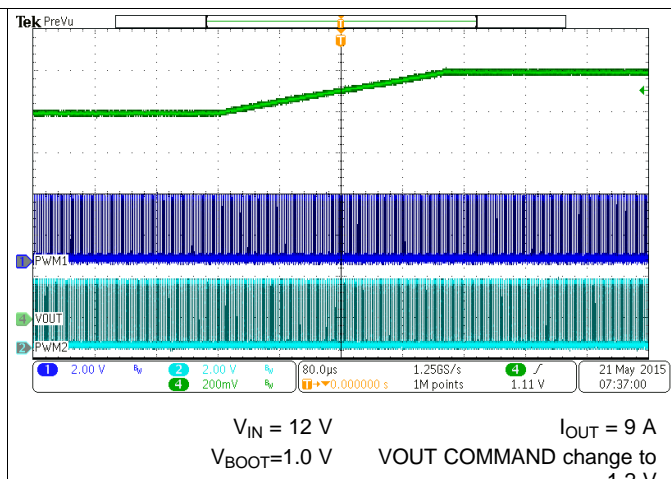


Figure 110. VID Change to 1.2 V

4-Phase, 120-A, full load application

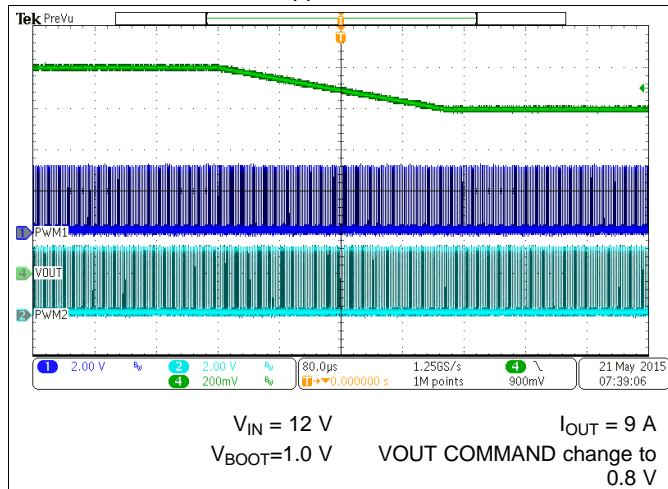


Figure 111. VID Change to 0.8 V

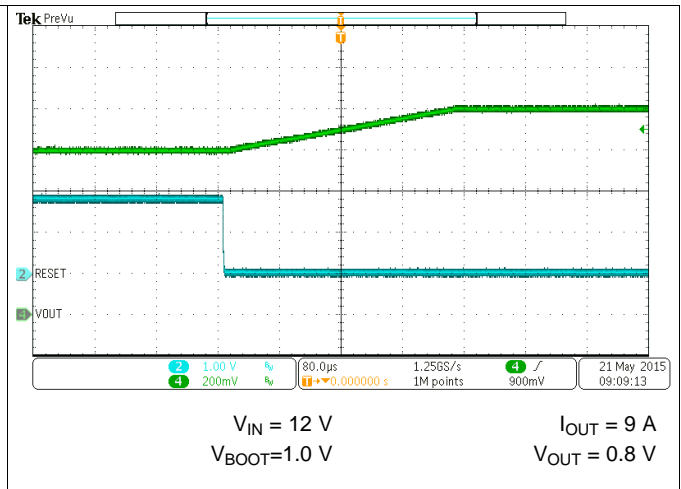


Figure 112. RESET Function ($V_{OUT} = 0.8\text{ V}$)

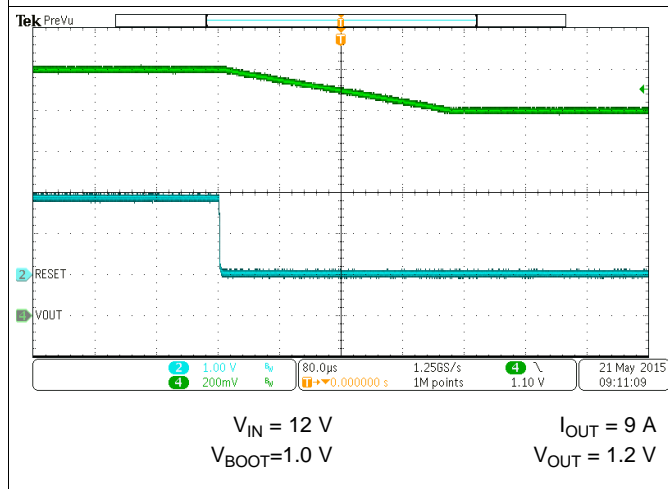


Figure 113. Reset Function ($V_{OUT} = 1.2\text{ V}$)

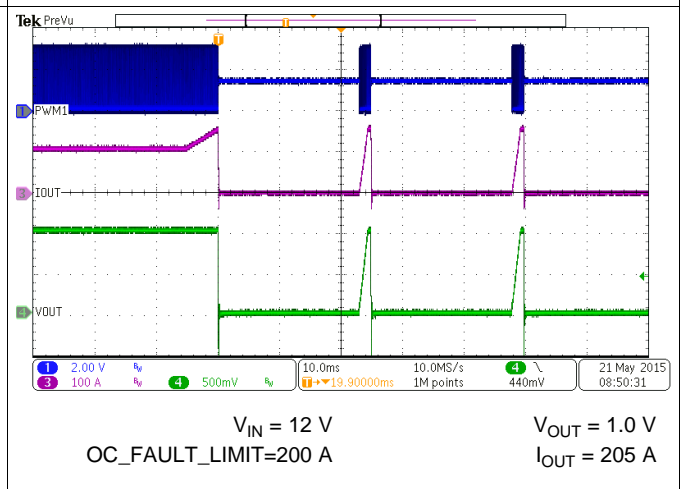


Figure 114. Hiccup mode (OCP)

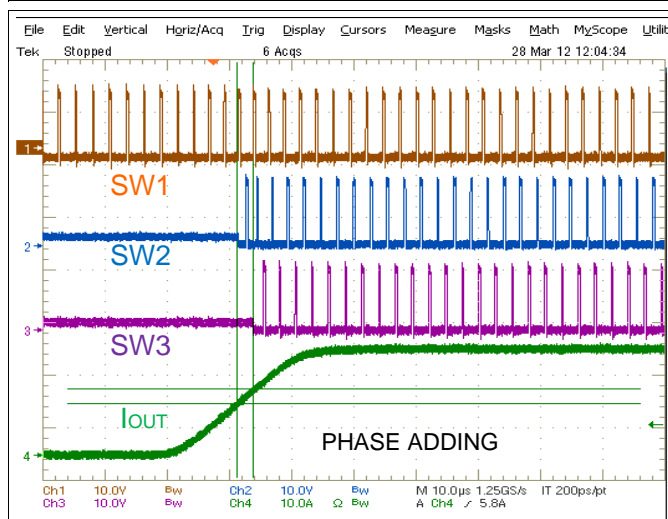


Figure 115. Phase Adding

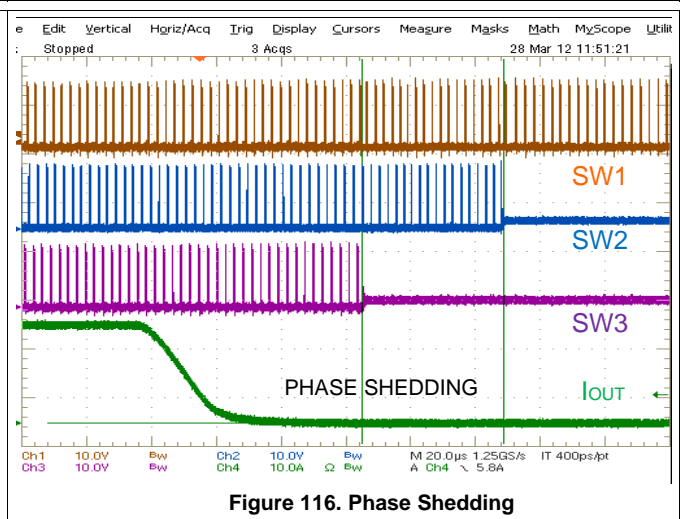
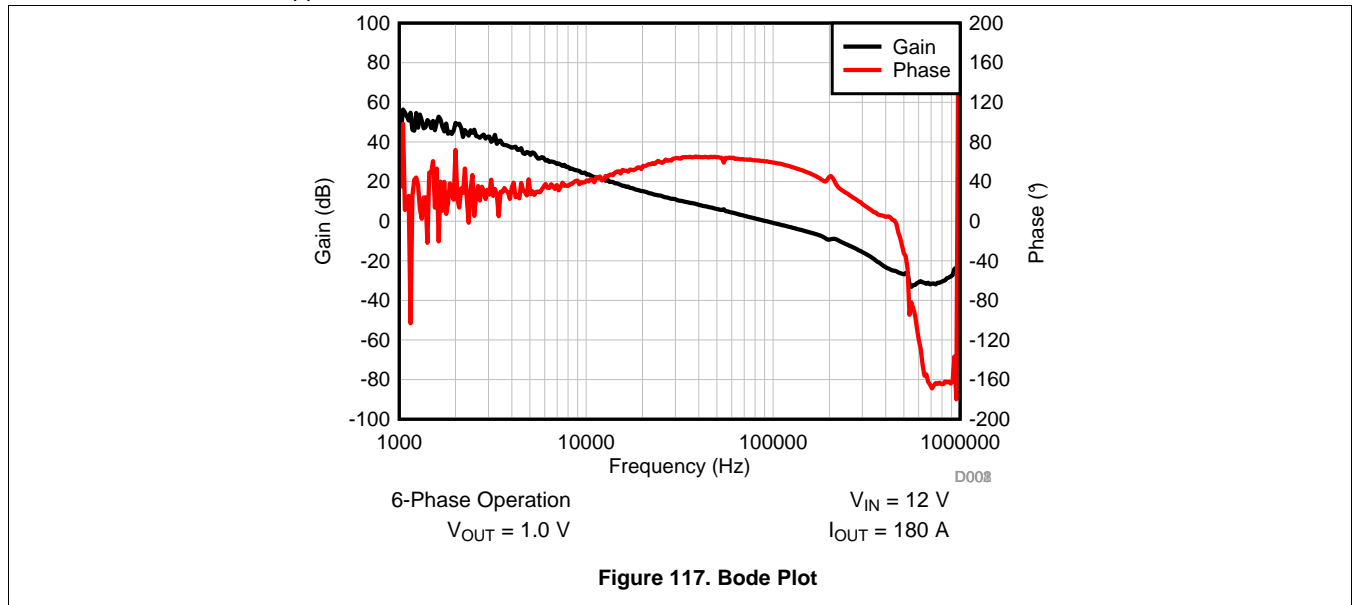


Figure 116. Phase Shedding

4-Phase, 120-A, full load application



9 Power Supply Recommendations

The TPS53647 device operates from a 5-V supply at the V5 pin, and a 12-V supply on the VIN pin. For best results, consider the UVLO range for VIN, V5 pin voltages, use well regulated supplies and use the recommended filter network.

The controller requires 1.2 ms to complete the reading of the pinstrap settings. If the converter is enabled before pinstrap completion, the controller first completes the pinstrap function and then initiated the start-up sequence. After the ENABLE pin voltage goes high, the controller waits for approximately 260 μ s before V_{OUT} begins to ramp up.

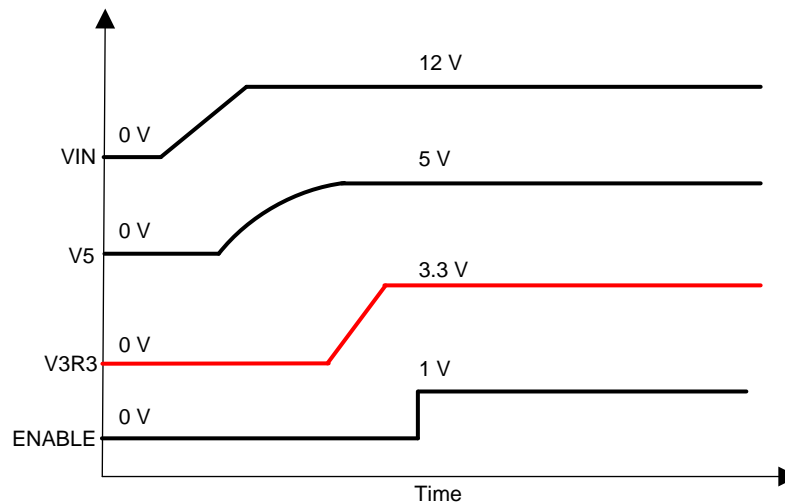


Figure 118. Power Supply Waveforms

10 Layout

10.1 Layout Guidelines

10.1.1 Schematic Review Checklist

- Confirm the pin-out of the controller on schematic to the pin-out of datasheet
- Get a closest TI reference design to check for connection and component values
- Have a component value design tool ready to check component values.
- Carefully confirm the choice of inductor and DCR (see the [Detailed Design Procedure](#) section).
- Carefully confirm the choice of output capacitors (see the [Detailed Design Procedure](#) section).
- Confirm the polarity of the differential pair of voltage sensing (VSP/VSN).
- Confirm the current sensing feedback and reference voltage of TI smart power stages (ex: CSD95372BQ5MC).
- A separated IC ground (analog ground) is recommended but not a must.

10.1.2 PCB Design Guidelines

Most Critical Layout Requirement

Separate noisy driver interface lines from sensitive analog lines.

The TPS53647 device makes this separation easy. The power stage (CSD95372B) is outside of the TPS53647 device. So all gate-drive and switch-node traces must be local to the inductor and the MOSFETs.

10.1.2.1 Layer Stack-up, 8-Layer PCB as example

- Top Layer: VIN, VOUT, power ground and analog ground
- Layer 2: Power ground
- Layer 3: VIN, VREF, VOUT, PWM signals, and current sense signals
- Layer 4: Power ground, analog ground, and VOUT plane
- Layer 5: Power ground, V3R3, and VOUT plane
- Layer 6: V5, VIN and VOUT plane
- Layer 7: Power ground
- Bottom Layer: VIN, VOUT, power ground, analog ground, and feedbacks

Layout Guidelines (continued)

10.1.2.2 Current Sensing Lines

Given the physical layout of most systems, the current feedback (CSPx) may have to pass near the power chain. Clean current feedback is required for good load-line, current sharing, and current limiting performance of the TPS53647, so please take the following precautions:

- Run the current feedback signals in the VREF plane as shown in [Figure 119](#).
- Recommended trace width is 8-10 mil
- The distance of each trace should be larger than 20 mil

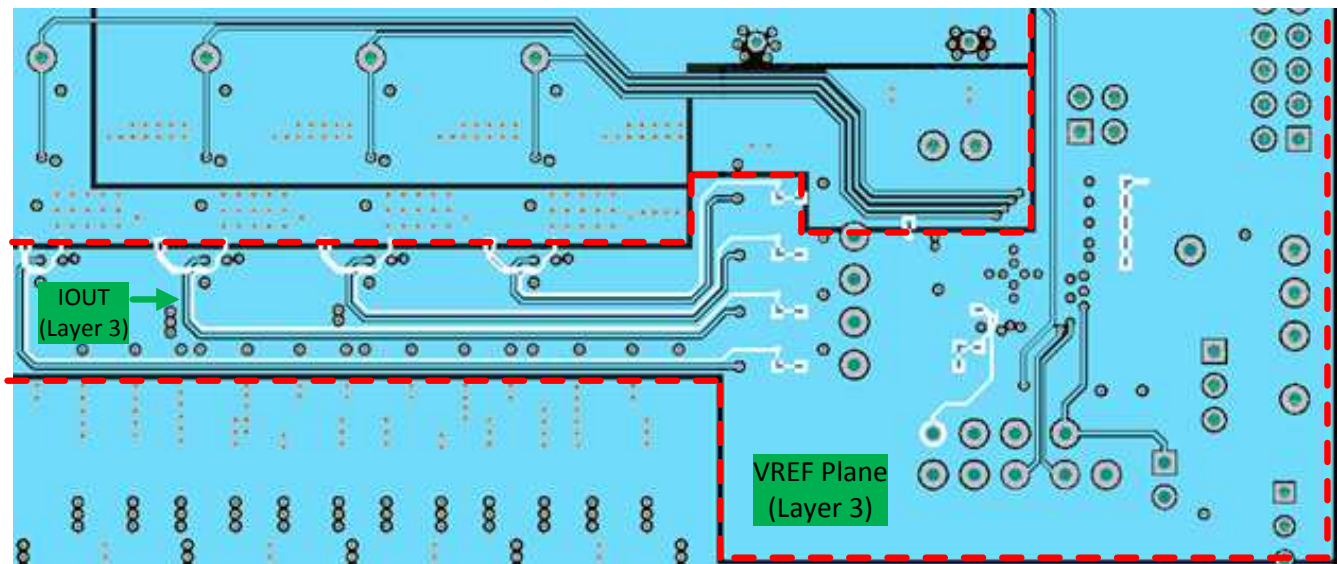


Figure 119. Layout Example of Current Sensing Traces

10.1.2.3 Feedback Voltage Sensing Lines

The voltage feedback coming from the load must be routed as differential pair (distance ≤ 10 mil) all the way to the TPS53647 VSP and VSN pins. Recommended trace width is 8-10 mil. Care should be taken to avoid routing over switch-node traces.

Layout Guidelines (continued)

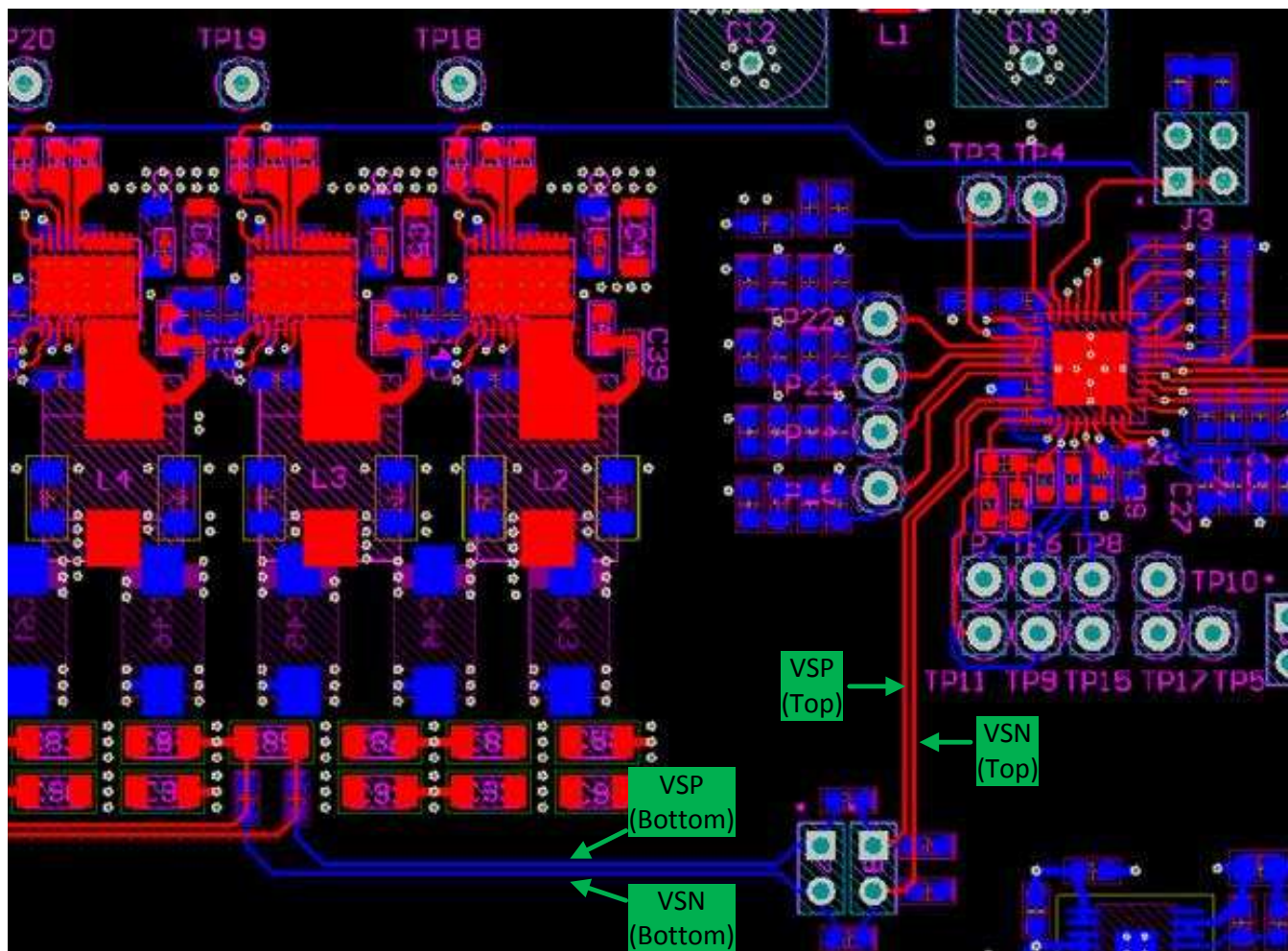


Figure 120. Layout Example for Feedback Voltage Sensing Traces

10.1.2.4 PWM Lines

The PWM lines should be routed from the (TPS53647) device to the power stage (CSD95372B) without crossing any switch-node signals.

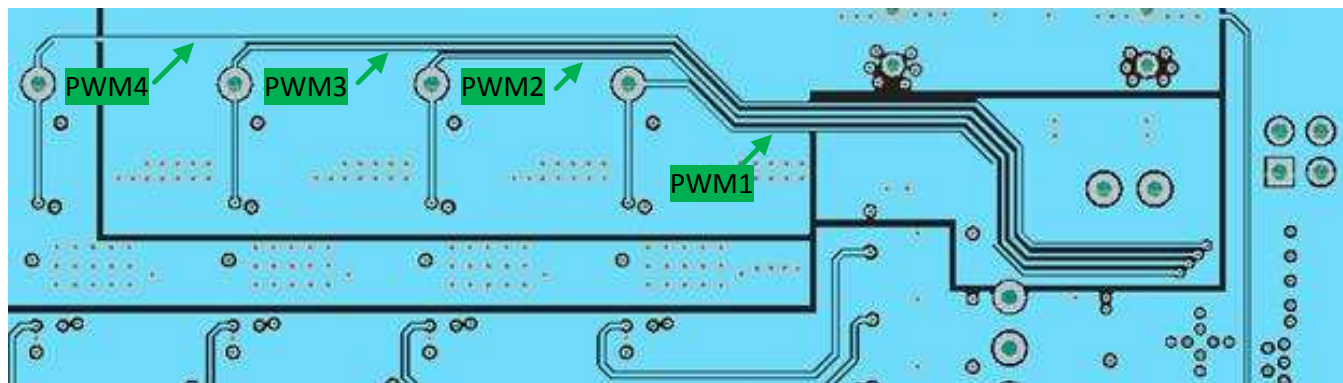


Figure 121. Layout Example for PWM Traces

Layout Guidelines (continued)

10.1.2.5 Power Chain Symmetry

The TPS53647 device does not require special care in the layout of the power chain components. This is because independent isolated current feedback is provided. If it is possible to lay out the phases in a symmetrical manner, then please do so. The rule is: the current feedback from each phase needs to be clean of noise and have the same effective current sense resistance.

Layout Guidelines (continued)

10.1.2.6 Placing Analog Signal Components

Place components close to the TPS53647 device in the following order, as shown in [Figure 122](#):

1. COMP pin and ISUM pin compensation components must be put on the same side of the controller as shown in. Recommended trace width is 8-10 mil.
2. Decoupling capacitors for VREF, V3R3, and V5 must be put on the same side of the controller as shown in. Recommended trace width is 8-10 mil.
 - Decouple VREF to GND with at most 0.47-uF ceramic capacitor.
 - Decouple V3R3 to GND with at least 1-uF ceramic capacitor.
 - Decouple V5 to GND with at least 4.7-uF ceramic capacitor. A 1-Ω resistor between 5V supply voltage and V5 pin is also recommended as a filter.
 - Decouple VIN to GND with at least 1-uF ceramic capacitor. A 1-Ω resistor between 12V supply voltage and VIN pin is also recommended as a filter.
3. OCL-R resistors, F-IMAX resistors, SLEW-MODE resistors, VBOOT resistors, IMON resistor, and O-USR resistors. Recommended trace width is 8-10 mil.

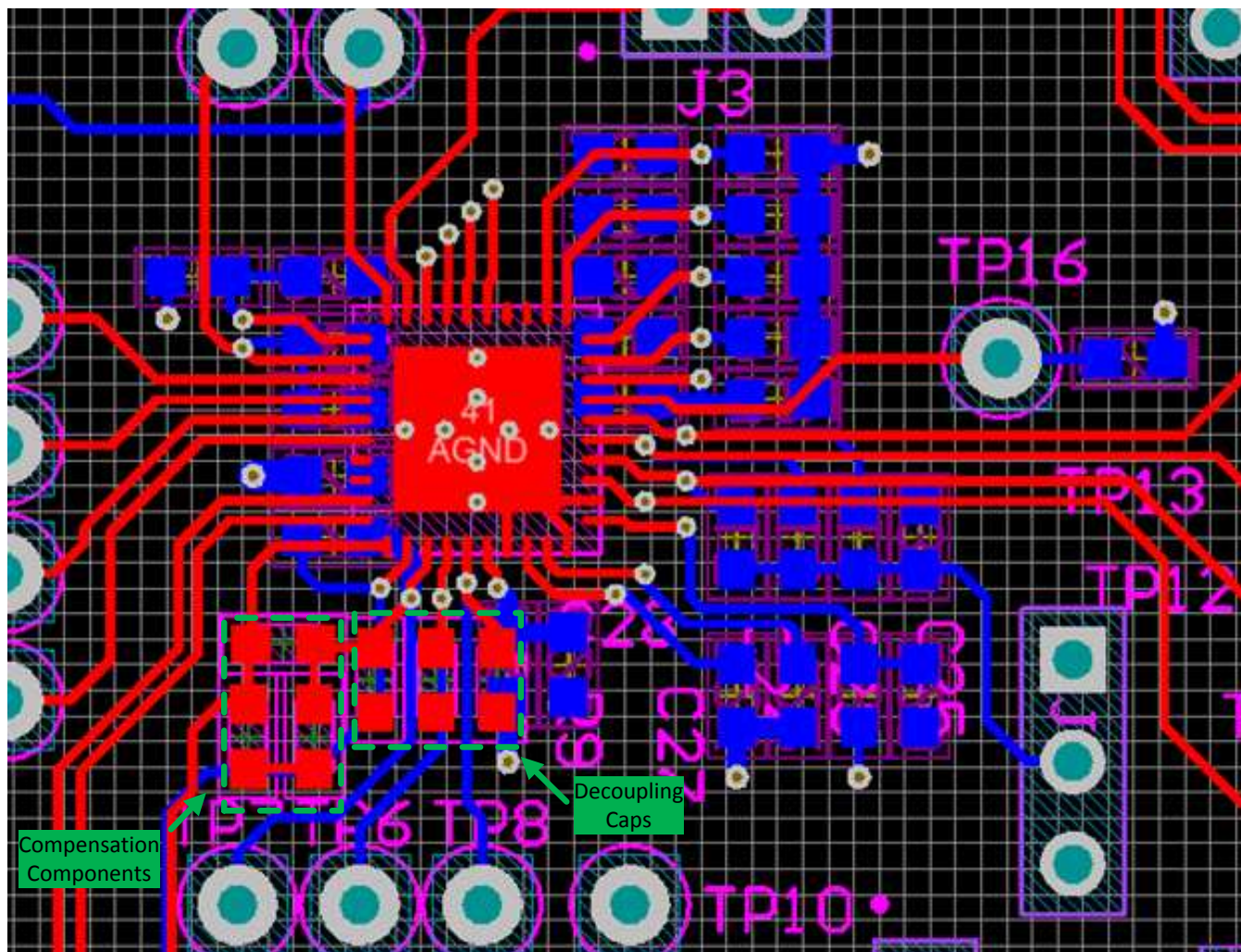


Figure 122. Layout Example of Decoupling Caps and Compensation Components

Layout Guidelines (continued)

10.1.2.7 Grounding Recommendations

The TPS53647 device has a GND pin, and a thermal pad. The normal procedure for connecting these follows:

- The thermal pad does not have an electrical connection to the TPS53647 device. However, it is suggested to be connected to GND pin of the TPS53647 device (analog ground) to give good ground shielding as shown in [Figure 123](#)
- All the analog components should connect to this analog ground island
- Use a single point connection from analog ground to the power ground.
- The return path of the decoupling capacitors (V3R3, V5, VREF, Vin) should be as short as possible.
- When a separated analog ground is used, it's recommended to have an analog ground shape in layer 3 (assuming controller is on the top layer) to interconnect all the analog ground signals.

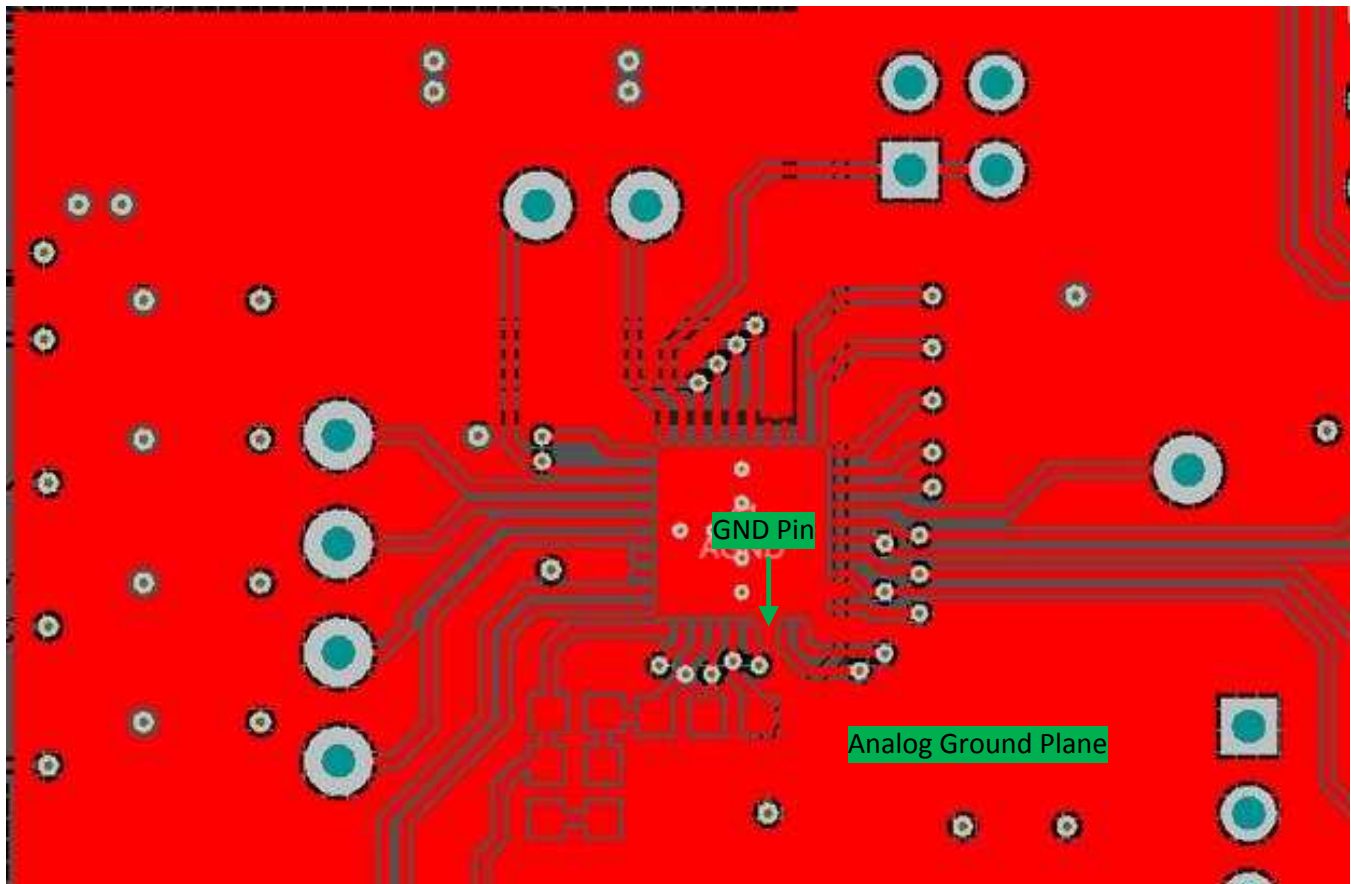


Figure 123. Layout Example for TPS53647 Grounding

Layout Guidelines (continued)

10.1.2.8 TI Smart Power Stage CSD95372BQ5MC

The following layout recommendations refer to the CSD95372BQ5MC. Download the datasheet ([SLPS417](#)) for more details.

10.1.2.8.1 Electrical Performance

The CSD95372BQ5MC has the ability to switch at voltage rates greater than 10 kV/ μ s. Special care must be taken with the PCB layout design and placement of the input capacitors, inductor and output capacitors.

- The placement of the input capacitors relative to VIN and PGND pins of CSD95372BQ5MC device should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, place ceramic input capacitors as close as possible to the VIN and PGND pins. The example in uses 1 \times 3300 pF, 0402, 50-V, X7R ceramic capacitor and 3 \times 22 μ F, 1206, 25-V ceramic capacitors (TDK part number C3216X5R1E226M160AB or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers.
- Closely connect the bootstrap capacitor (0.1- μ F, 0603, 25-V ceramic capacitor) between the BOOT and BOOT_R pins.
- The switching node of the output inductor should be placed relatively close to the Power Stage CSD95372BQ5MC VSW pins. Minimizing the VSW node length between these two components reduces the PCB conduction losses and actually reduce the switching noise level.

10.1.2.8.2 Thermal Performance

The CSD95372BQ5MC has the ability to use the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in uses vias with a 12 mil drill hole and a 26 mil capture pad.
- Tent the opposite side of the vias with solder-mask.

In the end, the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

10.1.2.8.3 Sensing Performance

The thermal sensing output TAO pin must be properly decoupled for accurate reporting. As discussed above, a 1nF 25V X7R ceramic capacitor should be placed between TAO and PGND as close to the TAO pin as practical.

The integrated current sensing technology built into the driver of the CSD95372BQ5MC produces an analog signal that is proportional to the inductor current with a proportionality constant of 5 mV/A. This signal is referenced to the voltage applied to REFIN. For optimal performance of this technology a 0.1 μ F or larger ceramic capacitor should be placed across the REFIN and PGND pins as close as possible to the device.

In addition the IOUT pin should be routed back to the TPS53647 device in a quiet inner layer. If multiple CSD95372BQ5M's are used on the same board, the IOUT traces should have at least 20 mils spacing between them. Capacitive loading of the IOUT pin should be avoided to maintain the integrity of the sensed signal.

Layout Guidelines (continued)

10.1.2.9 Power Delivery and Power Density

Power stage layout guidelines:

- Maximize the widths of power, ground and drive signal connections.
- For conductors in the power path, be sure there is adequate trace width for the amount of current flowing through the traces.
- Make sure there are sufficient vias for connections between layers. A good rule of thumb is to use 1 minimum via per ampere of current.

10.2 Layout Example

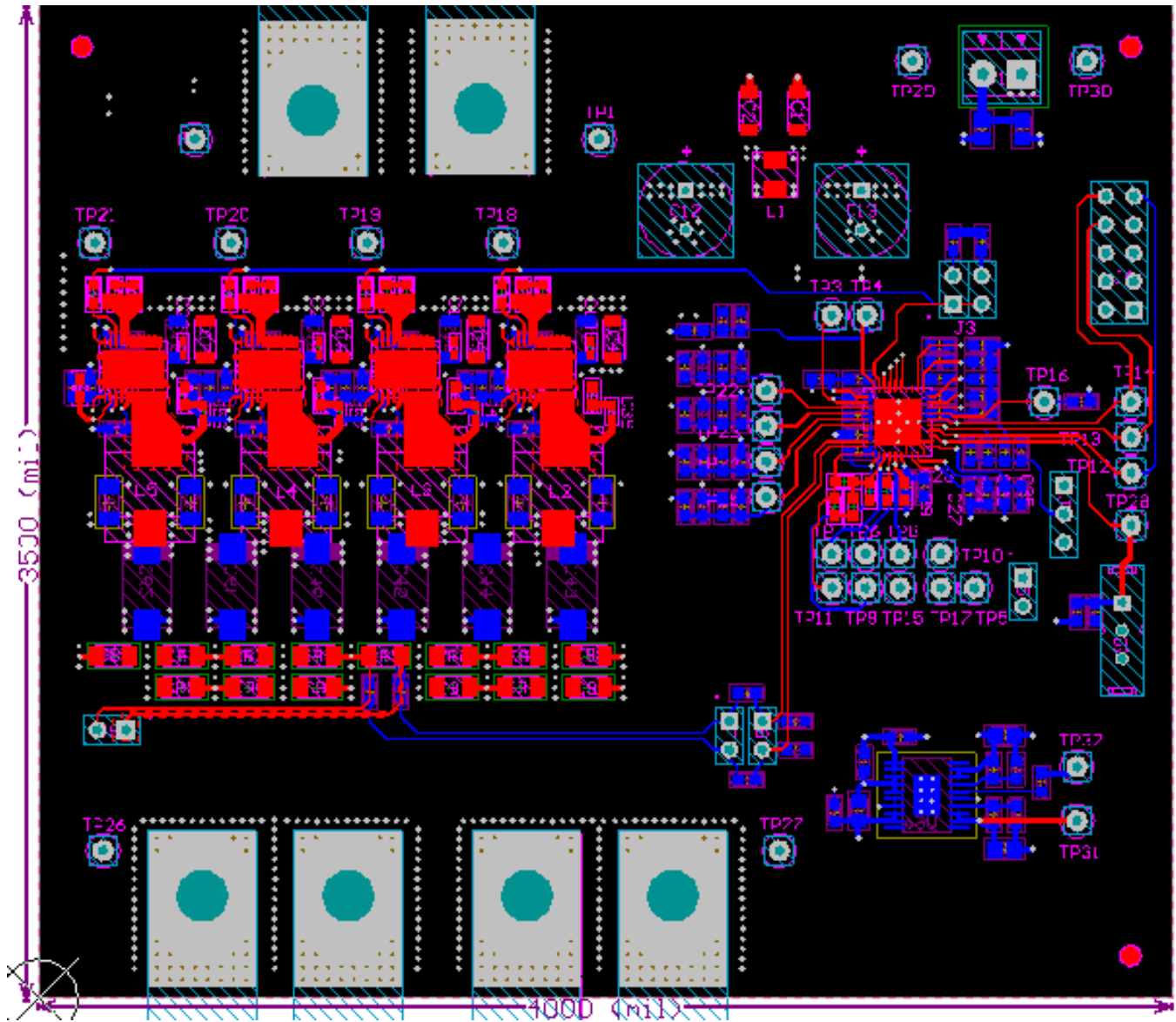


Figure 124. TPS53647 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

For the Power Stage Designer tool, go to www.ti.com/tool/powerstage-designer.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- *CSD95372BQ5MC Synchronous Buck NexFET™ Smart Power Stage (SLPS417)*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

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PMBus is a trademark of SMIF, Inc.

All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary



SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| TPS53647RTAR | ACTIVE | WQFN | RTA | 40 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TPS 53647 |  |
| TPS53647RTAT | ACTIVE | WQFN | RTA | 40 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TPS 53647 |  |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS53647RTAR | WQFN | RTA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS53647RTAT | WQFN | RTA | 40 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

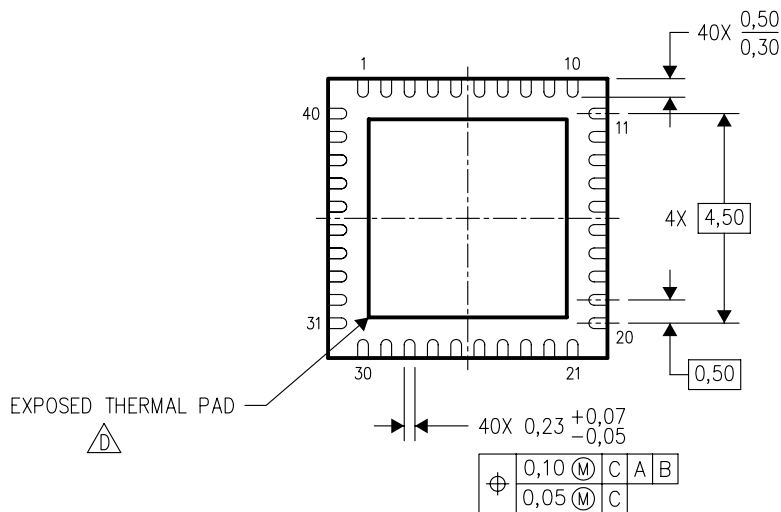
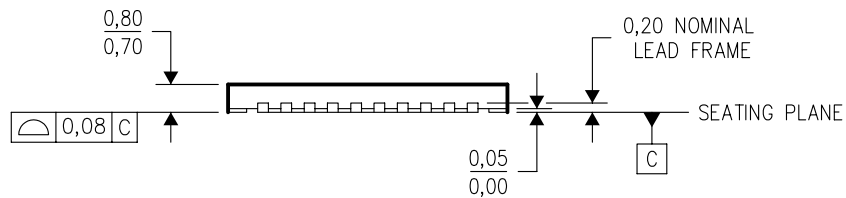
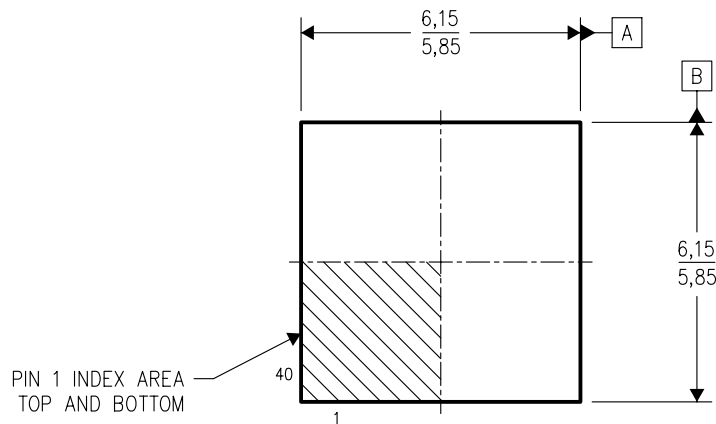


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS53647RTAR | WQFN | RTA | 40 | 2500 | 367.0 | 367.0 | 38.0 |
| TPS53647RTAT | WQFN | RTA | 40 | 250 | 210.0 | 185.0 | 35.0 |

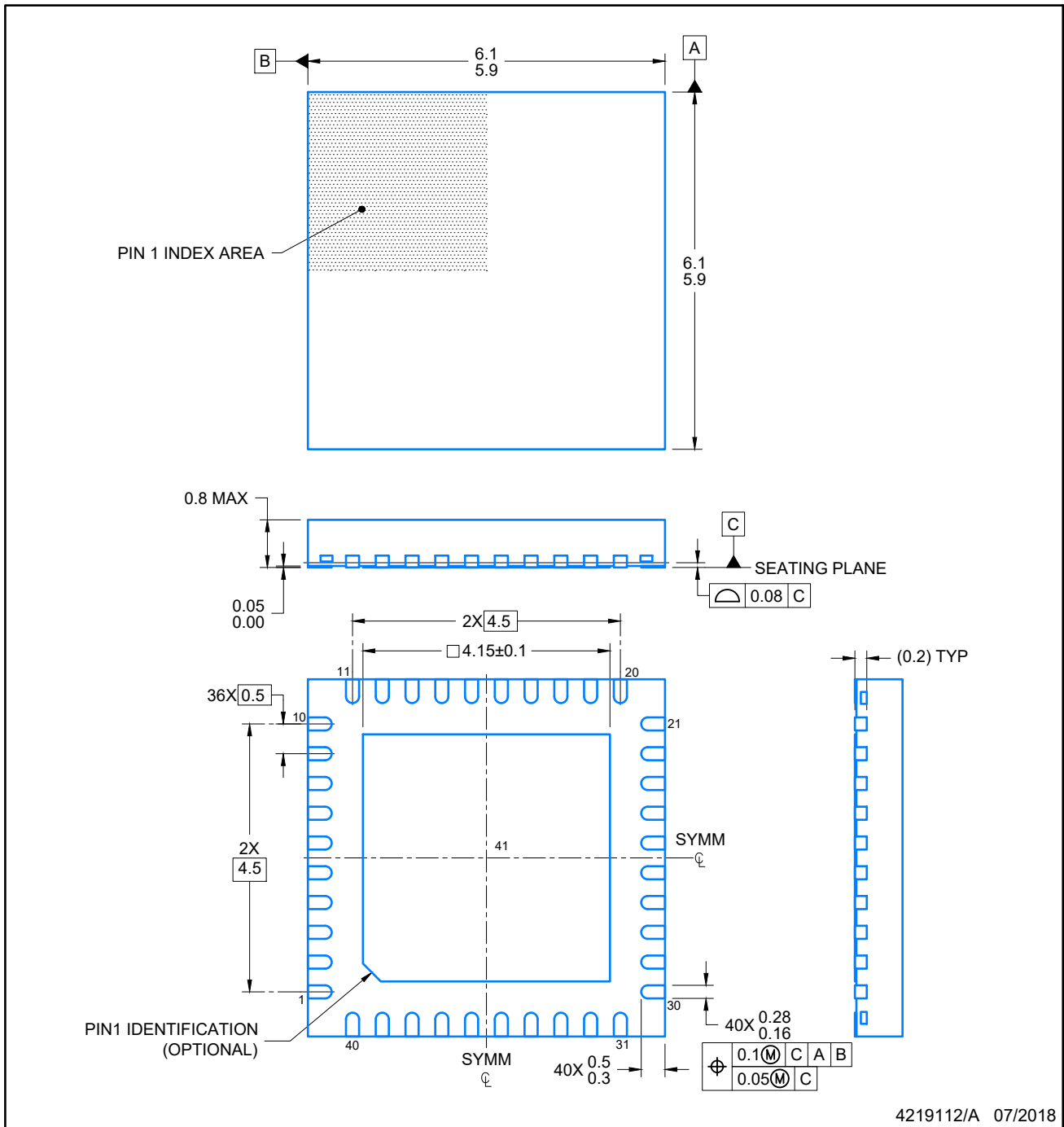
RTA (S-PQFP-N40)

PLASTIC QUAD FLATPACK



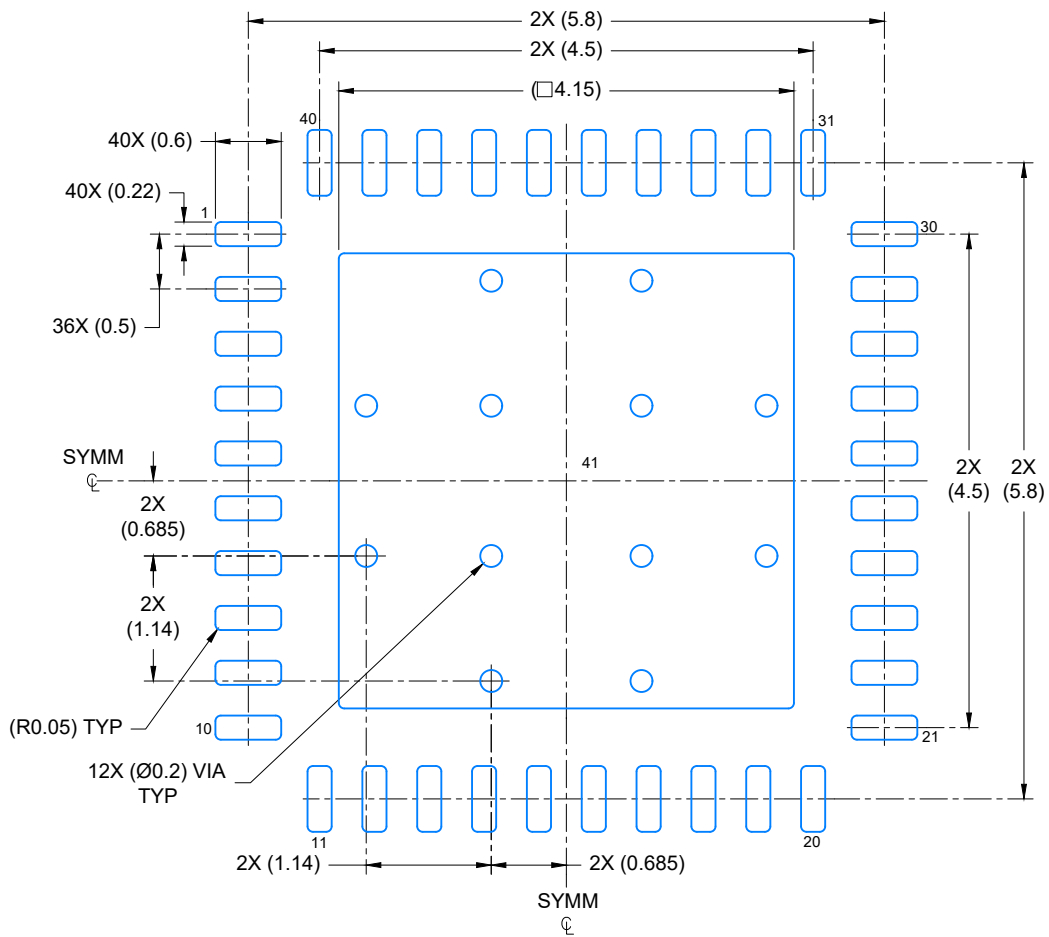
4204422/B 11/04

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.



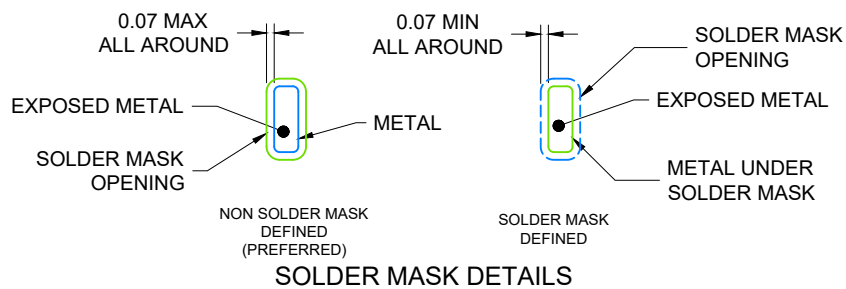
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

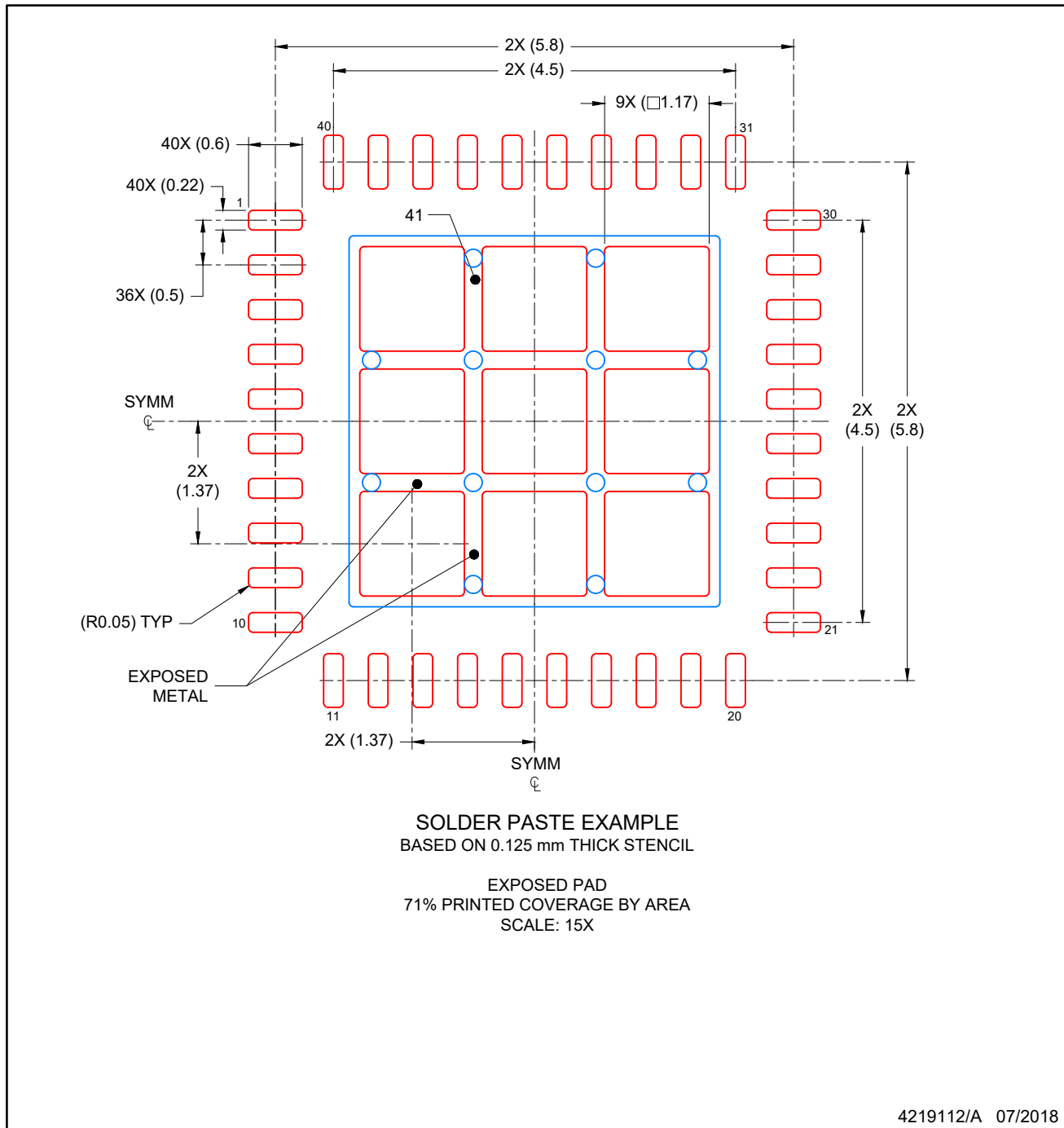
SCALE: 15X



4219112/A 07/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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