2.5-A and 5-A, 35-V_{MAX} VDD FET and IGBT Single-Gate Driver

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- Low-Cost Gate Driver (offering optimal solution for driving FET and IGBTs)
- Superior Replacement to Discrete Transistor Pair Drive (providing easy interface with controller)
- CMOS Compatible Input-Logic Threshold (becomes fixed at VDD above 18 V)
- Split Outputs Allow Separate Turnon and Turnoff Tuning
- Enable with Fixed TTL Compatible Threshold
- High 2.5-A Source and 5-A Sink Peak-Drive Currents at 18-V VDD
- Wide VDD Range From 10 V up to 35 V
- Input Pins Capable of Withstanding up to –5-V DC Below Ground
- Output Held Low When Inputs are Floating or During VDD UVLO
- Fast Propagation Delays (17-ns typical)
- Fast Rise and Fall Times (15-ns and 7-ns typical with 1800-pF Load)
- Undervoltage Lockout (UVLO)
- Used as a High-Side or Low-Side Driver (if designed with proper bias and signal isolation)
- Low-Cost Space-Saving 6-Pin DBV (SOT-23) Package
- Operating Temperature Range of –40°C to 140°C

APPLICATIONS

- Automotive
- Switch-Mode Power Supplies
- DC-to-DC Converters
- Solar Inverters, Motor Control, UPS
- HEV and EV Chargers
- Home Appliances
- Renewable Energy Power Conversion
- SiC FET Converters

DESCRIPTION

The UCC27532-Q1 device is a single-channel high-speed gate driver capable of effectively driving MOSFET and IGBT power switches by up to 2.5-A source and 5-A sink (asymmetrical drive) peak current. Strong sink capability in asymmetrical drive boosts immunity against parasitic Miller turnon effect. The UCC27532-Q1 device also features a split-output configuration where the gate-drive current is sourced through the OUTH pin and sunk through the OUTL pin. This pin arrangement allows the user to apply independent turnon and turnoff resistors to the OUTH and OUTL pins respectively and easily control the switching slew rates.

The driver has rail-to-rail drive capability and an extremely-small propagation delay of 17 ns (typically).

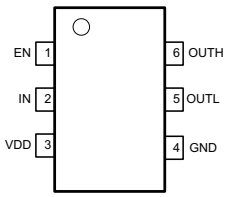
The UCC27532-Q1 device has a CMOS-input threshold-centered 55% rise and 45% fall in regards of VDD at VDD below or equal 18 V. When VDD is above 18 V, the input threshold remains fixed at the maximum level.

The driver has an EN pin with a fixed TTL-compatible threshold. EN is internally pulled up; pulling EN low disables driver, while leaving it open provides normal operation. The EN pin can be used as an additional input with the same performance as the IN pin.

Leaving the input pin of driver open holds the output low. The logic behavior of the driver is shown in the Timing Diagram, Input/Output Logic Truth Table, and Typical Application Diagrams.

Internal circuitry on the VDD pin provides an undervoltage-lockout function that holds the output low until the VDD supply voltage is within operating range.

The UCC27532-Q1 driver is offered in a 6-pin standard SOT-23 (DBV) package. The device operates over a wide temperature range of –40°C to 140°C.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage range	VDD	–0.3	35	V
Continuous	OUTH, OUTL	–0.3	VDD +0.3	
Pulse	OUTH, OUTL (200 ns)	–2	VDD +0.3	
Continuous IN, EN		–5	27	V
Pulse IN, EN (1.5 µs)		–6.5	27	
Electrostatic discharge (ESD) rating	Human body model (HBM)		2	kV
	Charged device model (CDM)		750	V
Operating virtual junction temperature range, T_J		–40	150	°C
Storage temperature range, T_{stg}		–65	150	
Lead temperature	Soldering, 10 seconds		300	
	Reflow		260	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.

THERMAL INFORMATION

THERMAL METRIC(1)		UCC27532-Q1 DBV 6 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	178.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	109.7	
θ_{JB}	Junction-to-board thermal resistance	28.3	
ψ_{JT}	Junction-to-top characterization parameter	14.7	
ψ_{JB}	Junction-to-board characterization parameter	27.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply voltage range, VDD	10	18	32	V
Operating junction temperature range	–40		140	°C
Input voltage, IN	–5		25	V
Enable, EN	–5		25	

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, VDD = 18 V, $T_A = T_J$ = –40°C to 140°C, IN switching from 0 V to VDD, 1-µF capacitor from VDD to GND, f = 100 kHz. Currents are positive into and negative out of the specified terminal. OUTH and OUTL are tied together. Typical condition specifications are at 25°C.

PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
Bias Currents						
I_{DDoff}	Startup current, VDD = 7.0	IN, EN = VDD	100	240	350	µA
		IN, EN = GND	100	250	350	
Under Voltage Lockout (UVLO)						
V_{ON}	Supply start threshold		8	8.9	9.8	V
V_{OFF}	Minimum operating voltage after supply start		7.3	8.2	9.1	
V_{DD_H}	Supply voltage hysteresis			0.7		
Input (IN)						
V_{IN_H}	Input signal high threshold	Output high	8.8	9.4	10	V
V_{IN_L}	Input signal low threshold	Output low	6.7	7.3	7.9	
V_{IN_HYS}	Input signal hysteresis			2.1		
Enable (EN)						
V_{EN_H}	Enable signal high threshold	Output high	1.7	1.9	2.1	V
V_{EN_L}	Enable signal low threshold	Output low	0.8	1	1.2	
V_{EN_HYS}	Enable signal hysteresis			0.9		
Outputs (OUTH/OUTL)						
$I_{SRC/SNK}$	Source peak current (OUTH)/ sink peak current (OUTL)(1)	C_{LOAD} = 0.22 µF, f = 1 kHz		–2.5 / +5		A
V_{OH}	OUTH, high voltage	I_{OUTH} = –10 mA	VDD –0.2	VDD –0.12	VDD –0.07	V
V_{OL}	OUTL, low voltage	I_{OUTL} = 100 mA		0.065	0.125	
R_{OH}	OUTH, pull-up resistance(2)	T_A = 25°C, I_{OUT} = -10 mA	11	12	12.5	Ω
		T_A = –40°C to 140°C, I_{OUT} = -10 mA	7	12	20	
R_{OL}	OUTL, pull-down resistance	T_A = 25°C, I_{OUT} = 100 mA	0.45	0.65	0.85	
		T_A = –40°C to 140°C, I_{OUT} = 100 mA	0.3	0.65	1.25	
Switching Time(1)(3)						
t_R	Rise time	C_{LOAD} = 1.8 nF		15		ns
t_F	Fall time	C_{LOAD} = 1.8 nF		7		
t_{D1}	Turnon propagation delay	C_{LOAD} = 1.8 nF, IN = 0 V to VDD		17	26	
t_{D2}	Turnoff propagation delay	C_{LOAD} = 1.8 nF, IN = VDD to 0 V		17	26	

(1) Ensured by design and tested during characterization. Not production tested.
(2) Output pullup resistance here is a DC measurement that measures resistance of PMOS structure only, not N-channel structure. The effective dynamic pull-up resistance is 3 × R_{OL}.
(3) See Figure 1.

Timing Diagram

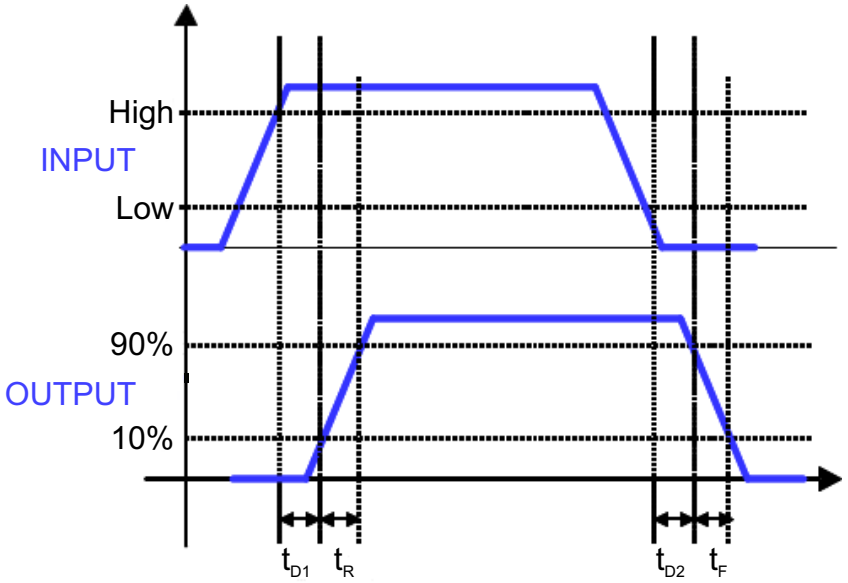
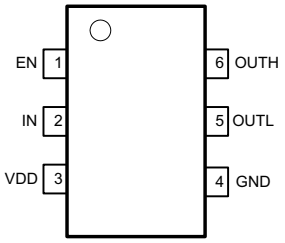


Figure 1. (OUTH tied to OUTL)
Input = IN, Output = OUT (EN = VDD)
or Input = EN, Output = OUT (IN = VDD)

DEVICE INFORMATION

SOT-23 PACKAGE
6-PIN DBV
(TOP VIEW)



TERMINAL FUNCTIONS

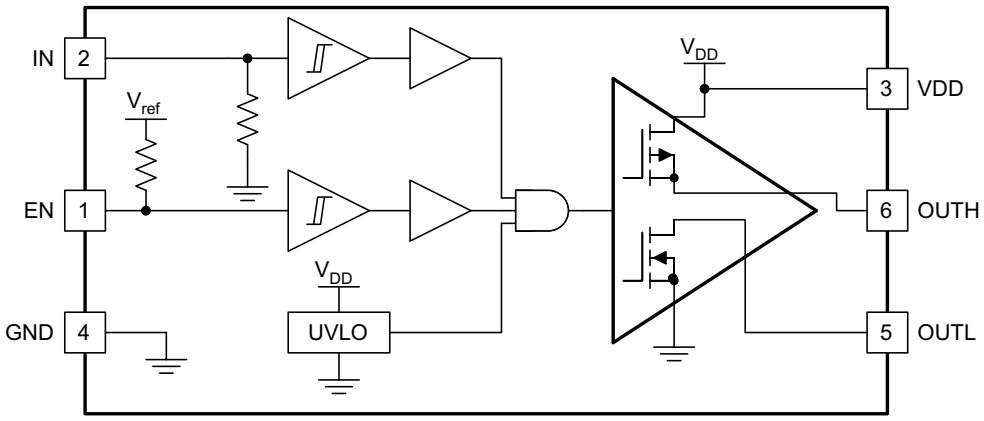
TERMINAL		I/O	FUNCTION
NAME	PIN NUMBER		
EN	1	I	Enable (Pull EN to GND in order to disable output, pull it high or leave it open to enable the output)
GND	4	–	Ground (all signals are referenced to this node)
IN	2	I	Driver non-inverting input (CMOS threshold)
OUTL	5	O	5-A sink current output of driver
OUTH	6	O	2.5-A source current output of driver
VDD	3	I	Bias supply input

INPUT/OUTPUT LOGIC TRUTH TABLE

IN PIN	EN PIN	OUTH PIN	OUTL PIN	OUT (OUTH and OUTL pins tied together)
L	L	High-impedance	L	L
L	H	High-impedance	L	L
H	L	High-impedance	L	L
H	H	H	High-impedance	H

Block Diagram

(EN Pullup Resistance to V_{ref} = 500 kΩ, V_{ref} = 5.8 V, In Pulldown Resistance to GND = 230 kΩ)



Typical Application Diagrams

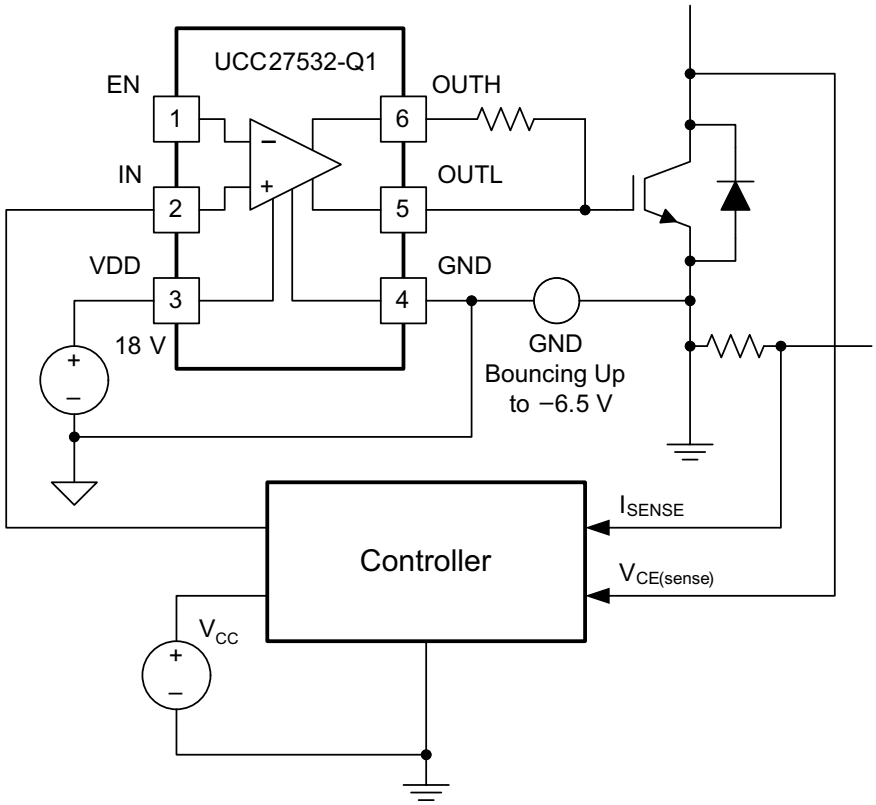


Figure 2. Driving IGBT Without Negative Bias

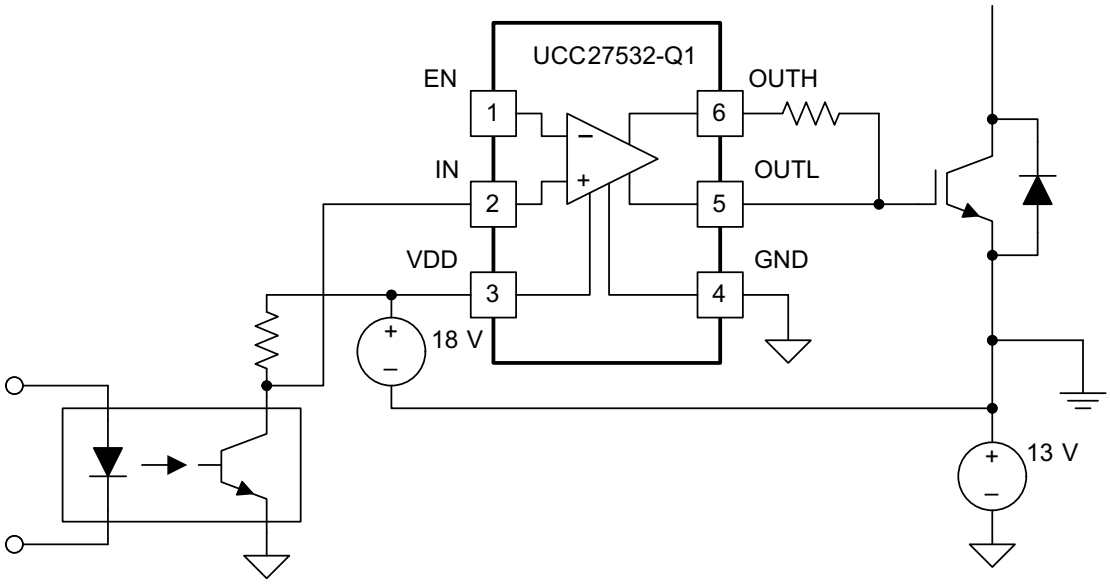


Figure 3. Driving IGBT With 13-V Negative Turnoff Bias

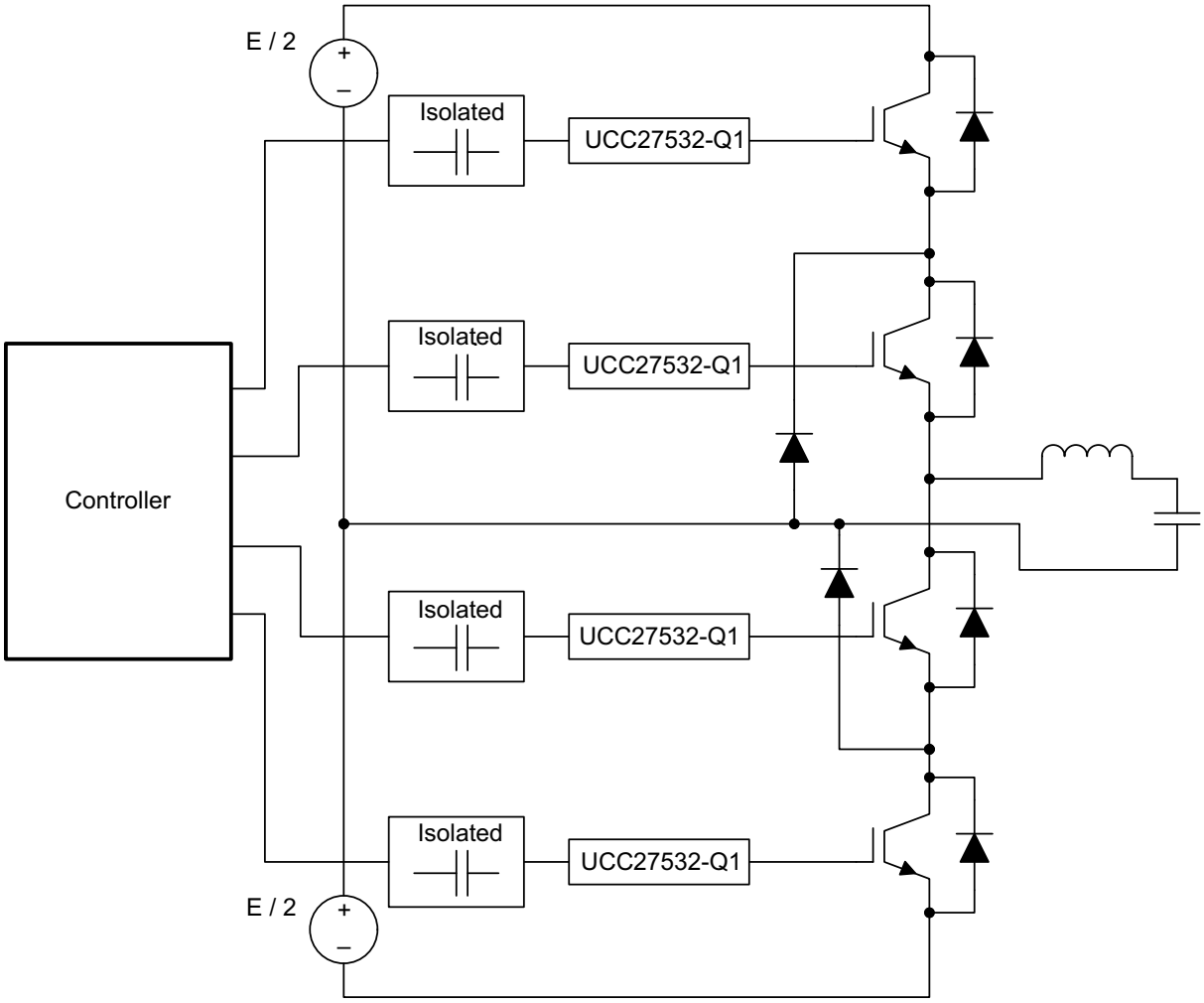


Figure 4. Using UCC27532-Q1 Drivers in an Inverter

TYPICAL CHARACTERISTICS

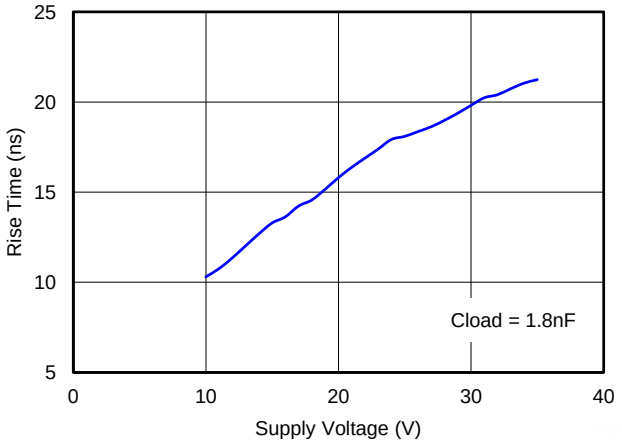


Figure 5.

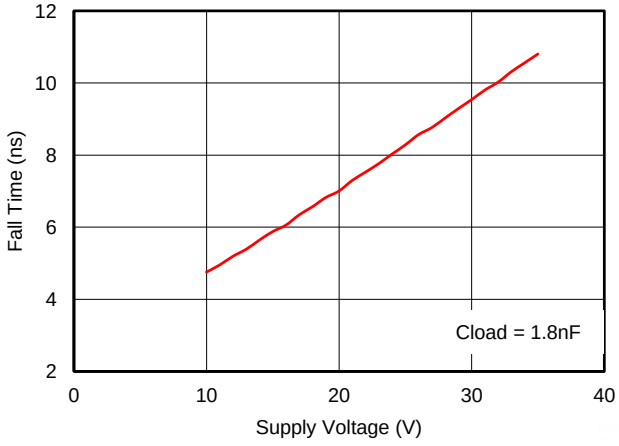


Figure 6.

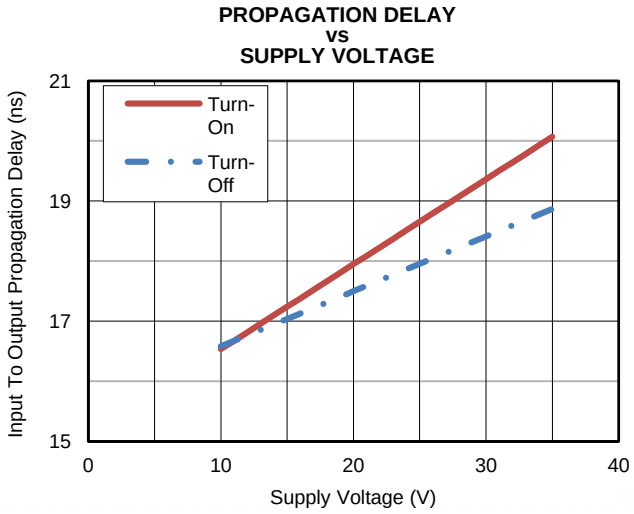


Figure 7.

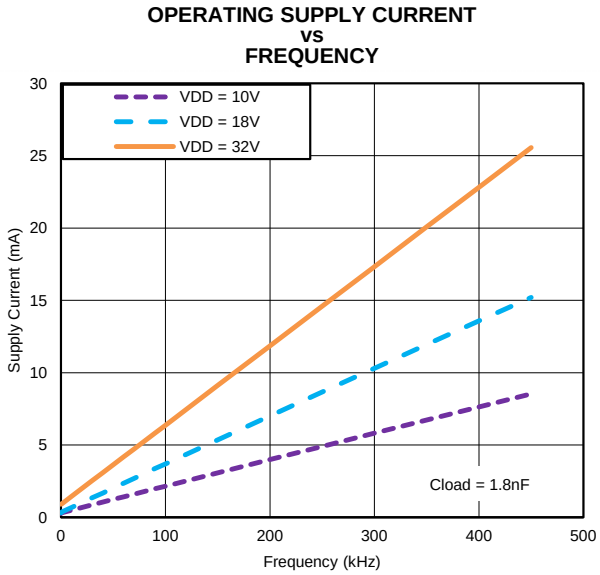


Figure 8.

TYPICAL CHARACTERISTICS (continued)

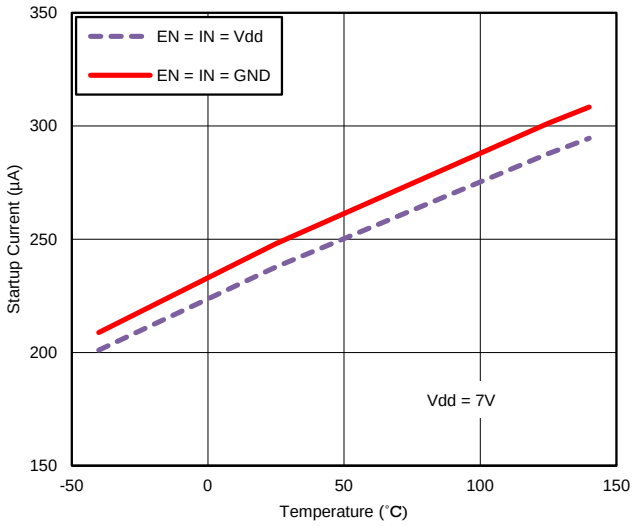


Figure 9.

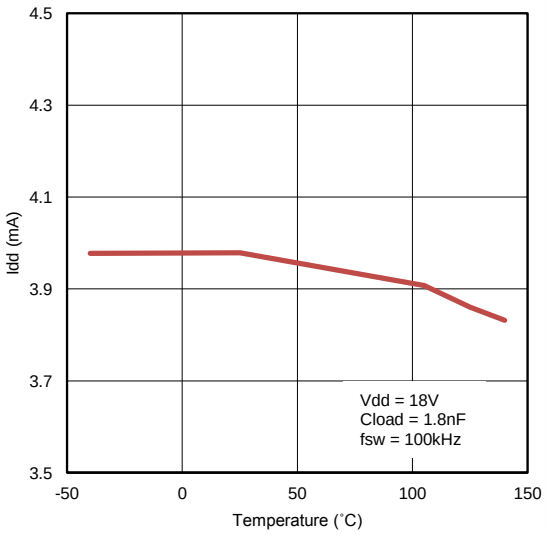


Figure 10.

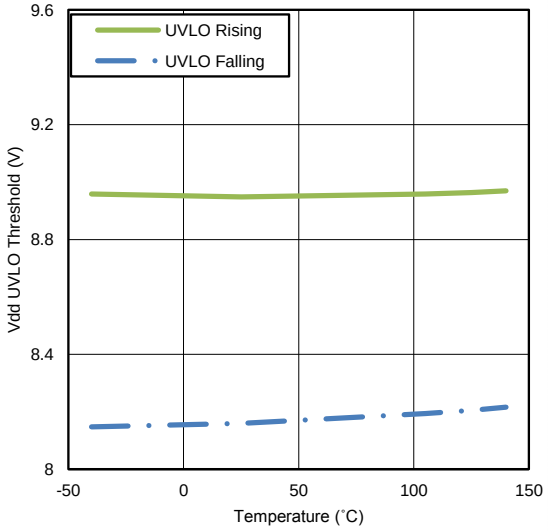


Figure 11.

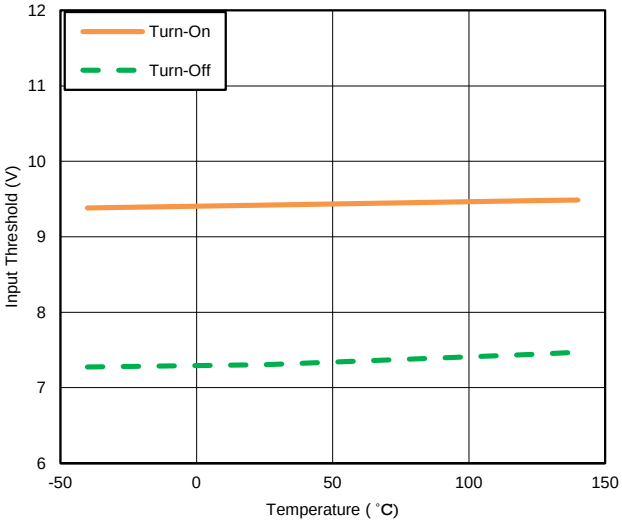


Figure 12.

TYPICAL CHARACTERISTICS (continued)

ENABLE THRESHOLD VS TEMPERATURE

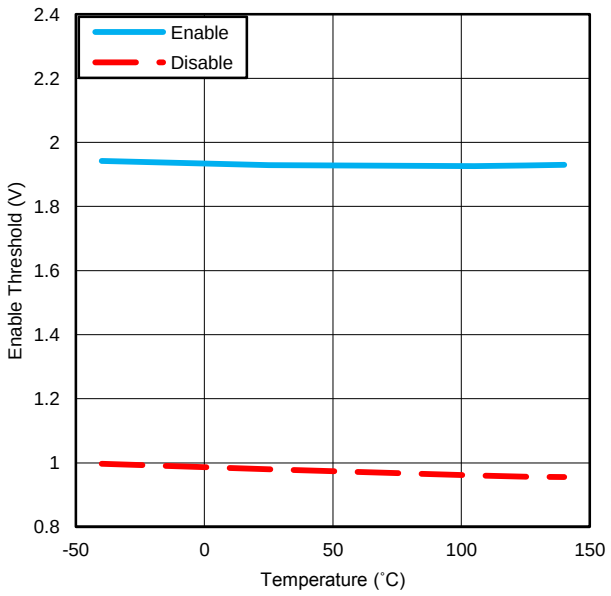


Figure 13.

OUTPUT PULLUP RESISTANCE VS TEMPERATURE

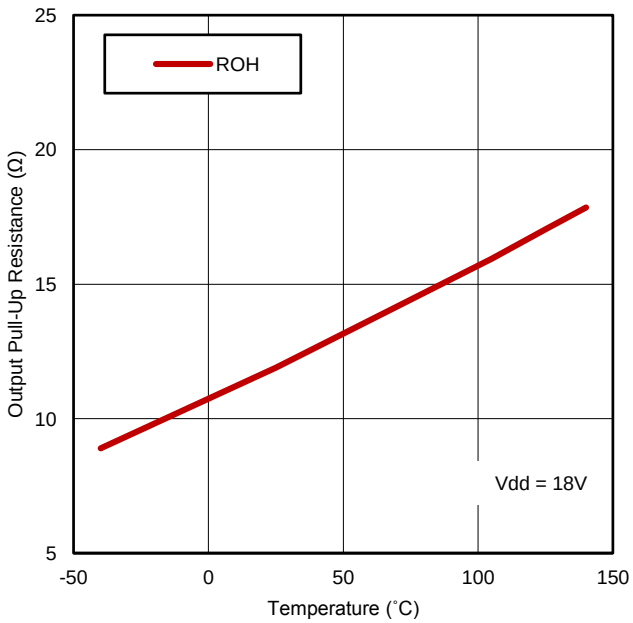


Figure 14.

OUTPUT PULLDOWN RESISTANCE VS TEMPERATURE

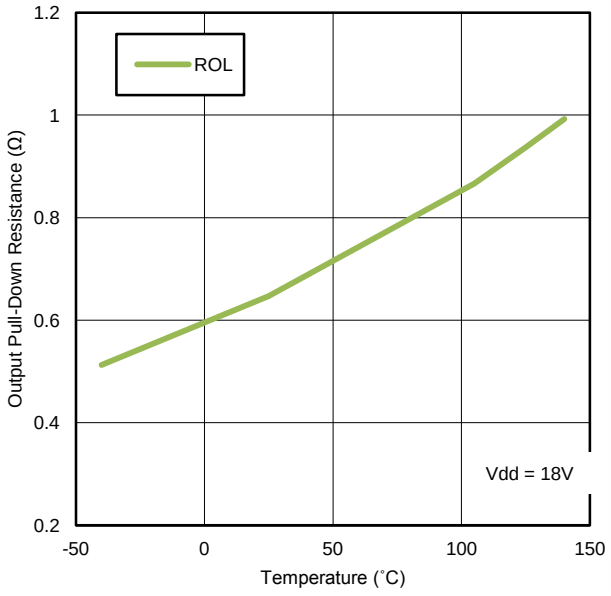


Figure 15.

OPERATING SUPPLY CURRENT VS TEMPERATURE (OUTPUT IN DC ON AND OFF CONDITION)

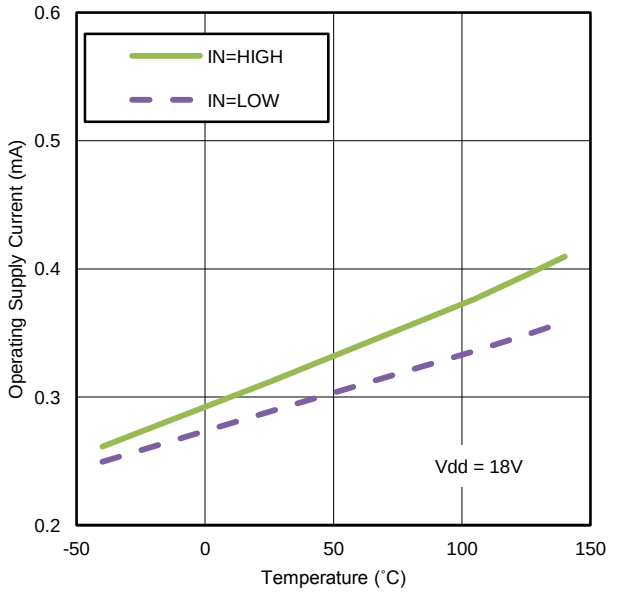


Figure 16.

TYPICAL CHARACTERISTICS (continued)

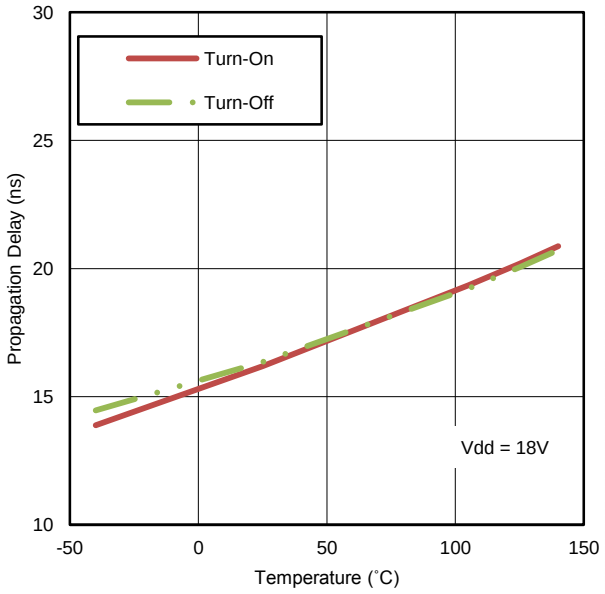


Figure 17.

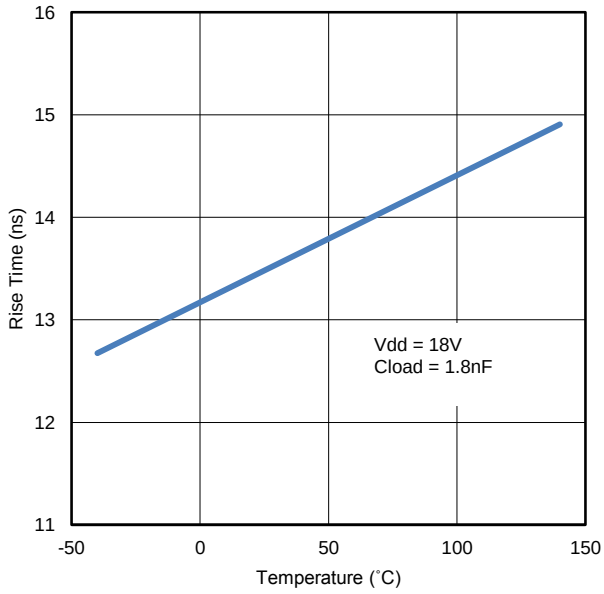


Figure 18.

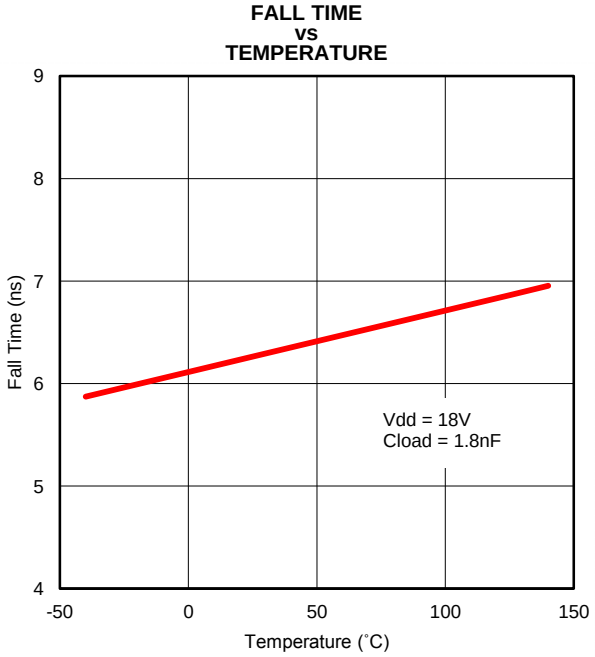


Figure 19.

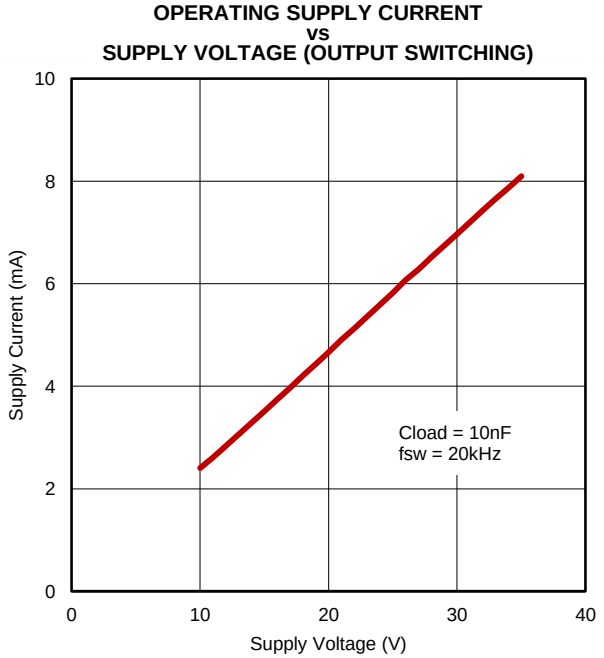


Figure 20.

TYPICAL CHARACTERISTICS (continued)

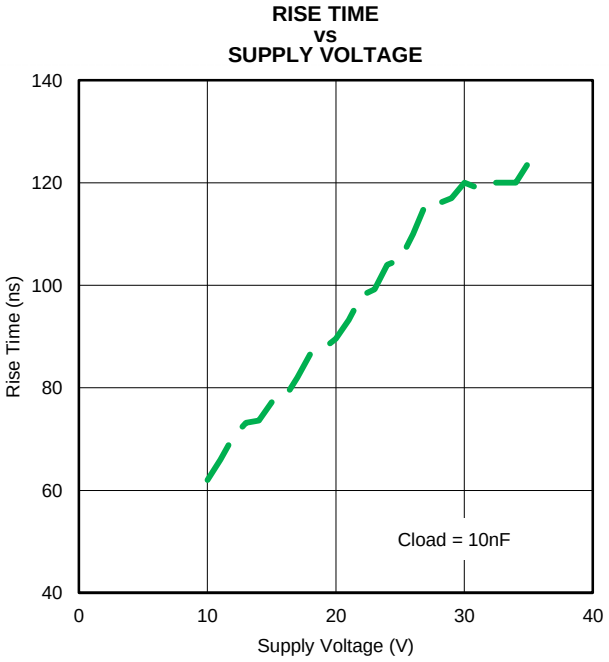


Figure 21.

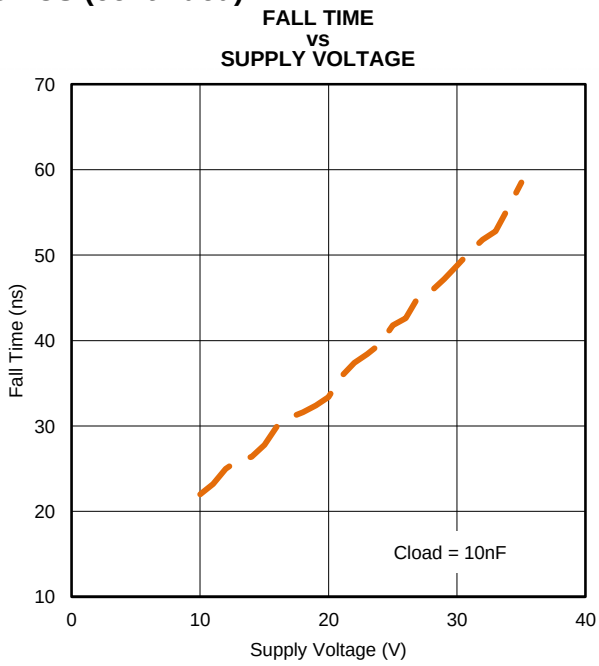


Figure 22.

APPLICATION INFORMATION

High-current gate driver devices are required in switching power applications for a variety of reasons. In order to enable fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be used between the PWM output of controllers or signal isolation devices and the gates of the power semiconductor devices. Further, gate drivers are indispensable when having the PWM controller directly drive the gates of the switching devices is not feasible. This situation is often encountered because the PWM signal from a digital controller or signal isolation device is often a 3.3-V or 5-V logic signal which is not capable of effectively turning on a power switch. A level shifting circuitry is required to boost the logic-level signal to the gate-drive voltage in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN and PNP bipolar (or P-channel and N-channel MOSFET) transistors in totem-pole arrangement, being emitter-follower configurations, prove inadequate for this function because these circuits lack level-shifting capability and low-drive voltage protection. Gate drivers effectively combine both the level-shifting, buffer drive, and UVLO functions. Gate drivers have other uses such as minimizing the effect of switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers, controlling floating power device gates, and reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself.

The UCC27532-Q1 device is very flexible in this role with a strong current-drive capability and wide supply-voltage range up to 35 V. These features allow the driver to be used in 12-V Si MOSFET applications, 20-V and –5-V (relative to source) SiC FET applications, 15-V and –15-V (relative to emitter) IGBT applications, and many others. As a single-channel driver, the UCC27532-Q1 device can be used as a low-side or high-side driver. To use the device as a low-side driver, the switch ground is typically the system ground so it can be connected directly to the gate driver. To use as a high-side driver with a floating return node, however, signal isolation is required from the controller as well as an isolated bias to the UCC27532-Q1 device. Alternatively, in a high-side drive configuration the UCC27532-Q1 device can be tied directly to the controller signal and biased with a non-isolated supply. However, in this configuration the outputs of the UCC27532-Q1 device must drive a pulse transformer which then drives the power-switch to work properly with the floating source and emitter of the power switch. Further, having the ability to control turnon and turnoff speeds independently with both the OUTH and OUTL pins ensures optimum efficiency while maintaining system reliability. These requirements coupled with the need for low propagation delays and availability in compact, low-inductance packages with good thermal capability makes gate driver devices such as the UCC27532-Q1 device extremely important components in switching power combining benefits of high-performance, low cost, component count and board-space reduction, and simplified system design.

Table 1. UCC27532-Q1 Features and Benefits

FEATURE	BENEFIT
High source and sink current capability, 2.5 A and 5 A (asymmetrical).	High current capability offers flexibility in employing UCC27532-Q1 device device to drive a variety of power switching devices at varying speeds.
Low 17 ns (typ) propagation delay.	Extremely low pulse transmission distortion.
Wide VDD operating range of 10 V to 32 V.	Flexibility in system design.
	Can be used in split-rail systems such as driving IGBTs with both positive and negative (relative to Emitter) supplies.
	Optimal for many SiC FETs.
VDD UVLO protection.	Outputs are held Low in UVLO condition, which ensures predictable, glitch-free operation at power-up and power-down.
	High UVLO of 8.9 V typical ensures that power switch is not on in high-impedance state which could result in high power dissipation or even failures.
Outputs held low when input pin (IN) in floating condition.	Safety feature, especially useful in passing abnormal condition tests during safety certification
Split output structure (OUTH, OUTL).	Allows independent optimization of turnon and turnoff speeds using series gate resistors.
Strong sink current (5 A) and low pulldown impedance (0.65 Ω).	High immunity to high dV/dt Miller turnon events.
CMOS compatible input threshold logic with wide 2.1-V hysteresis.	Excellent noise immunity.
Input capable of withstanding –6.5 V.	Enhanced signal reliability in noisy environments that experience ground bounce on the gate driver.

VDD Under Voltage Lockout

The UCC27532-Q1 device has an internal undervoltage-lockout (UVLO) protection feature on the VDD-pin supply-circuit blocks. To ensure acceptable power dissipation in the power switch, this UVLO prevents the operation of the gate driver at low supply voltages. Whenever the driver is in UVLO condition (when the VDD voltage less than V_{ON} during power-up and when the VDD voltage is less than V_{OFF} during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 8.9 V with a 700-mV typical hysteresis. This hysteresis helps prevent chatter when low-VDD supply voltages have noise from the power supply. This hysteresis also prevents chatter when there are droops in the VDD bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at voltage levels such as 10 V to 32 V provides flexibility to drive Si MOSFETs, IGBTs, and emerging SiC FETs.

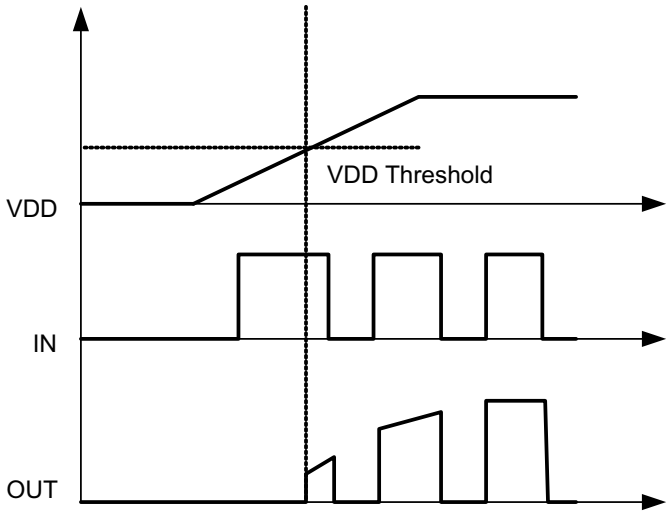


Figure 23. Power Up

Input Stage

The input pin of UCC27532-Q1 device is based on a standard CMOS-compatible input-threshold logic that is dependent on the VDD supply voltage. The input threshold is approximately 55% of VDD for rise and 45% of VDD for fall. With 18-V VDD, the typical high threshold is 9.4 V and the typical low threshold is 7.3 V. The 2.1-V hysteresis offers excellent noise immunity compared to traditional TTL logic implementations where the hysteresis is typically less than 0.5 V. For proper operation using CMOS input, the input signal level must be at a voltage equal to VDD. Using an input signal slightly larger than the threshold but less than VDD for the CMOS input can result in slower propagation delay from input to output (for example). This device also features tight control of the input-pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The very low input capacitance, typically 20 pF, on these pins reduces loading and increases switching speed.

The device features an important safety function where the output is held in the low state whenever the input pin is in a floating condition. This function is achieved using GND pulldown resistors on the non-inverting input pin (IN pin), as shown in the Block Diagram.

The input stage of the driver is best driven by a signal with a short rise or fall time. Caution must be exercised whenever the driver is used with slowly varying input signals, especially in situations where the device is located in a separate daughter board or PCB layout has long input-connection traces:

- High dI/dt current from the driver output coupled with board layout parasitics can cause ground bounce. Because the device features just one GND pin which can be referenced to the power ground, this can interfere with the differential voltage between input pins and GND and can trigger an unintended change of output state. Because of the fast 17-ns propagation delay, this can ultimately result in high-frequency oscillations, which increases power dissipation and poses a risk of damage
- 2.1-V input threshold hysteresis boosts noise immunity compared to most other industry standard drivers.

If limiting the rise or fall times to the power device in order to reduce EMI is necessary, then an external resistance is highly recommended between the output of the driver and the power device instead of adding delays on the input signal. This external resistor has the additional benefit of reducing part of the gate-charge-related power dissipation in the gate-driver device package and transferring the dissipation into the external resistor itself.

Enable Function

The enable (EN) pin of the UCC27532-Q1 device has an internal pullup resistor to an internal reference voltage. Therefore, leaving the EN pin floating turns on the driver and allows it to send output signals properly. If desired, the EN pin can also be driven by low-voltage logic to enable and disable the driver.

Output Stage

Figure 24 shows the output stage of the UCC27532-Q1 device. The UCC27532-Q1 device features a unique architecture on the output stage which delivers the highest peak-source current when it is most needed during the Miller plateau region of the power switch turnon transition (when the power switch drain or collector voltage experiences dV/dt). The device output stage features a hybrid pullup structure using a parallel arrangement of N-Channel and P-Channel MOSFET devices. By turning on the N-Channel MOSFET during a narrow instant when the output changes state from low to high, the gate driver device is able to deliver a brief boost in the peak sourcing current enabling fast turn on.

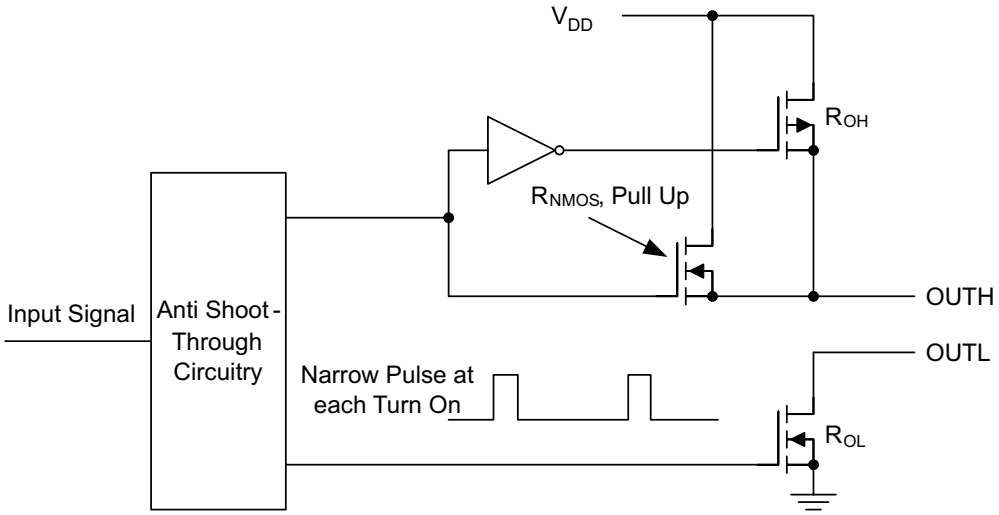


Figure 24. UCC27532-Q1 Gate-Driver Output Stage

The R_{OH} parameter (see ELECTRICAL CHARACTERISTICS) is a DC measurement and is representative of the on-resistance of the P-Channel device only because the N-Channel device is turned-on only during output change of state from low to high. Thus the effective resistance of the hybrid pullup stage is much lower than what is represented by R_{OH} parameter. The pulldown structure is composed of a N-Channel MOSFET only. The R_{OL} parameter (see ELECTRICAL CHARACTERISTICS), which is also a DC measurement, is representative of true impedance of the pulldown stage in the device. In UCC27532-Q1 device, the effective resistance of the hybrid pullup structure is approximately 3 × R_{OL}.

The UCC27532-Q1 device is capable of delivering 2.5-A source, 5-A Sink (asymmetrical drive) at VDD = 18 V. Strong sink capability in asymmetrical drive results in a very low pulldown impedance in the driver output stage which boosts immunity against the parasitic Miller turnon (high slew-rate dV/dt turn on) effect that is seen in both IGBT and FET power switches.

An example of a situation where Miller turnon is a concern is synchronous rectification (SR). In SR application, the dV/dt occurs on MOSFET drain when the MOSFET is already held in the off state by the gate driver. The current charging the C_{GD} Miller capacitance during this high dV/dt is shunted by the pulldown stage of the driver. If the pulldown impedance is not low enough then a voltage spike can result in the V_{GS} of the MOSFET, which can result in spurious turnon. This phenomenon is illustrated in Figure 25.

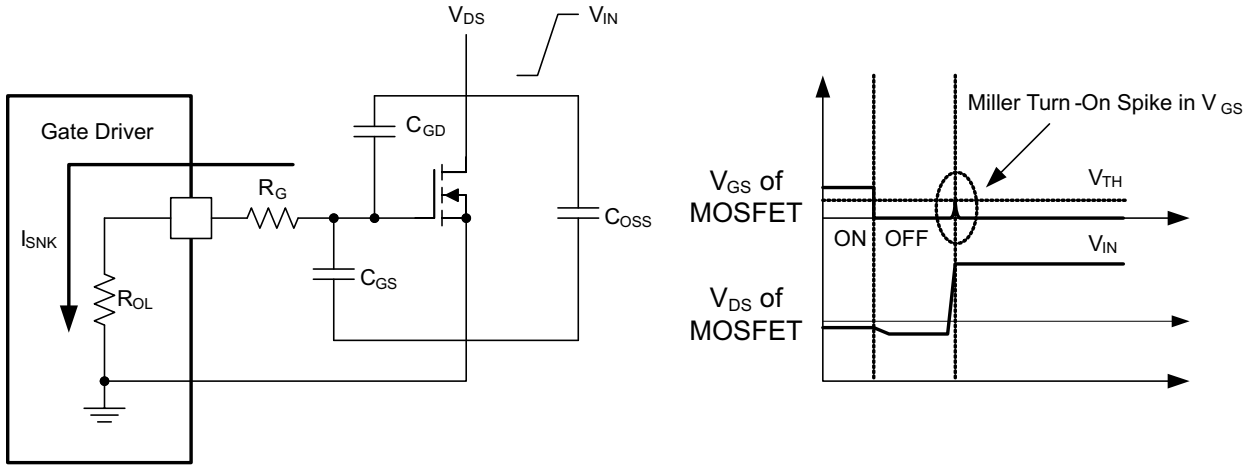


Figure 25. Low Pulldown Impedance in the UCC27532-Q1 Device (Output Stage Mitigates Miller Turnon Effect)

The driver output voltage swings between VDD and GND providing rail-to-rail operation because of the MOS output stage which delivers very low dropout. The presence of the MOSFET body diodes also offers low impedance to switching overshoots and undershoots which means that in many cases, external Schottky diode clamps can be eliminated.

Power Dissipation

Power dissipation of the gate driver has two portions as shown in Equation 1.

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

The DC portion of the power dissipation is shown in Equation 2.

$$P_{DC} = IQ \times V_{DD}$$

where

- I_Q is the quiescent current for the driver (2)

The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and others, as well as any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances and parasitic shoot-through). The UCC27532-Q1 device features very-low quiescent currents (less than 1 mA) and contains internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the P_{DC} on the total power dissipation within the gate driver can be assumed as insignificant. In practice, this is the power consumed by the driver when the output is disconnected from the gate of power switch.

The power dissipated in the gate driver package during switching (P_{SW}) is based on the following factors:

- Gate charge required of the power device (typically a function of the drive voltage V_G, which is very close to input bias supply voltage VDD due to low V_{OH} drop-out)
- Switching frequency
- Use of external gate resistors

When a driver device is tested with a discrete, capacitive load, calculating the power that is required from the bias supply is simple. Equation 3 calculates the energy that must be transferred from the bias supply to charge the capacitor.

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2$$

where

- C_{LOAD} is load capacitor
- V_{DD} is bias voltage feeding the driver

(3)

When the capacitor is discharged an equal amount of energy is dissipated. During turnoff the energy stored in capacitor is fully dissipated in drive circuit which leads to a total power loss during switching cycle given by Equation 4.

$$P_G = C_{LOAD} V_{DD}^2 f_{SW}$$

where

- f_{SW} is the switching frequency

(4)

The switching load presented by a power FET and IGBT can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge required to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, the power that must be dissipated when charging a capacitor is determined by using the equivalence, $Q_g = C_{LOAD} V_{DD}$, which results in Equation 5 for power:

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} = Q_g V_{DD} f_{SW} \quad (5)$$

This power, P_G, is dissipated in the resistive elements of the circuit when the MOSFET and IGBT is turning on or turning off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET and IGBT, this power is completely dissipated inside the driver package. With the use of external gate drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power is dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated in Equation 6.

$$P_{SW} = 0.5 \times Q_g \times V_{DD} \times f_{SW} \left(\frac{R_{OFF}}{(R_{OFF} + R_{GATE})} + \frac{R_{ON}}{(R_{ON} + R_{GATE})} \right)$$

where

- $R_{OFF} = R_{OL}$
- R_{ON} (effective resistance of pull-up structure) = $3 \times R_{OL}$

(6)

Thermal Information

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the package. In order for a gate driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package is summarized in the THERMAL INFORMATION table. For detailed information regarding the thermal information table, please see SPRA953.

PCB Layout

Proper PCB layout is extremely important in a high-current fast-switching circuit in order to provide appropriate device operation and design robustness. The UCC27532-Q1 gate driver incorporates short propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power switch to facilitate voltage transitions very quickly. At higher VDD voltages, the peak current capability is even higher (2.5-A and 5-A peak current is at VDD = 18 V). Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to the power device in order to minimize the length of high-current traces between the driver output pins and the gate of the power-switch device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high peak current being drawn from VDD during turnon of power switch. The use of low-inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turnon and turnoff current-loop paths (driver device, power switch, and VDD bypass capacitor) must be minimized as much as possible in order to keep the stray inductance to a minimum. High di/dt is established in these loops at two instances — during turnon and turnoff transients — which induces significant voltage transients on the output pins of the driver device and gate of the power switch.
- Wherever possible, parallel the source and return traces of a current loop which takes advantage of flux cancellation
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver must be connected to the other circuit nodes such as source of power switch, ground of PWM controller, and others at one, single point. The connected paths must be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT can corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.

REVISION HISTORY

Changes from Original (December 2013) to Revision A	Page
• Changed document status from *Product Preview* to *Production Data*	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27532QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 140	EAIQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UCC27532-Q1 :

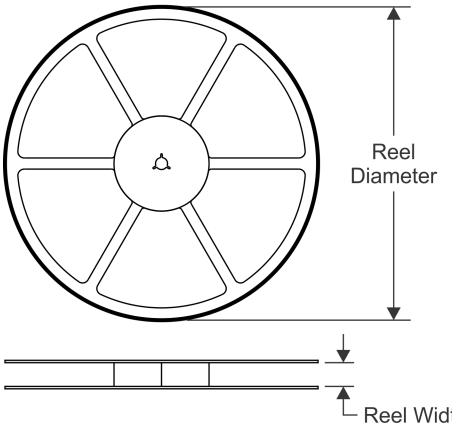
- Catalog: UCC27532

NOTE: Qualified Version Definitions:

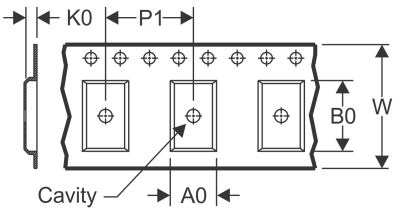
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

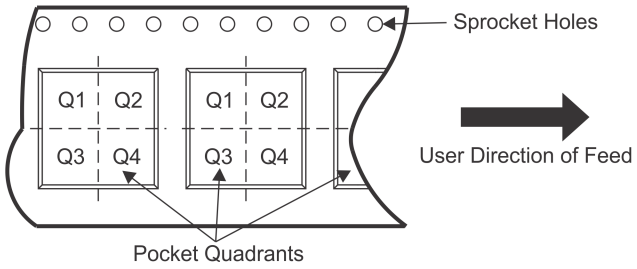


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

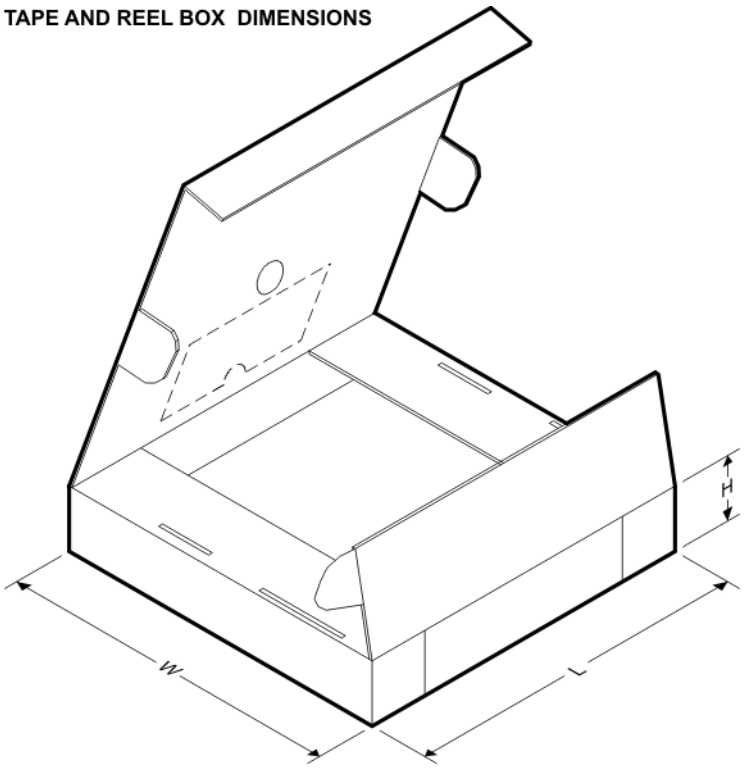
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27532QDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

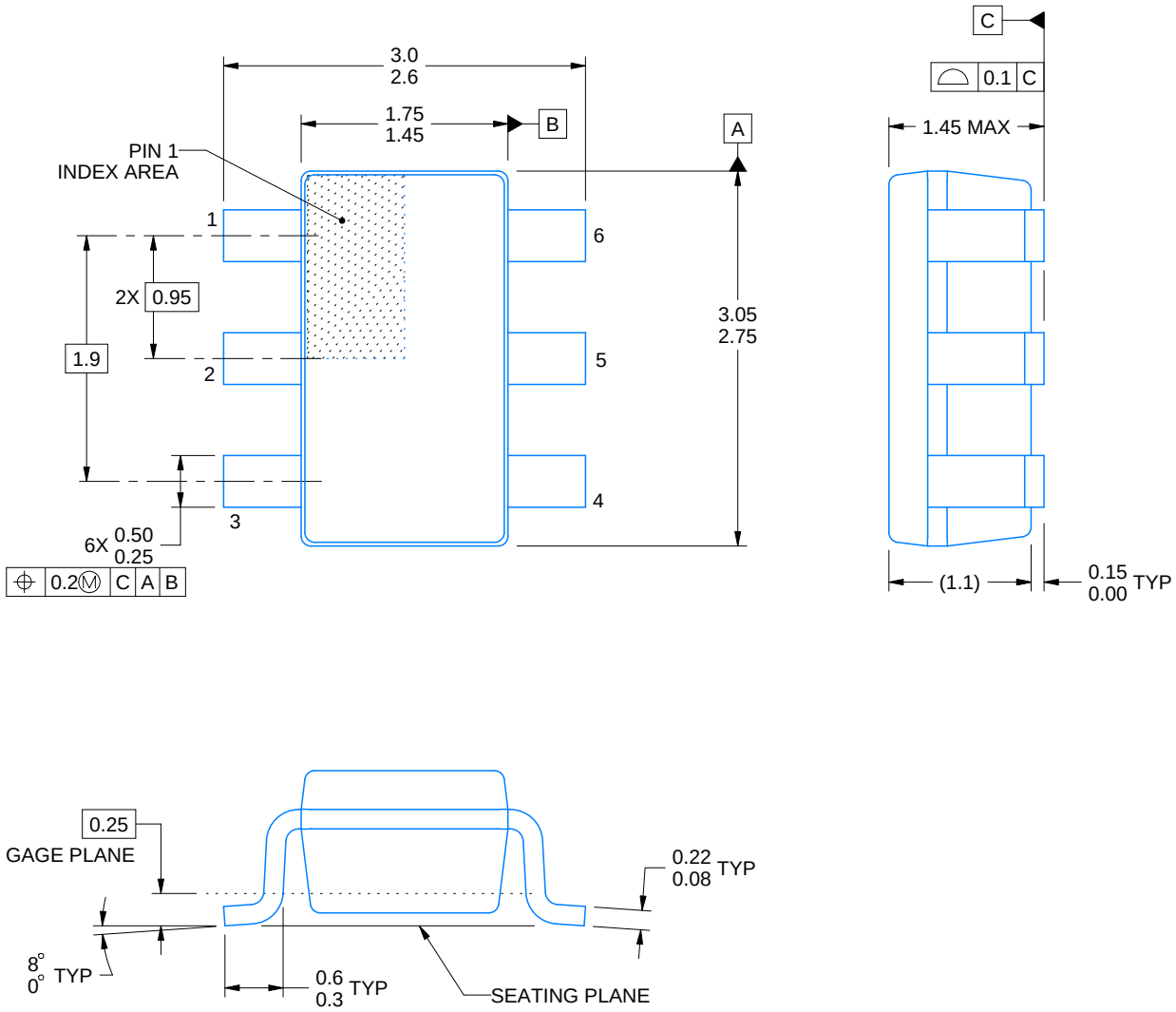
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27532QDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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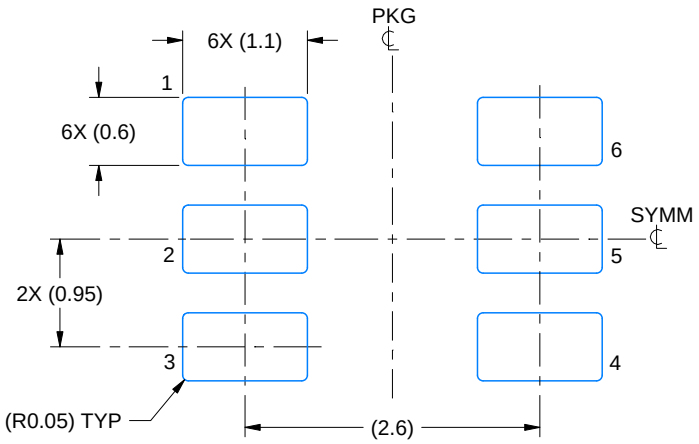
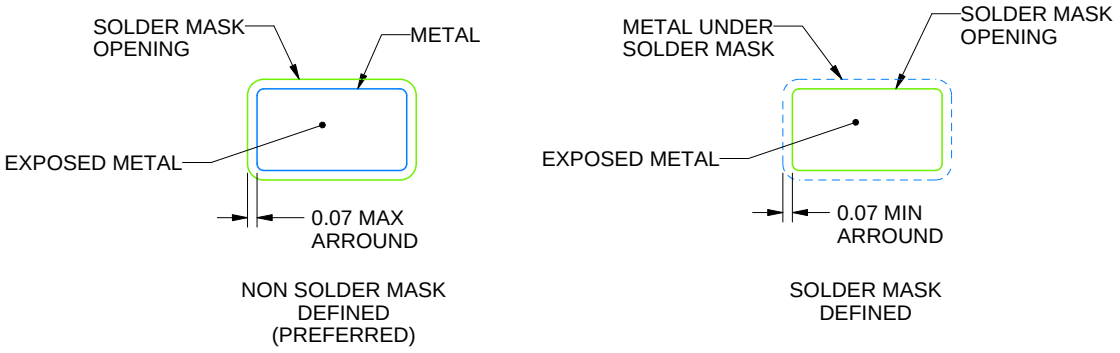
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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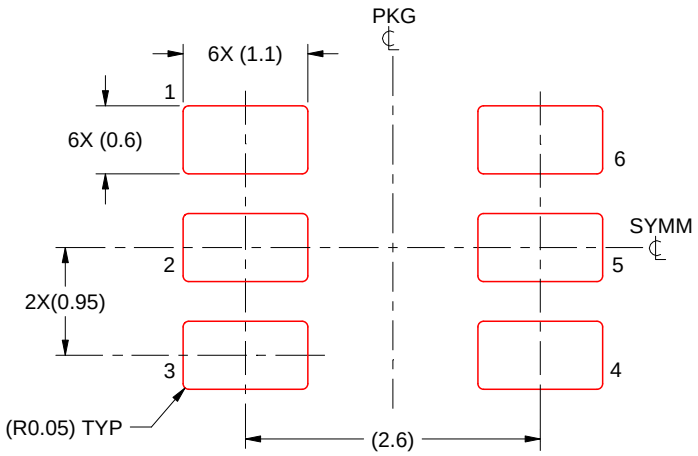
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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