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FAN73711

High-Current, High-Side Gate Drive IC

Features

- Floating Channel for Bootstrap Operation to +600 V
- 4 A / 4 A Sourcing/Sinking Current Driving Capability
- Common-Mode dv/dt Noise Canceling Circuit
- 3.3 V and 5 V Input Logic Compatible
- Output In-phase with Input Signal
- Under-Voltage Lockout for V_{BS}
- Built-In Shunt Regulator on V_{DD} and V_{BS}
- 8-Lead, Small Outline Package (SOP)

Applications

- High-Speed Gate Driver
- Sustain Switch Driver in PDP Application
- Energy Recovery Circuit Switch Driver in PDP Application
- High-Power Buck Converter
- Motor Drive Inverter

Description

The FAN73711 is a monolithic high-side gate-drive IC that can drive high-speed MOSFETs and IGBTs operating up to +600 V. It has a buffered output stage with all NMOS transistors designed for high pulse-current driving capability and minimum cross-conduction.

Fairchild's high-voltage process and common-mode noise canceling techniques provide stable operation of the high-side driver under high dv/dt noise circumstances. An advanced level-shift circuit offers high-side gate driver operation up to $V_S = -9.8$ V (typical) for $V_{BS} = 15$ V. The UVLO circuit prevents malfunction when V_{BS} is lower than the specified threshold voltage.

The high-current and low-output voltage-drop feature makes this device suitable as a sustain and energy-recovery circuit switch driver in plasma display panel, motor drive inverter, switching power supply, and high-power DC-DC converter applications.

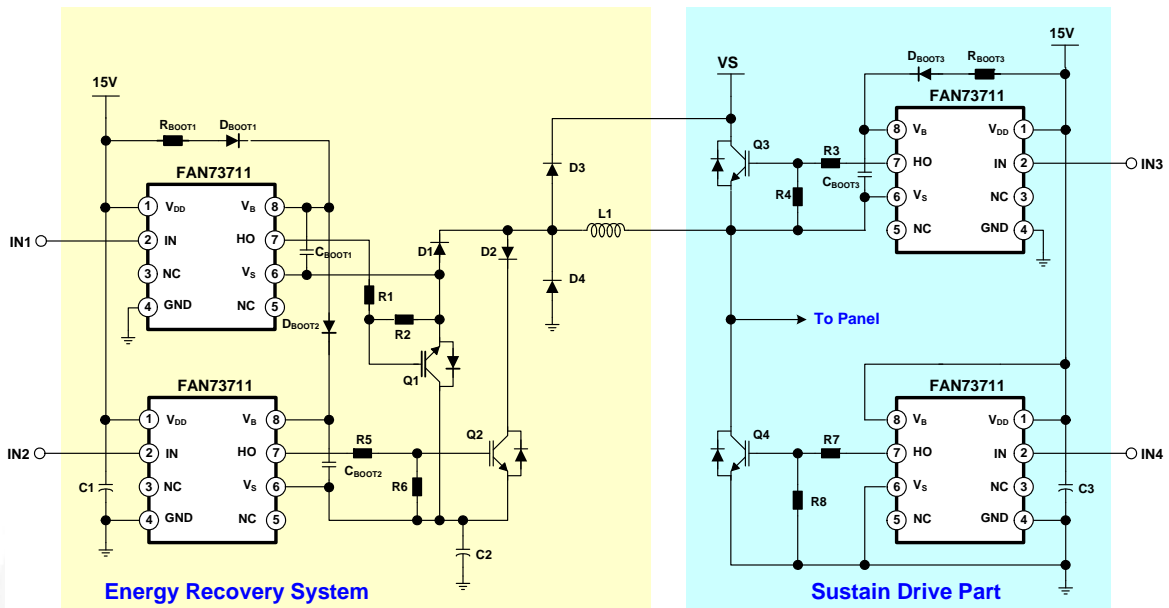
8-SOP



Ordering Information

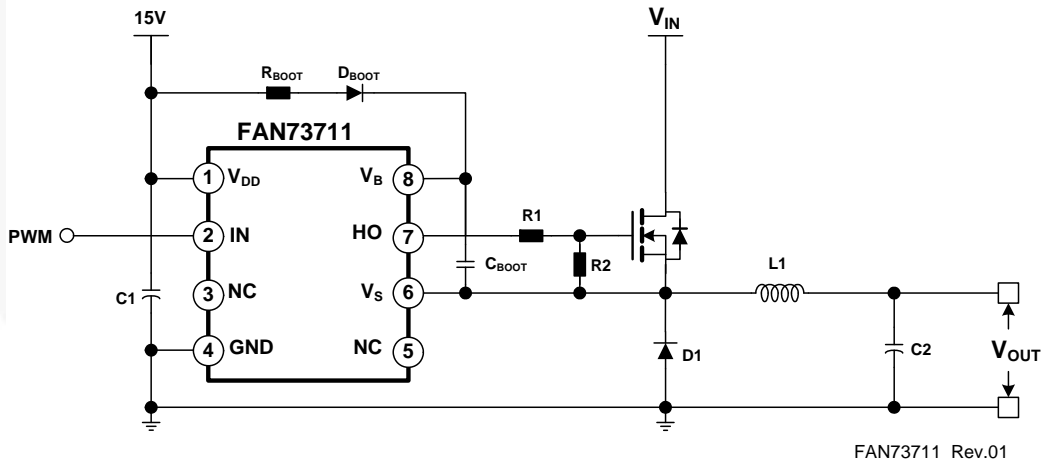
| Part Number | Operating Temperature Range | Package | Packing Method |
|-------------|-----------------------------|---------|----------------|
| FAN73711MX | 40°C ~ 125°C | 8-SOP | Tape and Reel |

Typical Application Diagrams



FAN73711 Rev.01

Figure 1. Floated Bi-Directional Switch and Half-Bridge Driver: PDP Application



FAN73711 Rev.01

Figure 2. Step-Down (Buck) DC-DC Converter Application

Internal Block Diagram

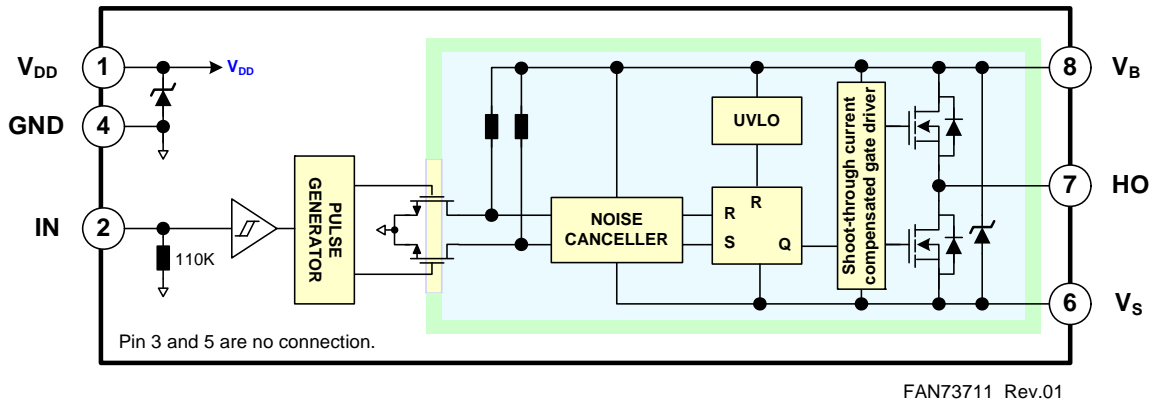


Figure 3. Functional Block Diagram

Pin Configuration

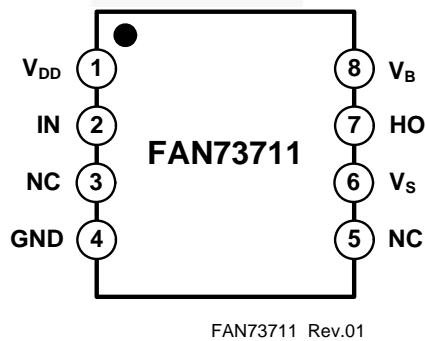


Figure 4. Pin Configuration (Top View)

Pin Definitions

| Pin # | Name | Description |
|-------|-----------------|--|
| 1 | V _{DD} | Supply Voltage |
| 2 | IN | Logic Input for High-Side Gate Driver Output |
| 3 | NC | No Connection |
| 4 | GND | Ground |
| 5 | NC | No Connection |
| 6 | V _S | High-Voltage Floating Supply Return |
| 7 | HO | High-Side Driver Output |
| 8 | V _B | High-Side Floating Supply |

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A=25^{\circ}\text{C}$ unless otherwise specified.

| Symbol | Characteristics | Min. | Max. | Unit |
|---------------|--|-------------------|----------------|-----------------------------|
| V_S | High-Side Floating Offset Voltage ⁽¹⁾ | $V_B - V_{SHUNT}$ | $V_B + 0.3$ | V |
| V_B | High-Side Floating Supply Voltage | -0.3 | 625.0 | V |
| V_{HO} | High-Side Floating Output Voltage | $V_S - 0.3$ | $V_B + 0.3$ | V |
| V_{DD} | Low-Side and Logic Supply Voltage ⁽¹⁾ | -0.3 | V_{SHUNT} | V |
| V_{IN} | Logic Input Voltage | -0.3 | $V_{DD} + 0.3$ | V |
| dV_S/dt | Allowable Offset Voltage Slew Rate | | ± 50 | V/ns |
| P_D | Power Dissipation ^(2,3,4) | | 0.625 | W |
| θ_{JA} | Thermal Resistance | | 200 | $^{\circ}\text{C}/\text{W}$ |
| T_J | Junction Temperature | -55 | +150 | $^{\circ}\text{C}$ |
| T_{STG} | Storage Temperature | -55 | +150 | $^{\circ}\text{C}$ |

Notes:

- This IC contains a shunt regulator on V_{DD} and V_{BS} . This supply pin should not be driven by a low-impedance voltage source greater than the V_{SHUNT} specified in the Electrical Characteristics section.
- Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR-4 glass epoxy material).
- Refer to the following standards:
JESD51-2: Integral circuits thermal test method environmental conditions, natural convection, and
JESD51-3: Low effective thermal conductivity test board for leaded surface-mount packages.
- Do not exceed power dissipation (P_D) under any circumstances.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Min. | Max. | Unit |
|----------|--|--------------|------------|--------------------|
| V_B | High-Side Floating Supply Voltage | $V_S + 10$ | $V_S + 20$ | V |
| V_S | High-Side Floating Supply Offset Voltage | $6 - V_{DD}$ | 600 | V |
| V_{HO} | High-Side Output Voltage | V_S | V_B | V |
| V_{IN} | Logic Input Voltage | GND | V_{DD} | V |
| V_{DD} | Supply Voltage | 10 | 20 | V |
| T_A | Operating Ambient Temperature | -40 | +125 | $^{\circ}\text{C}$ |

Electrical Characteristics

$V_{BIAS}(V_{DD}, V_{BS})=15.0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to GND. The V_O and I_O parameters are relative to V_S and are applicable to the respective output HO.

| Symbol | Characteristics | Test Condition | Min. | Typ. | Max. | Unit |
|------------------------------------|--|---|------|------|------|------------------|
| Power Supply Section | | | | | | |
| I_{QDD} | Quiescent V_{DD} Supply Current | $V_{IN}=0\text{ V or }5\text{ V}$ | | 25 | 70 | μA |
| I_{PDD} | Operating V_{DD} Supply Current | $f_{IN}=20\text{ kHz, No Load}$ | | 35 | 100 | μA |
| Bootstrapped Supply Section | | | | | | |
| V_{BSUV+} | V_{BS} Supply Under-Voltage Positive-Going Threshold Voltage | $V_{BS}=\text{Sweep}$ | 8.0 | 9.0 | 10.0 | V |
| V_{BSUV-} | V_{BS} Supply Under-Voltage Negative-Going Threshold Voltage | $V_{BS}=\text{Sweep}$ | 7.3 | 8.3 | 9.3 | V |
| V_{BSHYS} | V_{BS} Supply Under-Voltage Lockout Hysteresis Voltage | $V_{BS}=\text{Sweep}$ | | 0.7 | | V |
| I_{LK} | Offset Supply Leakage Current | $V_B=V_S=625\text{ V}$ | | | 10 | μA |
| I_{QBS} | Quiescent V_{BS} Supply Current | $V_{IN}=0\text{V or }5\text{ V}$ | | 60 | 120 | μA |
| I_{PBS} | Operating V_{BS} Supply Current | $C_{LOAD}=1000\text{ pF, }f_{IN}=20\text{ kHz, rms Value}$ | | 470 | 800 | μA |
| Shunt Regulator Section | | | | | | |
| V_{SHUNT} | V_{DD} and V_{BS} Shunt Regulator Clamping Voltage | $V_{DD}=\text{Sweep or }V_{BS}=\text{Sweep}$ $I_{SHUNT}=5\text{ mA}$ | 21 | 23 | 25 | V |
| Input Logic Section | | | | | | |
| V_{IH} | Logic "1" Input Voltage | | 2.5 | | | V |
| V_{IL} | Logic "0" Input Voltage | | | | 0.8 | V |
| I_{IN+} | Logic Input High Bias Current | $V_{IN}=5\text{ V}$ | | 40 | 65 | μA |
| I_{IN-} | Logic Input Low Bias Current | $V_{IN}=0\text{ V}$ | | | 2 | μA |
| R_{IN} | Input Pull-Down Resistance | | 90 | 110 | | $\text{K}\Omega$ |
| Gate Driver Output Section | | | | | | |
| V_{OH} | High Level Output Voltage ($V_{BIAS} - V_O$) | No Load | | | 1.2 | V |
| V_{OL} | Low Level Output Voltage | No Load | | | 30 | mV |
| I_{O+} | Output High, Short-Circuit Pulsed Current ⁽⁵⁾ | $V_{HO}=0\text{ V, }V_{IN}=5\text{ V, }PW \leq 10\ \mu\text{s}$ | 3 | 4 | | A |
| I_{O-} | Output Low, Short-Circuit Pulsed Current ⁽⁵⁾ | $V_{HO}=15\text{ V, }V_{IN}=0\text{ V, }PW \leq 10\ \mu\text{s}$ | 3 | 4 | | A |
| V_S | Allowable Negative V_S Pin Voltage for IN Signal Propagation to HO | | | -9.8 | -7.0 | V |

Note:

5. These parameters guaranteed by design.

Dynamic Electrical Characteristics

$V_{DD}=V_{BS}=15\text{ V}$, $\text{GND}=0\text{ V}$, $C_{LOAD}=1000\text{ pF}$, $T_A=25^\circ\text{C}$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|-----------|----------------------------|------------------|------|------|------|------|
| t_{on} | Turn-On Propagation Delay | $V_S=0\text{ V}$ | | 150 | 210 | ns |
| t_{off} | Turn-Off Propagation Delay | $V_S=0\text{ V}$ | | 150 | 210 | ns |
| t_r | Turn-On Rise Time | | | 25 | 50 | ns |
| t_f | Turn-Off Fall Time | | | 15 | 40 | ns |

Typical Characteristics

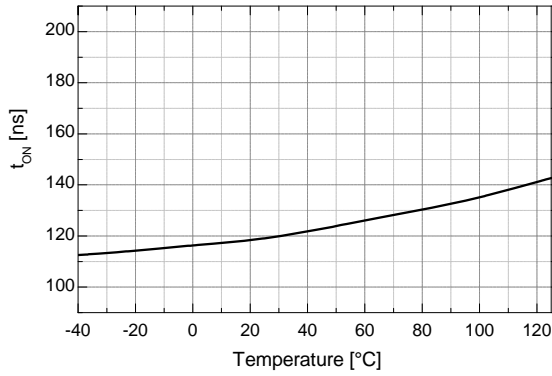


Figure 5. Turn-On Propagation Delay vs. Temperature

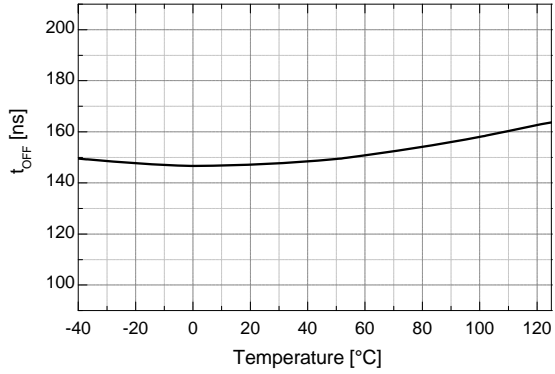


Figure 6. Turn-Off Propagation Delay vs. Temperature

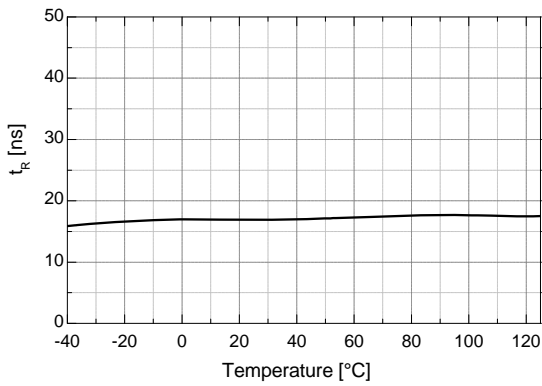


Figure 7. Turn-On Rise Time vs. Temperature

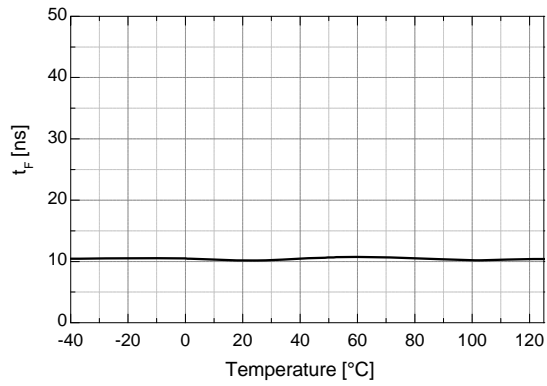


Figure 8. Turn-Off Fall Time vs. Temperature

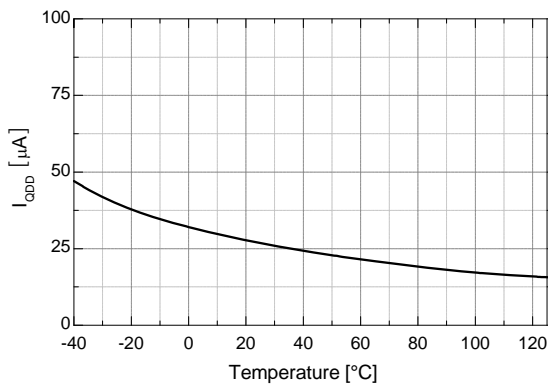


Figure 9. Quiescent V_{DD} Supply Current vs. Temperature

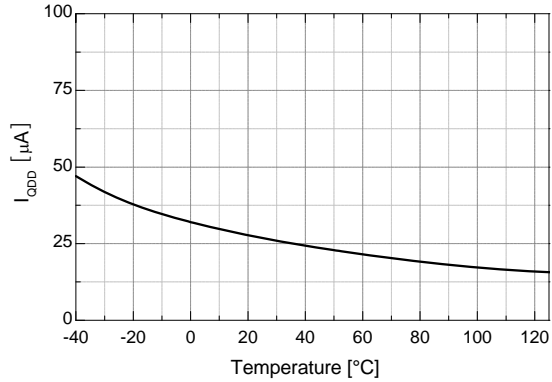


Figure 10. Quiescent V_{BS} Supply Current vs. Temperature

Typical Characteristics (Continued)

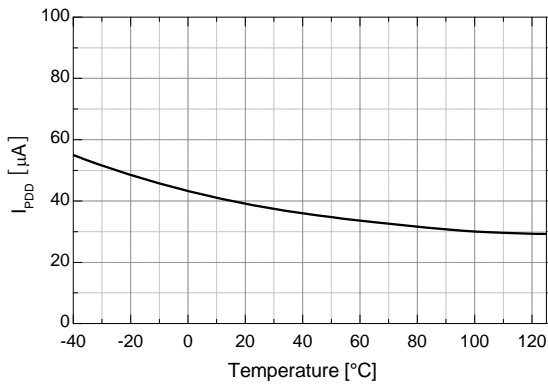


Figure 11. Operating V_{DD} Supply Current vs. Temperature

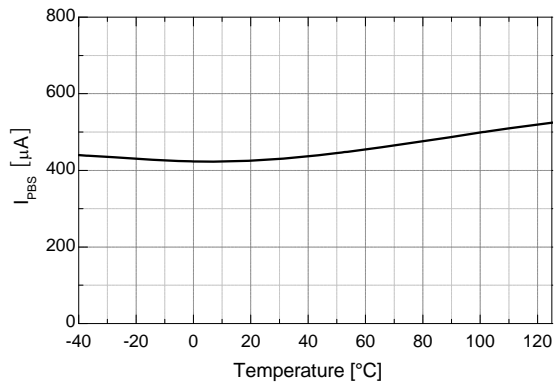


Figure 12. Operating V_{BS} Supply Current vs. Temperature

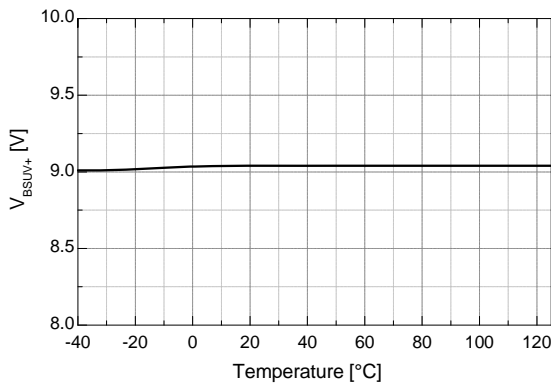


Figure 13. V_{BS} UVLO+ vs. Temperature

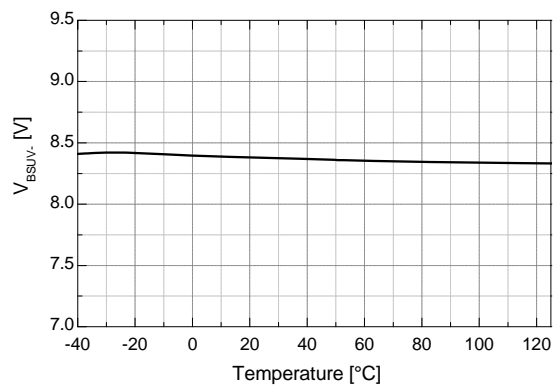


Figure 14. V_{BS} UVLO- vs. Temperature

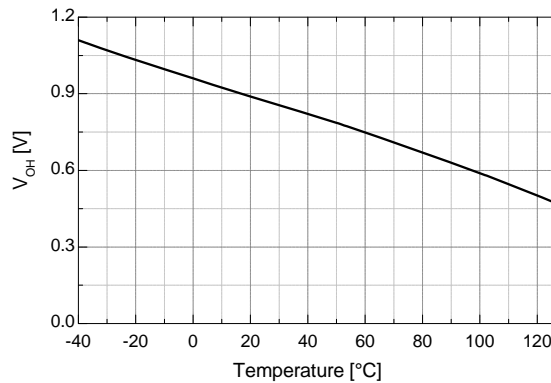


Figure 15. High-Level Output Voltage vs. Temperature

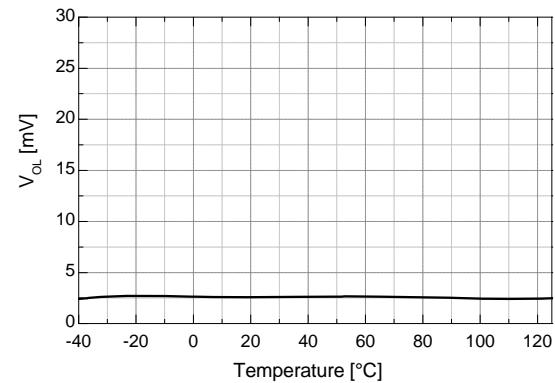


Figure 16. Low-Level Output Voltage vs. Temperature

Typical Characteristics (Continued)

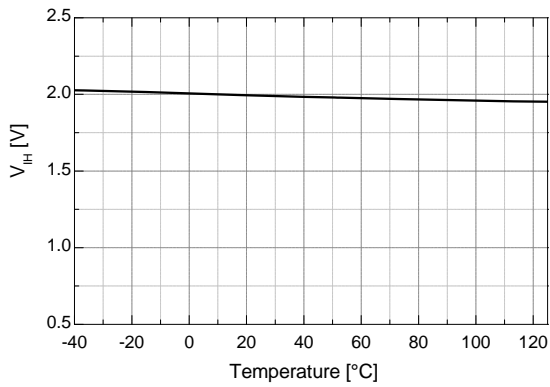


Figure 17. Logic High Input Voltage vs. Temperature

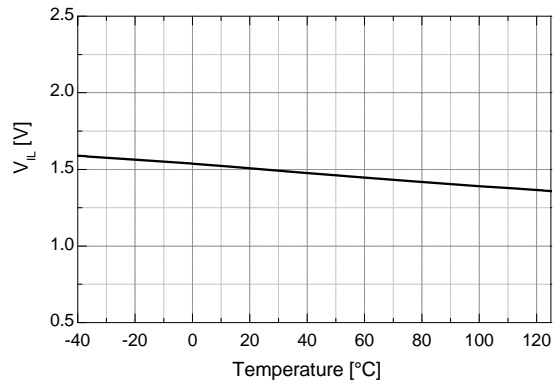


Figure 18. Logic Low Input Voltage vs. Temperature

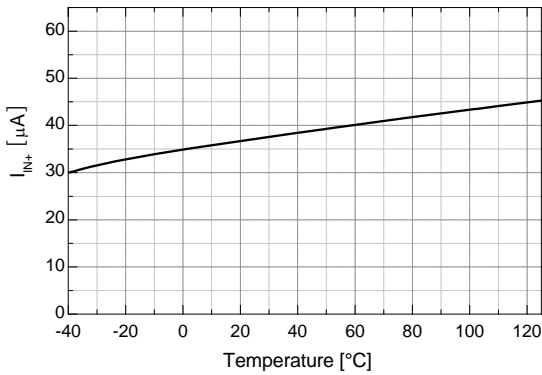


Figure 19. Logic Input High Bias Current vs. Temperature

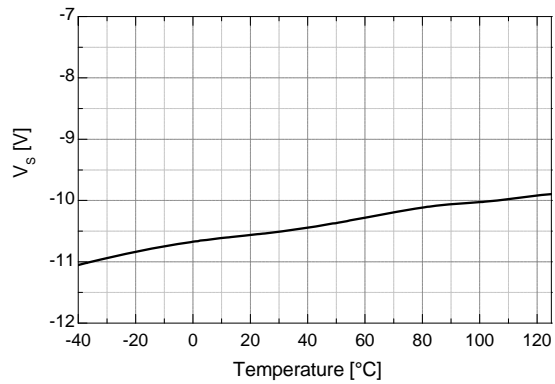


Figure 20. Allowable Negative V_S Voltage vs. Temperature

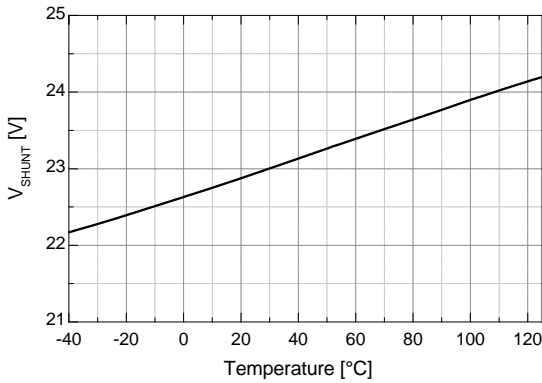


Figure 21. Shunt Regulator Clamping Voltage vs. Temperature

Switching Time Definitions

Timing Diagram

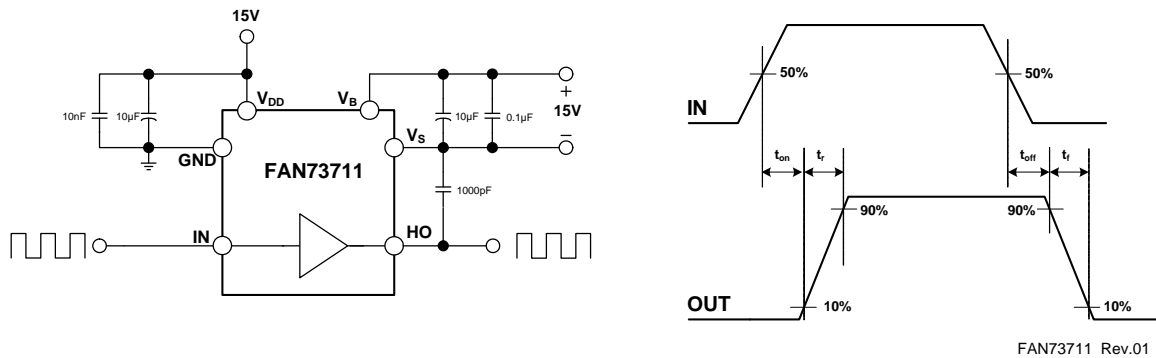


Figure 22. Switching Time Test Circuit and Waveform Definitions

Package Dimensions

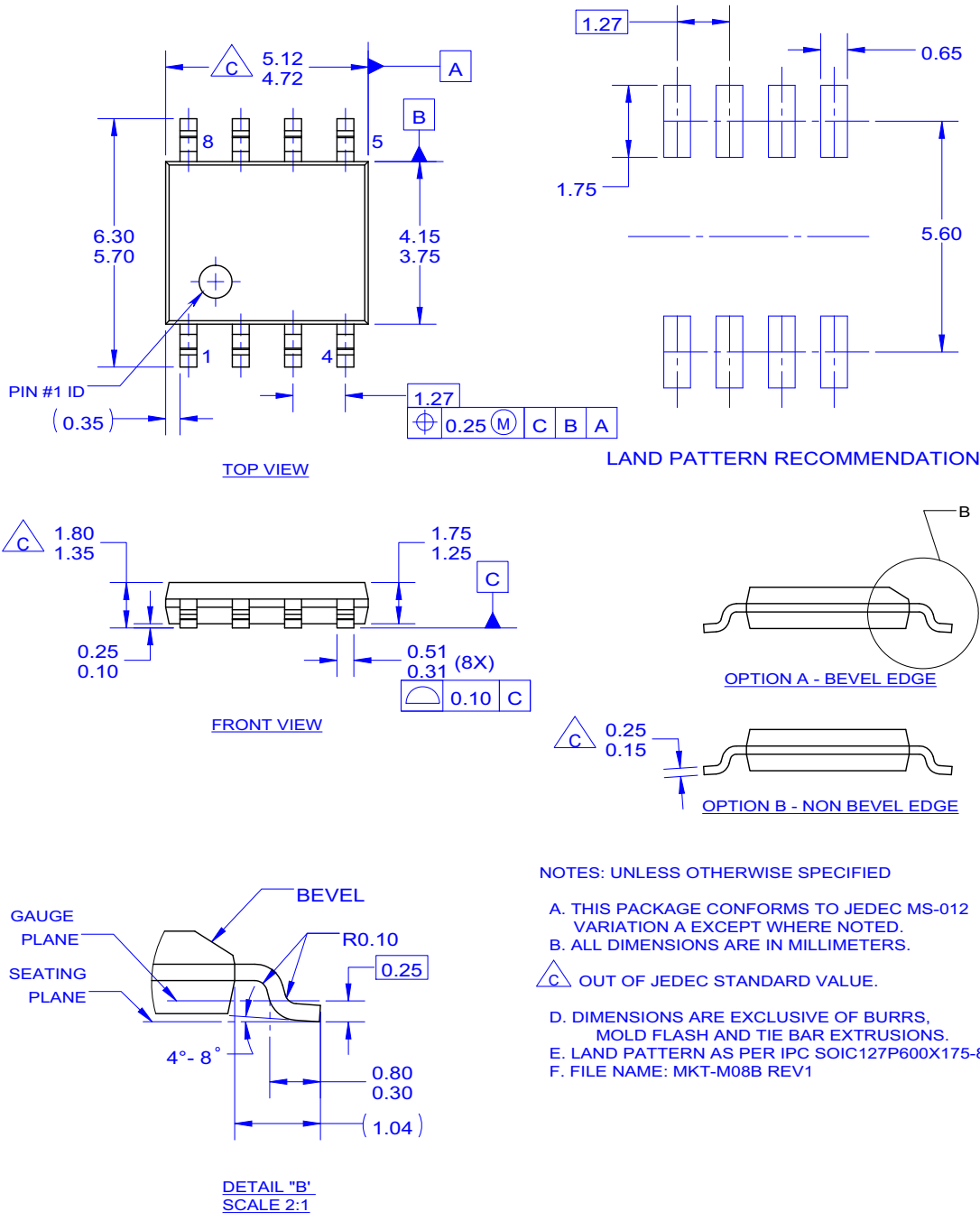


Figure 23. 8-Lead Small Outline Package (SOP)

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