TPS61187 White-LED Driver For Notebooks With PWM Interface and Automatic Phase Shift

1 Features

- Input Voltage 4.5 V to 24 V
- Maximum Output Voltage 38 V
- Integrated 2-A, 40-V MOSFET
- Programmable Switching Frequency 300 kHz to 1 MHz
- Adaptive Boost Output to WLED Voltages
- Wide PWM Dimming Frequency Range
  - 100 Hz to 50 KHz for Direct PWM Mode
  - 100 Hz to 22 KHz for Frequency Programmable Mode
- 100:1 Dimming Ratio at 20 kHz
- 10000:1 Dimming Ratio at 200 Hz (Direct PWM mode)
- Small External Components
- Integrated Loop Compensation
- Six Current Sinks of 30 mA Maximum
- 1.5% (Typical) Current Matching
- PWM Brightness Interface Control
- PWM Phase Shift Mode Brightness Dimming Method or Direct PWM Dimming Method
- HBM ESD Protection 4 kV
- Programmable Overvoltage Threshold
- Built-in WLED Open/Short Protection
- Thermal Shutdown

2 Applications

Notebook LCD Display Backlight

3 Description

The TPS61187 device provides a highly integrated white-light-emitting-diode (WLED) driver solution for notebook LCD backlight. This device has a built-in high efficiency boost regulator with integrated 2-A, 40-V power MOSFET. The six current sink regulators provide high precision current regulation and matching. In total, the device can support up to 60 WLEDs. In addition, the boost output automatically adjusts its voltage to the WLED forward voltage to optimize efficiency.

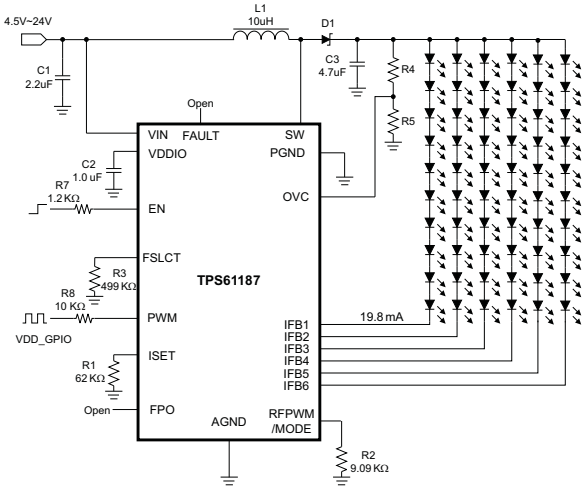
The TPS61187 supports the automatic phase-shift-dimming method and direct-PWM-dimming method. During phase-shift-PWM dimming, the WLED current is turned on and turned off at the duty cycle controlled by the input PWM signal, and each channel is shifted according to the frequency determined by an integrated pulse-width-modulation (PWM) signal. The frequency of this signal is resistor programmable, while the duty cycle is controlled directly from an external PWM signal input to the PWM pin. During direct PWM dimming, the WLED current is turned on and/or turned off synchronized with the input PWM signal.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS61183	WQFN (20)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application – Phase Shift PWM Mode



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (February 2012) to Revision E — **Page**

- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* and *Thermal Information* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Deleted Ordering table - information in POA ... 1
- Added last 2 sentences of *IFB Pin Unused* ... 12

Changes from Revision C (September 2011) to Revision D — **Page**

- Changed Figure 18 X axis unit from mA to A ... 20
- Changed Figure 19 X axis unit from mA to A ... 20

Changes from Revision B (April 2011) to Revision C — **Page**

- Added a description paragraph and replaced Figure 15 in the PHASE SHIFT PWM DIMMING section ... 13

Changes from Revision A (July 2010) to Revision B — **Page**

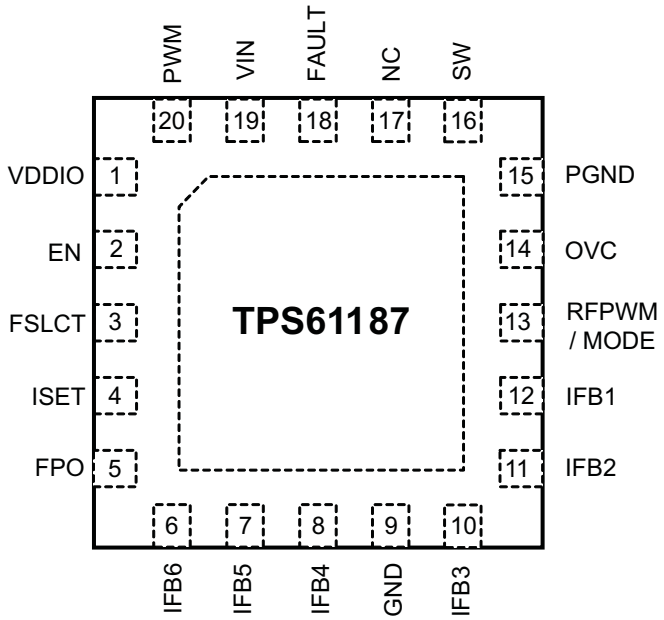
- Changed in ABS MAX table, in row "All other pins", MAX col: from 3.6 to 3.7 ... 4

Changes from Original (June 2010) to Revision A — **Page**

- Changed Typical Application graphic ... 1
- Changed ceramic capacitor value, attached to VDDIO, from 0.1 to 1 µF ... 3
- Changed bypass capacitor value in SUPPLY VOLTAGE section from 0.1 to 1 µF. ... 11
- Changed BRIGHTNESS DIMMING CONTROL section ... 12
- Deleted PWM BRIGHTNESS CONTROL INTERFACE section ... 13

5 Pin Configuration and Functions

RTJ Package
20-Pin QFN With Thermal Pad
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDDIO	A	Internal pre-regulator. Connect a 1-µF ceramic capacitor to VDDIO.
2	EN	I	Enable
3	FSLCT	I	Switching frequency selection pin. Use a resistor to set the frequency between 300 kHz to 1 MHz.
4	ISET	I	Full-scale LED current set pin. Connecting a resistor to the pin programs the current level.
5	FPO	O	Fault protection output to indicate fault conditions including OVP, OC, and OT.
6, 7, 8, 10,11,12	IFB1 to IFB6	A	Regulated current sink input pins
9,	GND	G	Analog ground
13	RFPWM / MODE	I	Dimming frequency program pin with an external resistor / mode selection, see(1)
14	OVC	A	Overvoltage clamp pin / voltage feedback, see(1)
15	PGND	G	Power ground
16	SW	A	Drain connection of the internal power FET
17	NC	—	No connection
18	FAULT	O	Fault pin to drive external ISO FET
19	VIN	A	Supply input pin
20	PWM	I	PWM signal input pin
—	Thermal Pad	—	Connect to GND plane for better thermal performance.
A: Analog; G: Ground; I: Input: O: Output; P: Power			

(1) See *Application and Implementation* for details.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage range(2)	VIN, FAULT	–0.3	24	V
	FPO	–0.3	7	V
	SW	–0.3	40	V
	EN, PWM, IFB1 to IFB4	–0.3	20	V
	VDDIO	–0.3	3.7	V
	All other pins	–0.3	3.6	V
Continuous power dissipation		See *Thermal Information*		
Operating junction temperature range		–40	150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
		Machine model	200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	4.5		24	V
V_{OUT}	Output voltage	V_{IN}		38	V
L1	Inductor, 600-kHz to 1-MHz switching frequency	10		22	µH
L1	Inductor, 300-kHz to 600-kHz switching frequency	22		47	µH
C_I	Input capacitor	1			µF
C_O	Output capacitor	1	4.7	10	µF
F_{PWM_O}	IFBx PWM dimming frequency - frequency programmable mode	0.1		22(1)	KHz
F_{PWM_O}	IFBx PWM dimming frequency - direct PWM mode	0.1		50	KHz
F_{PWM_I}	PWM input signal frequency	0.1		22	KHz
F_{BOOST}	Boost regulator switching frequency	300		1000	KHz
T_A	Operating free-air temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) 5-µs minimum pulse on time.

6.4 Thermal Information

THERMAL METRIC(1)		TPS61187 RTJ (WQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	34.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.5	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	2	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

6.5 Electrical Characteristics

V_{IN} = 12 V, PWM/EN = high, IFB current = 20 mA, IFB voltage = 500 mV, T_A = –40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		4.5		24	V
I_{Q_VIN}	Operating quiescent current into V_{IN}	Device enable, switching 1 MHz and no load, V_{IN} = 24 V			4	mA
VDDIO	VDDIO pin output voltage	I_{LOAD} = 5 mA	3	3.3	3.6	V
I_{SD}	Shutdown current	V_{IN} = 12 V , EN = low			11	µA
		V_{IN} = 24 V, EN = low			16	
V_{IN_UVLO}	V_{IN} undervoltage lockout threshold	V_{IN} ramp down			3.5	V
		V_{IN} ramp up			3.75	
V_{IN_Hys}	V_{IN} undervoltage lockout hysterisis			250		mV
PWM						
V_H	EN logic high threshold	EN	2.1			V
V_L	EN logic low threshold	EN			0.8	
V_H	PWM logic high threshold	PWM	2.1			
V_L	PWM logic low threshold	PWM			0.8	
R_{PD}	Pulldown resistor on PWM and EN		400	800	1600	kΩ
CURRENT REGULATION						
V_{ISET}	ISET pin voltage		1.204	1.229	1.253	V
K_{ISET}	Current multiplier			980		
I_{FB}	Current accuracy	I_{ISET} = 20 µA, 0°C to 70°C	–2%		2%	
		I_{ISET} = 20 µA, –40°C to 85°C	–2.3%		2.3%	
K_m	$(I_{max}–I_{min}) / I_{AVG}$	I_{ISET} = 20 µA		1.3%		
I_{leak}	IFB pin leakage current	IFB voltage = 15 V, each pin		2	5	µA
		IFB voltage = 5 V, each pin		1	2	
I_{IFB_max}	Current sink max output current	IFB = 350 mV	30			mA
f_{dim}	PWM dimming frequency	R_{FPWM} = 9.09 kΩ		20		kHz

Electrical Characteristics (continued)

V_{IN} = 12 V, PWM/EN = high, IFB current = 20 mA, IFB voltage = 500 mV, T_A = –40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BOOST OUTPUT REGULATION						
V_{IFB_L}	Output voltage up threshold	Measured on $V_{IFB(min)}$		350		mV
V_{IFB_H}	Ouput voltage down threshold	Measured on $V_{IFB(min)}$		650		mV
POWER SWITCH						
R_{PWM_SW}	PWM FET on-resistance	V_{IN} = 12 V		0.25	0.35	Ω
I_{LN_NFET}	PWM FET leakage current	V_{SW} = 40 V, T_A = 25°C			2	µA
OSCILLATOR						
f_S	Oscillator frequency	R_{FSW} = 499 kΩ	0.8	1	1.2	MHz
D_{max}	Maximum duty cycle	IFB = 0		94%		
OC, SC, OVP, AND SS						
I_{LIM}	N-channel MOSFET current limit	D = D_{max}	2		3	A
V_{CLAMP_TH}	Ouput voltage clamp program threshold		1.90	1.95	2	V
V_{OVP_IFB}	IFB overvoltage threshold	Measured on the IFBx pin, IFB on	12	13.5	15	V
FPO, FAULT						
V_{FPO_L}	FPO Logic low voltage	$I_{\_SOURCE}$ = 0.5 mA			0.4	V
V_{FAULT_HIGH}	Fault high voltage	Measured as V_{IN} – V_{FAULT}		0.1		V
V_{FAULT_LOW}	Fault low voltage	Measured as V_{IN} – V_{FAULT} , Sink, 10 µA	6	8	10	V
I_{FAULT}	Maximum sink current	V_{IN} – V_{FAULT} = 0 V		20		µA
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			150		°C
	Thermal shutdown hysteresis			15		

6.6 Typical Characteristics

6.6.1 Table Of Graphs

TITLE	DESCRIPTION	FIGURE
Dimming linearity	V_{OUT} = 32 V, V_{IN} = 8 V, 12 V, 24 V, F_{DIM} = 20 KHz, L = 10 µH, R_{ISET} = 62 kΩ	Figure 1
Dimming linearity	V_{OUT} = 32 V, V_{IN} = 8 V, 12 V, 24 V, F_{DIM} = 200 Hz, L = 10 µH, R_{ISET} = 62 kΩ	Figure 2
Boost switching frequency	V_{IN} = 12 V, V_{OUT} = 33.8 V, L = 10 µH, R_{ISET} = 62 kΩ	Figure 3
Phase shift dimming frequency	V_{IN} = 12 V, V_{OUT} = 33.8 V, L = 10 µH, R_{ISET} = 62 kΩ	Figure 4
Switch waveform	V_{IN} = 8 V, V_{OUT} = 33.8 V, F_{DIM} = 20 kHz, Duty = 100%, L = 10 µH, R_{ISET} = 62 kΩ	Figure 5
Switch waveform	V_{IN} = 12 V, V_{OUT} = 33.8 V, F_{DIM} = 20 kHz, Duty = 100%, L = 10 µH, R_{ISET} = 62 kΩ	Figure 6
Phase shift PWM dimming F_{DIM} = 200Hz, duty = 50%	V_{IN} = 12 V, V_{OUT} = 33.8 V, F_{DIM} = 20 kHz, Duty = 45%, L = 10 µH, R_{ISET} = 62 kΩ	Figure 7
Phase shift PWM dimming F_{DIM} = 20KHz, duty = 50%	V_{IN} = 12 V, V_{OUT} = 33.8 V, F_{DIM} = 20 kHz, Duty = 51%, L = 10 µH, R_{ISET} = 62 kΩ	Figure 8
Output ripple of Phase shift PWM dimming	V_{IN} = 12 V, V_{OUT} = 33.8 V, F_{DIM} = 20 kHz, Duty = 50%, L = 10 µH, R_{ISET} = 62 kΩ	Figure 9
Output ripple of Phase shift PWM dimming	V_{IN} = 12 V, V_{OUT} = 33.8 V, F_{DIM} = 20 kHz, Duty = 70%, L = 10 µH, R_{ISET} = 62 kΩ	Figure 10
Start-up waveform	V_{IN} = 12 V, V_{OUT} = 33.8 V, F_{DIM} = 20 kHz, Duty = 100%, L = 10 µH, R_{ISET} = 62 kΩ	Figure 11
Start-up waveform	V_{IN} = 12 V, V_{OUT} = 33.8 V, F_{DIM} = 20 kHz, Duty = 50%, L = 10 µH, R_{ISET} = 62 kΩ	Figure 12

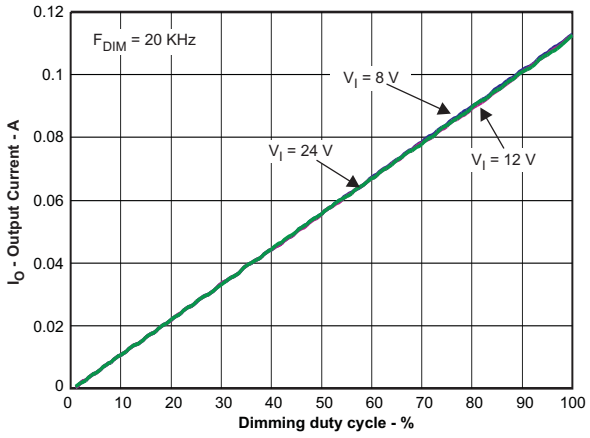


Figure 1. Output Current

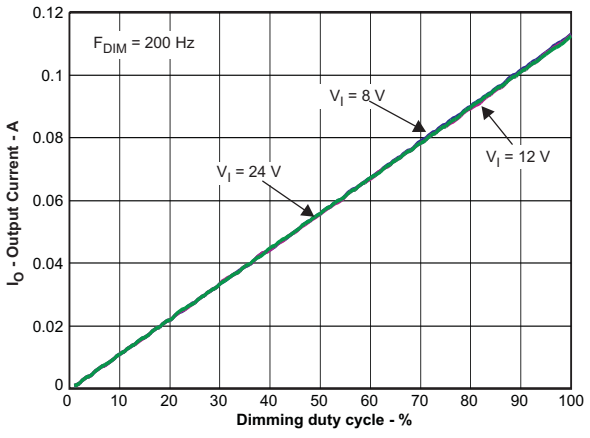


Figure 2. Output Current

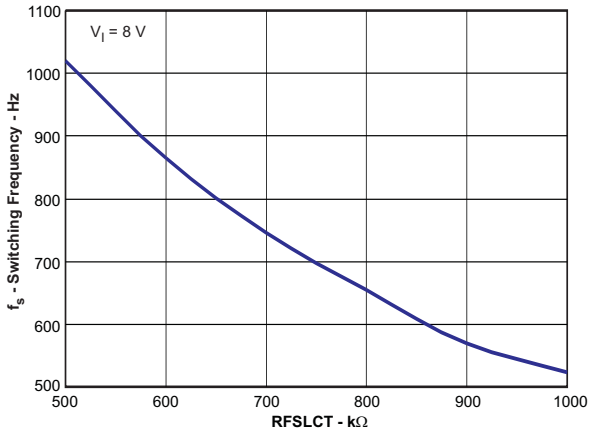


Figure 3. Switching Frequency

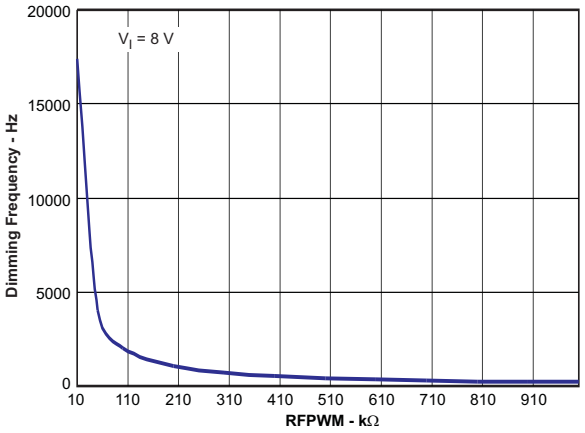


Figure 4. Dimming Frequency

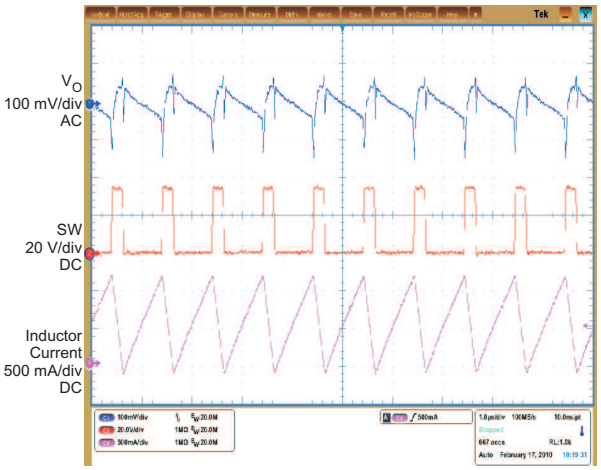


Figure 5. Switch Waveform

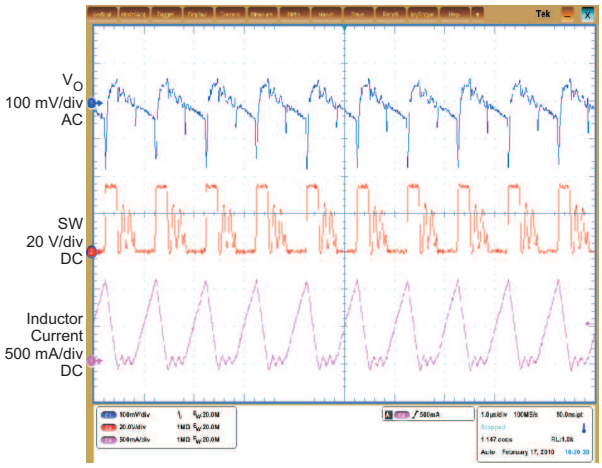


Figure 6. Switch Waveform

Figure 7. Phase-Shift Waveform

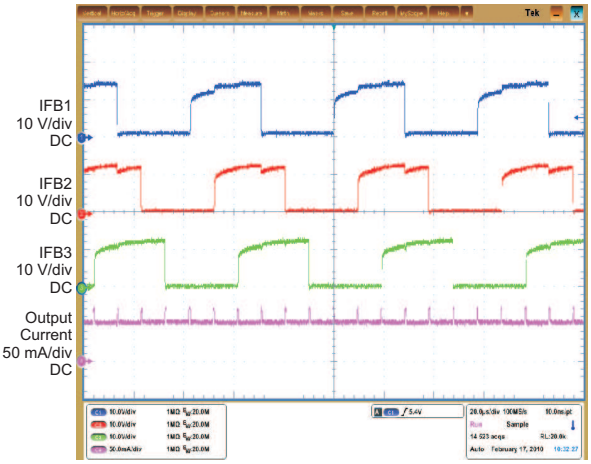


Figure 8. Phase-Shift Waveform

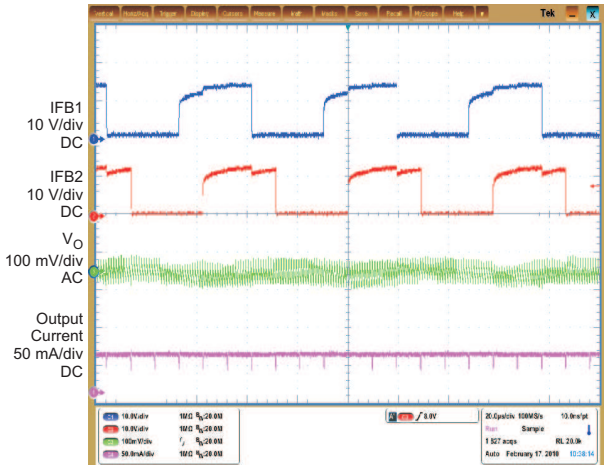


Figure 9. Output Ripple Waveform

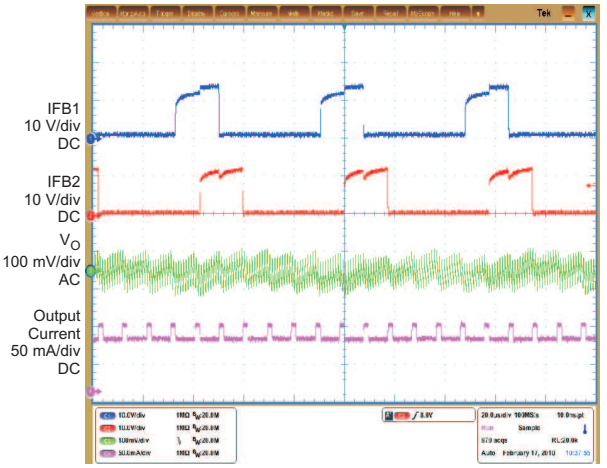


Figure 10. Output Ripple Waveform

Figure 11. Start-Up Waveform

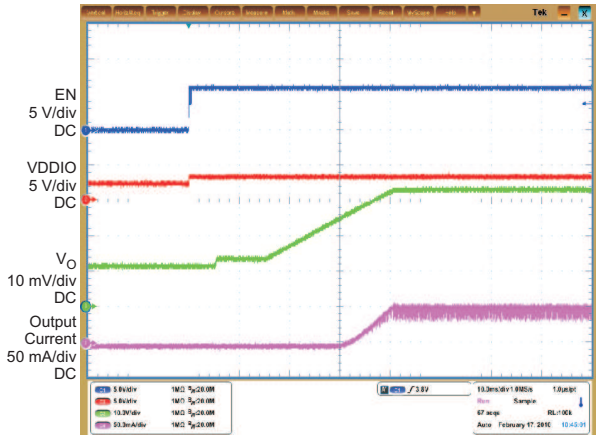


Figure 12. Start-Up Waveform

7 Detailed Description

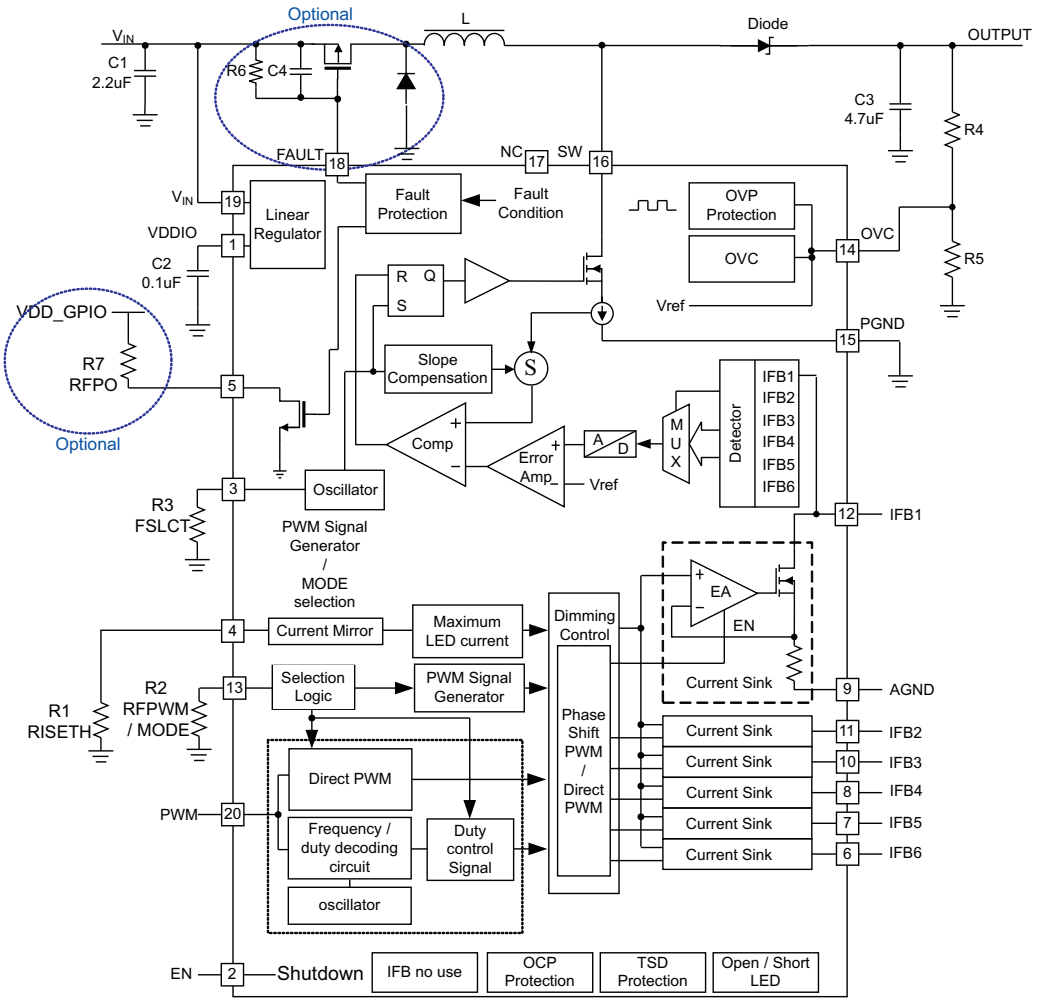
7.1 Overview

The TPS61187 is a high-efficiency, high-output-voltage WLED driver for notebook panel backlighting applications. The advantages of WLEDs compared to cold cathode fluorescent lamp (CCFL) backlights are higher power efficiency and lower profile design. Due to the large number of WLEDs required to provide backlighting for medium to large display panels, the LEDs must be arranged in parallel strings of several LEDs in series. Therefore, the backlight driver for battery powered systems is almost always a boost regulator with multiple current sink regulators. Having more WLEDs in series reduces the number of parallel strings, and therefore improves overall current matching. However, the efficiency of the boost regulator declines due to the need for high output voltage. Also, there must be enough white LEDs in series to ensure the output voltage stays above the input voltage range.

The TPS61187 device has integrated all of the key function blocks to power and control up to 60 WLEDs. The device includes a 40-V, 2-A boost regulator, six 30-mA current sink regulators, and a protection circuit for overcurrent, overvoltage, open LED, short LED, and output short-circuit failures.

The TPS61187 device integrates auto phase shifted PWM dimming methods with the PWM interface to reduce the output ripple voltage and audible noise. An optional direct PWM mode is user selectable through the MODE selection function.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Supply Voltage

The TPS61187 device has a built-in linear regulator to supply the device analog and logic circuit. The VDDIO pin, output of the regulator, is connected to a 1-µF bypass capacitor for the regulator to be controlled in a stable loop. VDDIO does not have high current sourcing capability for external use but it can be tied to the EN pin for start up.

7.3.2 Boost Regulator and Programmable Switch Frequency (FSCLT)

The fixed-frequency PWM boost converter uses current-mode control and has integrated loop compensation. The internal compensation ensures stable output over the full input and output voltage ranges assuming the recommended inductance and output capacitance values shown in *Typical Application – Phase Shift PWM Mode* are used. The output voltage of the boost regulator is automatically set by the device to minimize voltage drop across the IFB pins. The device regulates the lowest IFB pin to 350 mV and consistently adjusts the boost output voltage to account for any changes in LED forward voltages. If the input voltage is higher than the sum of the WLED forward voltage drops (for example, at low duty cycles), the boost converter is not able to regulate the output due to its minimum duty cycle limitation. In this case, increase the number of WLEDs in series or include series ballast resistors in order to provide enough headroom for the converter to boost the output voltage. Because the TPS61187 integrates a 2-A, 40-V power MOSFET, the boost converter can provide up to a 38-V output voltage.

The TPS61187 switching frequency can be programmed between 300 kHz to 1 MHz by the resistor value on the FSLCT pin according to Equation 1:

$$F_{SW} = \frac{5 \times 10^{11}}{R_{FSLCT}} \quad (1)$$

where

- R_{FSLCT} = FSCLT pin resistor

See Figure 3 for boost converter switching frequency adjustment resistor R_{FSLCT} selection.

The adjustable switching frequency feature provides the user with the flexibility of choosing a faster switching frequency, as well as an inductor with smaller inductance and footprint or slower switching frequency, and therefore, potentially higher efficiency due to lower switching losses. Use Equation 1 or refer to Table 1 to select the correct value:

Table 1. R_{FSLCT} Recommendations

R_{FLCT}	F_{SW}
833 kΩ	600 KHz
625 kΩ	800 KHz
499 kΩ	1 MHz

7.3.3 LED Current Sinks

The six current sink regulators embedded in the TPS61187 can be collectively configured to provide up to a maximum of 30 mA each. These six specialized current sinks are accurate to within ±2% maximum for currents at 20 mA, with a string-to-string difference of ±1.5% typical.

The IFB current must be programmed to the highest WLED current expected using the ISETH pin resistor and Equation 2.

$$I_{FB} = \frac{V_{ISETH}}{R_{ISETH}} \times K_{ISET} \quad (2)$$

where

- K_{ISET} = 980 (current multiple)
- V_{ISETH} = 1.229 V (ISETH pin voltage)
- R_{ISETH} = ISETH pin resistor

7.3.4 Enable and Start-up

The internal regulator which provides VDDIO wakes up as soon as V_{IN} is applied even when EN is low. This allows the device to start when EN is tied to the VDDIO pin. VDDIO does not come to full regulation until EN is high. The TPS61187 checks the status of all current feedback channels and shuts down any unused feedback channels. It is recommended to short the unused channels to ground for faster start-up.

After the device is enabled, if the PWM pin is left floating, the output voltage of the TPS61187 regulates to the minimum output voltage. Once the device detects a voltage on the PWM pin, the TPS61187 begins to regulate the IFB pin current, as pre-set per the ISETH pin resistor, according to the duty cycle of the signal on the PWM pin. The boost converter output voltage rises to the appropriate level to accommodate the sum of the white LED string with the highest forward voltage drops plus the headroom of the current sink at that current.

Pulling the EN pin low shuts down the device, resulting in the device consuming less than 11 µA in shutdown mode.

7.3.5 IFB Pin Unused

The TPS61187 has open/short string detection. For an unused IFB string, simply short it to ground or leave it open. TI recommend shorting unused IFB pins to ground for faster start-up. After EN is pulled high, the TPS61187 outputs about 40–µA current to each current channel for 4 ms and measures the voltage on each channel. If the voltage on any channel is less than 600 mV, the channel is turned off and removed from the boost control loop as unused channel.

7.4 Device Functional Modes

7.4.1 Brightness Dimming Control

The TPS61187 has auto-phase-shifted PWM dimming control with the PWM control interface.

The internal decoder block detects duty information from the input PWM signal, saves it in an eight bit register and delivers it to the output PWM dimming control circuit. The output PWM dimming control circuit turns on/off six output current sinks at the PWM frequency set by RFPWM and the duty cycle from the decoder block.

The TPS61187 also has direct PWM dimming control with the PWM control interface. In direct PWM mode, each current sink turns on/off at the same frequency and duty cycle as the input PWM signal. See the *Mode Selection – Phase-Shift PWM Or Direct PWM Dimming* for dimming mode selection.

When in phase-shifted PWM mode, TI recommends insertion of a series resistor of 10 kΩ to 20 kΩ value close to the PWMIN pin. This resistor together with an internal capacitor forms a low pass R-C filter with 30-ns to 60-ns time constant. This prevents possible high frequency noises being coupled into the input PWM signal and causing interference to the internal duty cycle decoding circuit. However, it is not necessary for direct PWM mode because the duty cycle decoding circuit is disabled during the direct PWM mode.

7.4.2 Adjustable PWM Dimming Frequency and Mode Selection (R_FPWM/MODE)

The TPS61187 can operate in auto phase shift mode or direct PWM mode. Tying the RFPWM/MODE pin to VDDIO forces the device to operate in direct PWM mode. A resistor between the RFPWM/MODE pin and ground sets the device into auto-phase-shift mode and the value of the resistor determines the PWM dimming frequency. Use Equation 3 or refer to Table 2 to select the correct value:

$$F_{DIM} = \frac{1.818 \times 10^8}{R_{FPWM}} \quad (3)$$

where

- R_{FPWM} = RFPWM pin resistor

Table 2. R_{FPWM} Recommendations

R_{FPWM}	F_{DIM}
866 kΩ	210 Hz
432 kΩ	420 Hz
174 kΩ	1.05 kHz
9.09 kΩ	20 kHz

7.4.3 Mode Selection – Phase-Shift PWM Or Direct PWM Dimming

The phase-shift PWM dimming method or direct PWM dimming method can be selected through the RFPWM pin. By attaching an external resistor to the RFPWM pin, the default phase shift PWM mode can be selected. To select direct PWM mode, the RFPWM pin needs to be tied to the VDDIO pin. The RFPWM/MODE pin can be noise sensitive when R2 has high impedance. In this case, careful layout or a parallel bypassing capacitor improves noise sensitivity but the value of the parallel capacitor may not exceed 33 pF for oscillator stability.

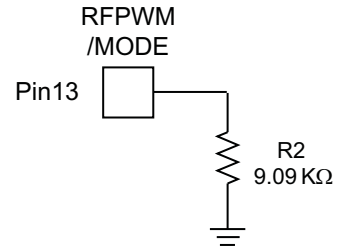


Figure 13. Phase-Shift PWM-Dimming-Mode Selection

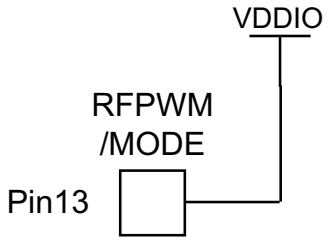


Figure 14. Direct PWM-Dimming-Mode Selection

7.4.3.1 Phase-Shift PWM Dimming

In phase-shift PWM mode, all current feedback channels are turned on and off at F_{DIM} frequency with a constant delay. However, the number of used channels and PWM dimming frequency determine the delay time between two neighboring channels per Equation 4.

$$T\_delay = \frac{1}{n \times F_{DIM}} \quad (4)$$

where

- n is the number of used channels
- F_{DIM} is the PWM dimming frequency that is determined by the value of R_{FPWM} on the RFPWM pin

Figure 15 provides the detailed timing diagram of the phase-shift PWM dimming mode.

In phase-shift PWM mode, the internal decoder converts the duty-cycle information from the applied PWM signal at the PWM pin into an 8-bit digital signal and stores it into a register. The integrated dimming control circuit reconstructs the PWM duty cycle per the register value and sends it to each of the current sinks. In order to avoid any flickering while the duty cycle information is reconstructed from the register, one LSB (1/256) of duty cycle hysteresis is included which results in 1/256 resolution when incrementing the applied signal's duty cycle but 2/256 resolution when decrementing the duty cycle.

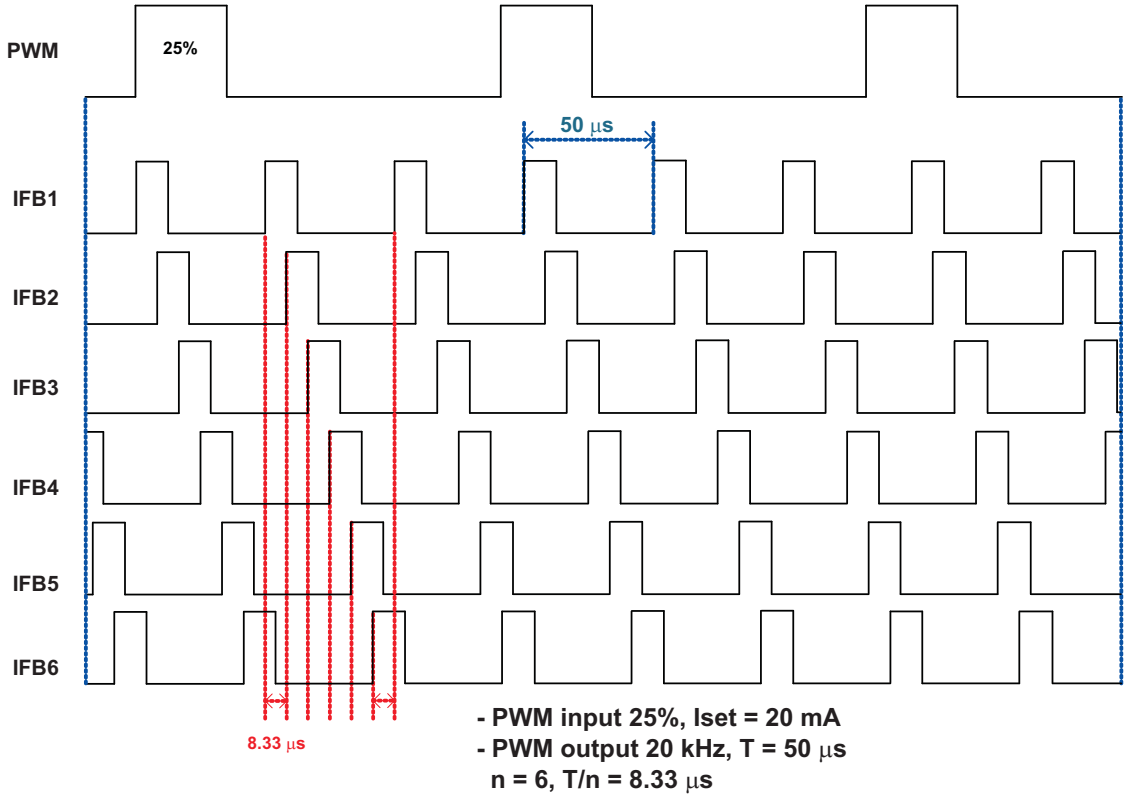


Figure 15. Phase-Shift PWM Dimming Timing Diagram

7.4.3.2 Direct PWM Dimming

In direct PWM mode, all current feedback channels are turned on and off and are synchronized with the input PWM signal.

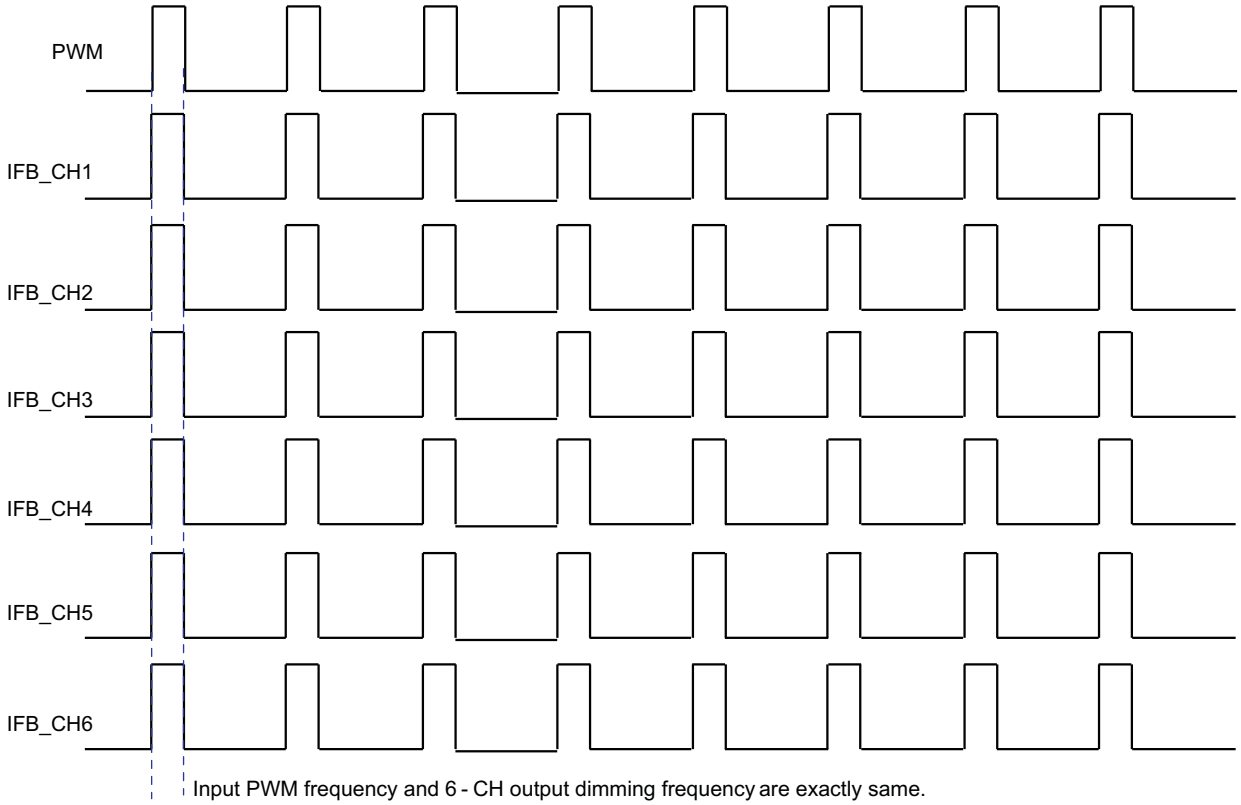


Figure 16. Direct PWM Dimming Timing Diagram

7.4.4 Overvoltage Clamp and Voltage Feedback (OVC / FB)

The correct divider ratio is important for optimum operation of the TPS61187. Use the following guidelines to choose the divider value. It can be noise sensitive if R_{upper} and R_{down} have high impedance. Careful layout is required. Also, choose lower resistance values for R_{upper} and R_{down} when power dissipation allows.

1. Determine the maximum output voltage, V_O, for the system according to the number of series WLEDs.
2. Select an R_{upper} resistor value (1 MΩ for a typical application; a lower value such as 100 kΩ for a noisy environment).
3. Calculate R_{down} using Equation 5

$$V_{OVP} = \left(\frac{R_{upper}}{R_{down}} + 1 \right) \times V_{OV\_TH} \quad (5)$$

where

- V_{OV_TH} = 1.95 V

When the device detects that the OVC pin exceeds 1.95 V typical, indicating that the output voltage is over the set threshold point, the OVC circuitry clamps the output voltage to the set threshold.

7.4.5 Current-Sink Open Protection

For the TPS61187, if one of the WLED strings is open, the device automatically detects and disables that string. The device detects the open WLED string by sensing no current in the corresponding IFB pin. As a result, the device deactivates the open IFB pin and removes it from the voltage feedback loop. Subsequently, the output voltage drops and is regulated to the minimum voltage required for the connected WLED strings. The IFB current of the connected WLED strings remains in regulation.

If any IFB pin voltage exceeds the IFB overvoltage threshold (13.5 V typical), the device turns off the corresponding current sink and removes this IFB pin from the regulation loop. The current regulation of the remaining IFB pins is not affected. This condition often occurs when there are several shorted WLEDs in one string. WLED mismatch typically does not create large voltage differences among WLED strings.

The device only shuts down if it detects that all of the WLED strings are open. If an open string is reconnected again, a power-on reset (POR) or EN pin toggling is required to reactivate a previously deactivated string.

7.4.6 Overcurrent and Short-Circuit Protection

The TPS61187 has a pulse-by-pulse over-current limit of 2 A (minimum). The PWM switch turns off when the inductor current reaches this current threshold. The PWM switch remains off until the beginning of the next switching cycle. This protects the device and external components during on overload conditions. When there is a sustained overcurrent condition, the device turns off and requires a POR or EN pin toggling to restart. Under severe overload and/or short-circuit conditions, the boost output voltage can be pulled below the required regulated voltage to keep all of the white LEDs operating. Under thses conditions, the current flows directly from input to output through the inductor and schottky diode. To protect the TPS61187, the device shuts down immediately. The device restarts after input POR or EN pin toggling.

7.4.7 Thermal Protection

When the junction temperature of the TPS61187 is over 150°C, the thermal protection circuit is triggered and shuts down the device immediately. Only a POR or EN pin toggling clears the protection and restarts the device.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS61187 provides a high-performance LED lighting solution for tablets, notebooks, monitors, and a variety of industrial designs. The device can drive 6 strings of 10 series LEDs in a compact and highly efficient solution. The TPS61187 provides a gate driver to an external P-channel MOSFET, which can be turned off during device shutdown or fault condition.

8.2 Typical Application

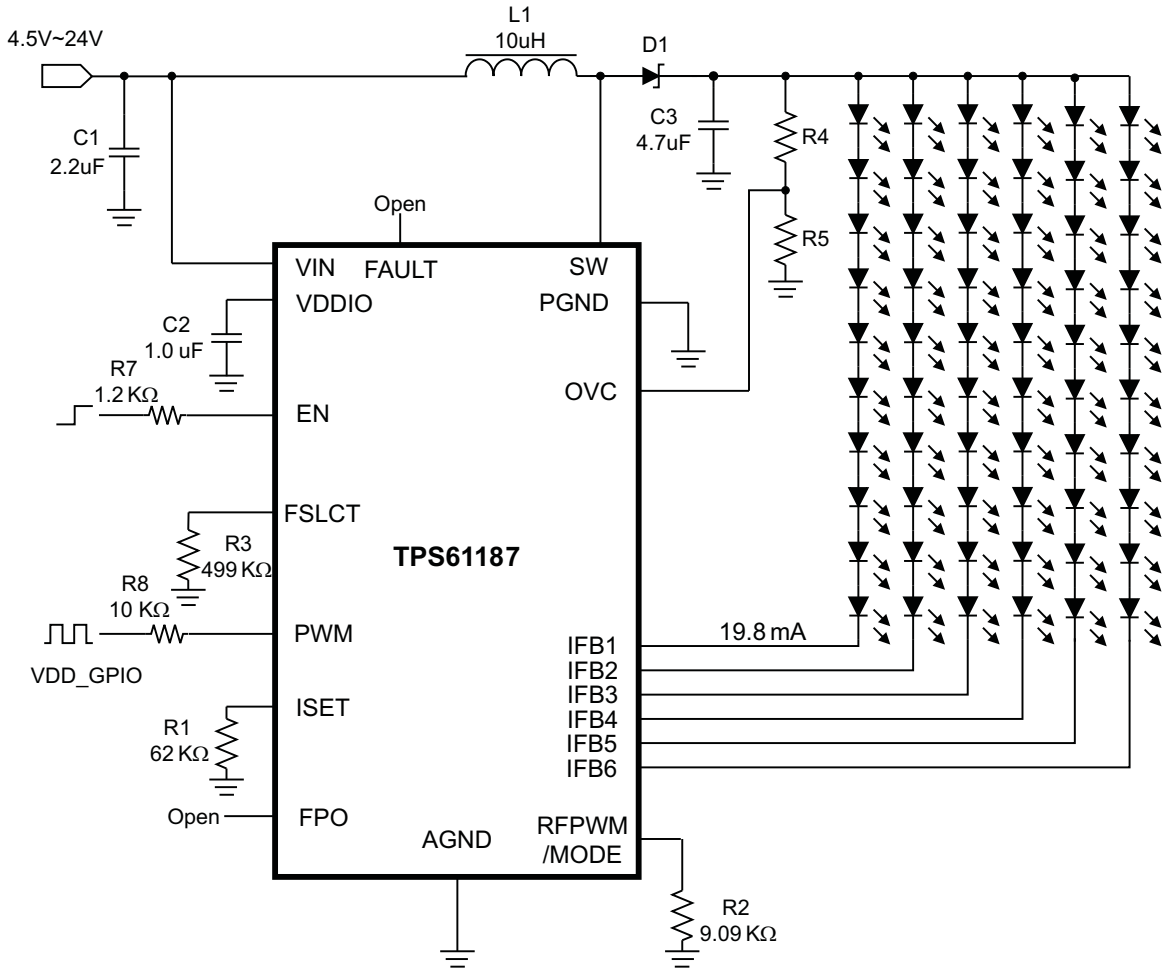


Figure 17. TPS61187 Typical Application

Typical Application (continued)

8.2.1 Design Requirements

For typical WLED-driver applications, use the parameters listed in Table 3.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	4 V to 24 V
Output voltage	38 V (maximum)
LED string current	30 mA (maximum)
Switching frequency	280 kHz to 1 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Inductor Selection

Because selection of the inductor affects power supply steady state operation, transient behavior, and loop stability, the inductor is the most important component in switching power regulator design. There are three specifications most important to the performance of the inductor: inductor value, DC resistance (DCR), and saturation current. The TPS61187 is designed to work with inductor values between 10 µH and 47 µH. A 10-µH inductor is typically available in a smaller or lower profile package, while a 47-µH inductor may produce higher efficiency due to a slower switching frequency and/or lower inductor ripple. If the boost output current is limited by the over-current protection of the device, using a 10-µH inductor and the highest switching frequency maximizes controller output current capability.

Internal loop compensation for PWM control is optimized for the external component values, including typical tolerances, recommended in Table 4. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0-A value depending on how the inductor vendor defines saturation. In a boost regulator, the inductor dc current can be calculated with Equation 6.

$$I_{DC} = \frac{Vout \times Iout}{Vin \times \eta} \quad (6)$$

where

- V_{OUT} = boost output voltage
- IOUT = boost output current
- VIN = boost input voltage
- η = power conversion efficiency, use 90% for TPS61187 applications

The inductor current peak-to-peak ripple can be calculated with Equation 7.

$$I_{PP} = \frac{1}{L \times \left(\frac{1}{Vout - Vin} + \frac{1}{Vin} \right) \times F_S} \quad (7)$$

where

- I_{PP} = inductor peak-to-peak ripple
- L = inductor value
- F_S = Switching frequency
- V_{OUT} = boost output voltage
- V_{IN} = boost input voltage

Therefore, the peak current seen by the inductor is calculated with Equation 8.

$$I_P = I_{DC} + \frac{I_{PP}}{2} \quad (8)$$

Select an inductor with a saturation current over the calculated peak current. To calculate the worst-case inductor peak current, use the minimum input voltage, maximum output voltage, and maximum load current.

Regulator efficiency is dependent on the resistance of its high current path and switching losses associated with the PWM switch and power diode. Although the TPS61187 device has optimized the internal switch resistances, the overall efficiency is affected by the inductor DCR. Lower DCR improves efficiency. However, there is a trade off between DCR and inductor footprint; furthermore, shielded inductors typically have higher DCR than unshielded ones. Table 4 lists the recommended inductors.

Table 4. Recommended Inductor For TPS61187

	L (µH)	DCR (mΩ)	I_{SAT} (A)	SIZE (L × W × H mm)
TOKO				
A915AY – 4R7M	4.7	38	1.87	5.2 × 5.2 × 3.0
A915AY – 100M	10	75	1.24	5.2 × 5.2 × 3.0
TDK				
SLF6028T – 4R7N1R6	4.7	38	1.87	5.2 × 5.2 × 3.0
SLF6028T – 4R7N1R6	10	75	1.24	5.2 × 5.2 × 3.0

8.2.2.2 Output Capacitor Selection

The output capacitor is mainly selected to meet the requirement for output ripple and loop stability. This ripple voltage is related to the capacitance of the capacitor and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated with Equation 9:

$$Cout = \frac{(Vout - Vin) \times Iout}{Vout \times F_S \times Vripple} \quad (9)$$

where

- Vripple = peak-to-peak output ripple

The additional part of the ripple caused by ESR is calculated using: $Vripple\_ESR = I_{OUT} \times RESR$

Due to its low ESR, Vripple_ESR can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used. The controller output voltage also ripples due to the load transient that occurs during PWM dimming. The TPS61187 adopts a patented technology to limit this type of output ripple even with the minimum recommended output capacitance. In a typical application, the output ripple is less than 250 mV during PWM dimming with a 4.7-µF output capacitor. However, the output ripple decreases with higher output capacitances.

8.2.2.3 Isolation FET Selection

The TPS61187 provides a gate driver to an external P-channel MOSFET, which can be turned off during device shutdown or fault condition. This MOSFET can provide a true shutdown function and also protect the battery from output short-circuit conditions. The source of the PMOS must be connected to the input, and a pullup resistor is required between the source and gate of the FET to keep the FET off during device shutdown. To turn on the isolation FET, the FAULT pin is pulled low and clamped at 8 V below the VBAT pin voltage. During device shutdown or fault condition, the isolation FET is turned off, and the input voltage is applied on the isolation MOSFET. During a short-circuit condition, the catch diode (D2 in the typical application circuit) is forward biased when the isolation FET is turned off. The drain of the isolation FET swings below ground. The voltage across the isolation FET can be momentarily greater than the input voltage. Therefore, select a 30-V PMOS for a 24-V maximum input. The on resistance of the FET has a large impact on power conversion efficiency since the FET carries the input voltage. Select a MOSFET with $R_{ds(on)}$ less than 100 mΩ to limit the power losses.

8.2.3 Application Curves

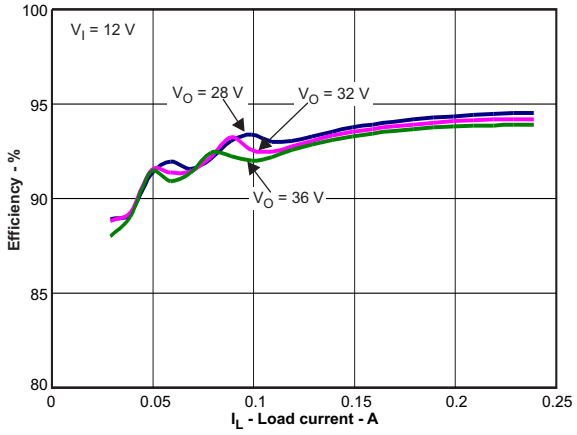


Figure 18. Efficiency

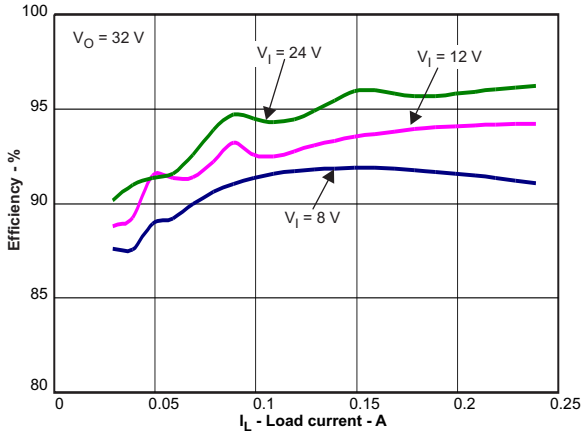


Figure 19. Efficiency

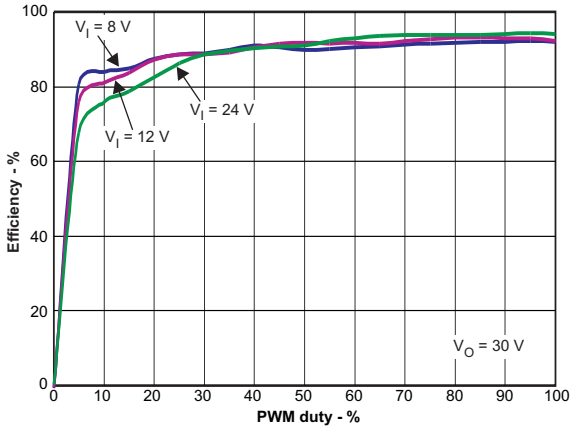


Figure 20. Efficiency

9 Power Supply Recommendations

The TPS61187 device requires a single-supply input voltage able to supply enough current for a given application. This voltage can range between 4.5 V to 24 V.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths. The input capacitor, C1 in *Typical Application – Phase Shift PWM Mode*, must not only be close to the VIN pin, but also to the GND pin in order to reduce the input ripple seen by the device. The input capacitor, C1 in *Typical Application – Phase Shift PWM Mode*, must also be placed close to the inductor. C2 is the filter and noise decoupling capacitor for the internal linear regulator powering the internal digital circuits; place C2 as close as possible between the VDDIO and AGND pins to prevent any noise insertion to the digital circuits. The SW pin carries high current with fast rising and falling edges. Therefore, the connection from the pin to the inductor and Schottky diode must be kept as short and wide as possible. It is also beneficial to have the ground of the output capacitor C3 close to the PGND pin because there is a large ground return current flowing between them. When laying out signal grounds, TI recommends using short traces separated from power ground traces and connecting them together at a single point, for example on the thermal pad. The thermal pad must be soldered on to the PCB and connected to the GND pin of the device. An additional thermal via can significantly improve power dissipation of the device.

10.2 Layout Example

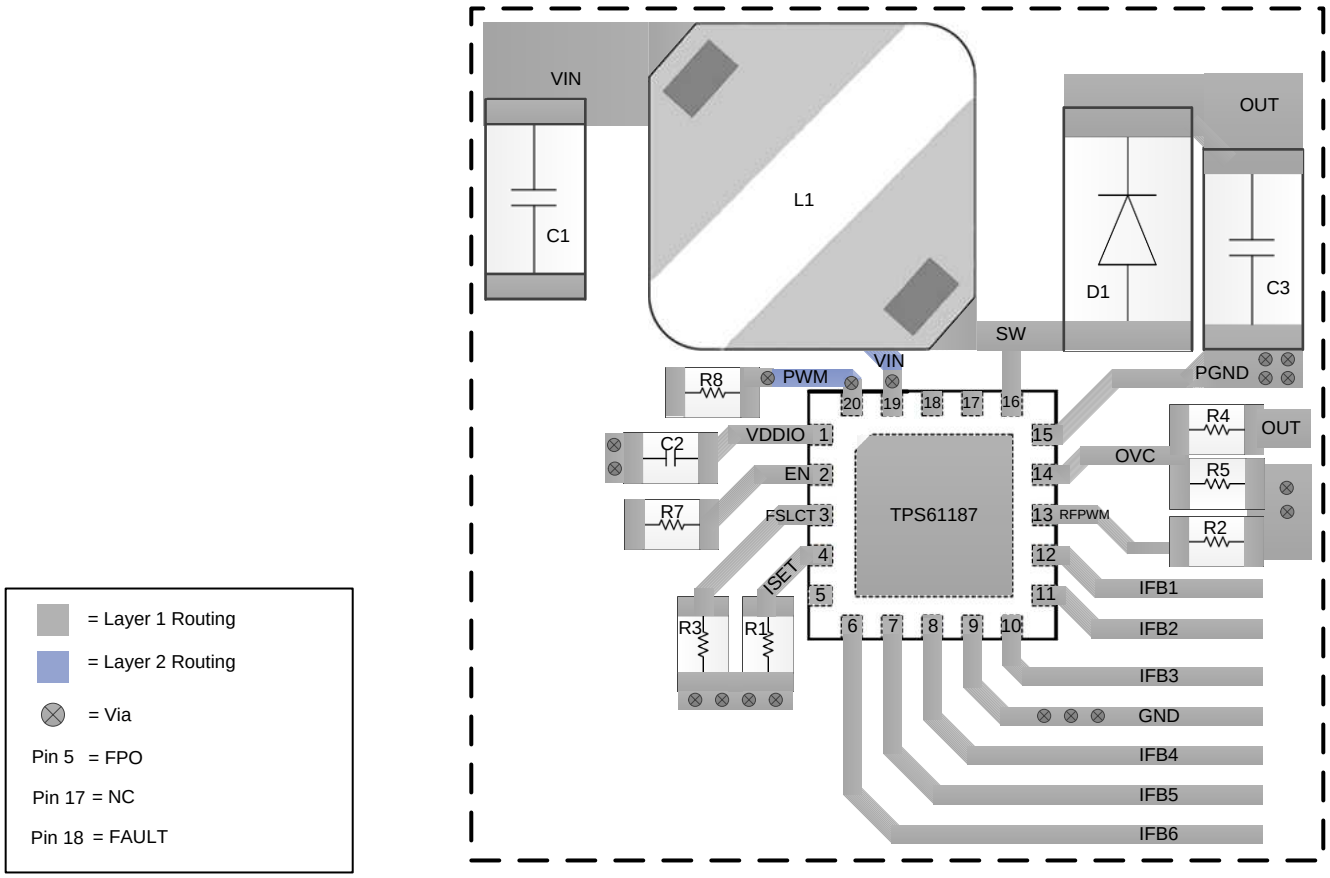


Figure 21. TPS61187 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61187RTJR	ACTIVE	QFN	RTJ	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 61187	Samples
TPS61187RTJT	ACTIVE	QFN	RTJ	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 61187	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

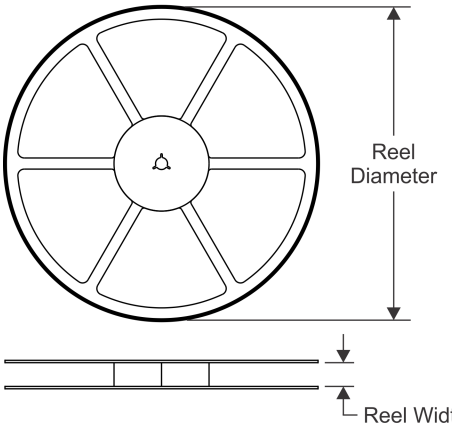
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

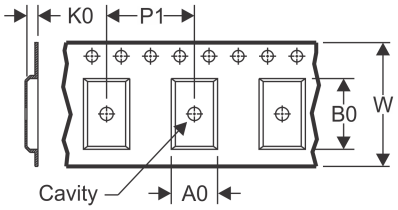
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

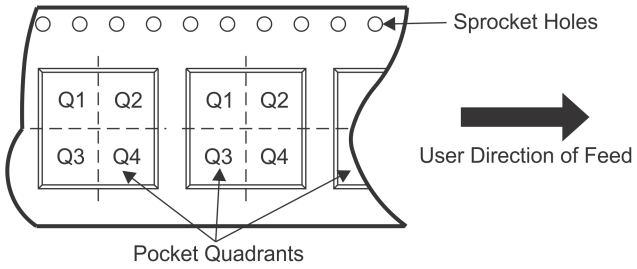


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

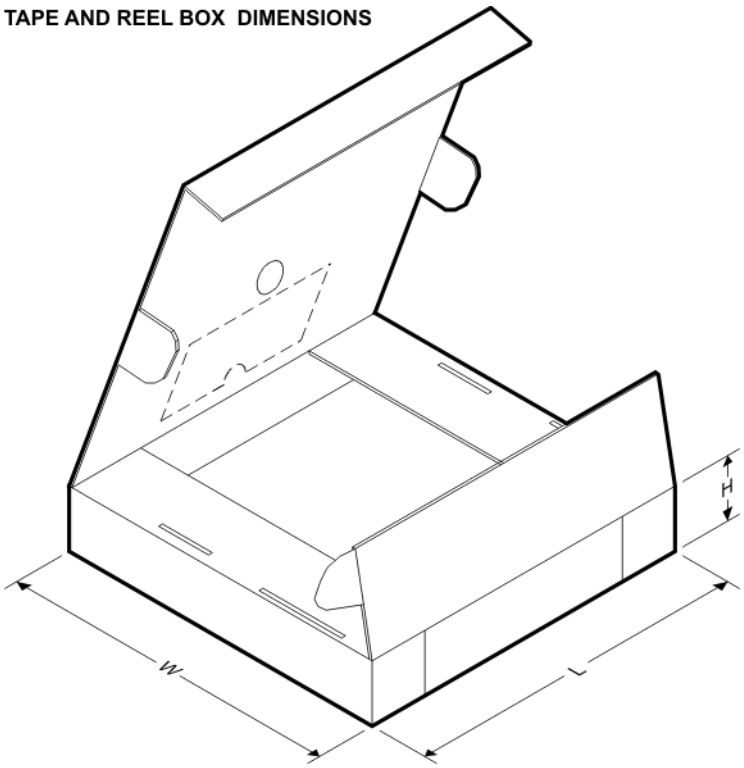
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61187RTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS61187RTJR	QFN	RTJ	20	3000	330.0	12.4	4.35	4.35	1.1	8.0	12.0	Q2
TPS61187RTJT	QFN	RTJ	20	250	180.0	12.5	4.35	4.35	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61187RTJR	QFN	RTJ	20	3000	853.0	449.0	35.0
TPS61187RTJR	QFN	RTJ	20	3000	205.0	200.0	33.0
TPS61187RTJT	QFN	RTJ	20	250	205.0	200.0	33.0

GENERIC PACKAGE VIEW

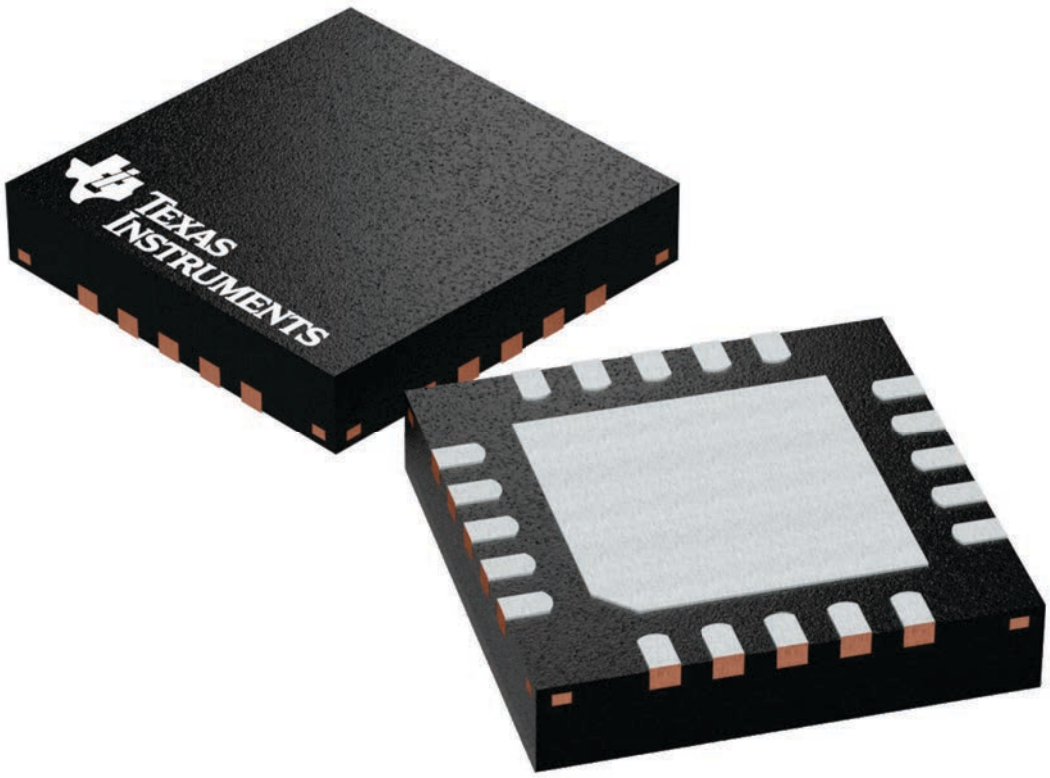
RTJ 20

WQFN - 0.8 mm max height

4 x 4, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224842/A

DATA BOOK
PACKAGE OUTLINE

LEADFRAME EXAMPLE
4222370

DRAFTSMAN: H. DENG	DATE: 09/12/2016		DIMENSIONS IN MILLIMETERS
DESIGNER: H. DENG	DATE: 09/12/2016	TEXAS INSTRUMENTS SEMICONDUCTOR OPERATIONS	CODE IDENTITY NUMBER 01295
CHECKER: V. PAKU & T. LEQUANG	DATE: 09/12/2016	ePOD, RTJ0020D / WQFN, 20 PIN, 0.5 MM PITCH	
ENGINEER: T. TANG	DATE: 09/12/2016		
APPROVED: E. REY & D. CHIN	DATE: 10/06/2016		
RELEASED: WDM	DATE: 10/24/2016		
TEMPLATE INFO: EDGE# 4218519	DATE: 04/07/2016		

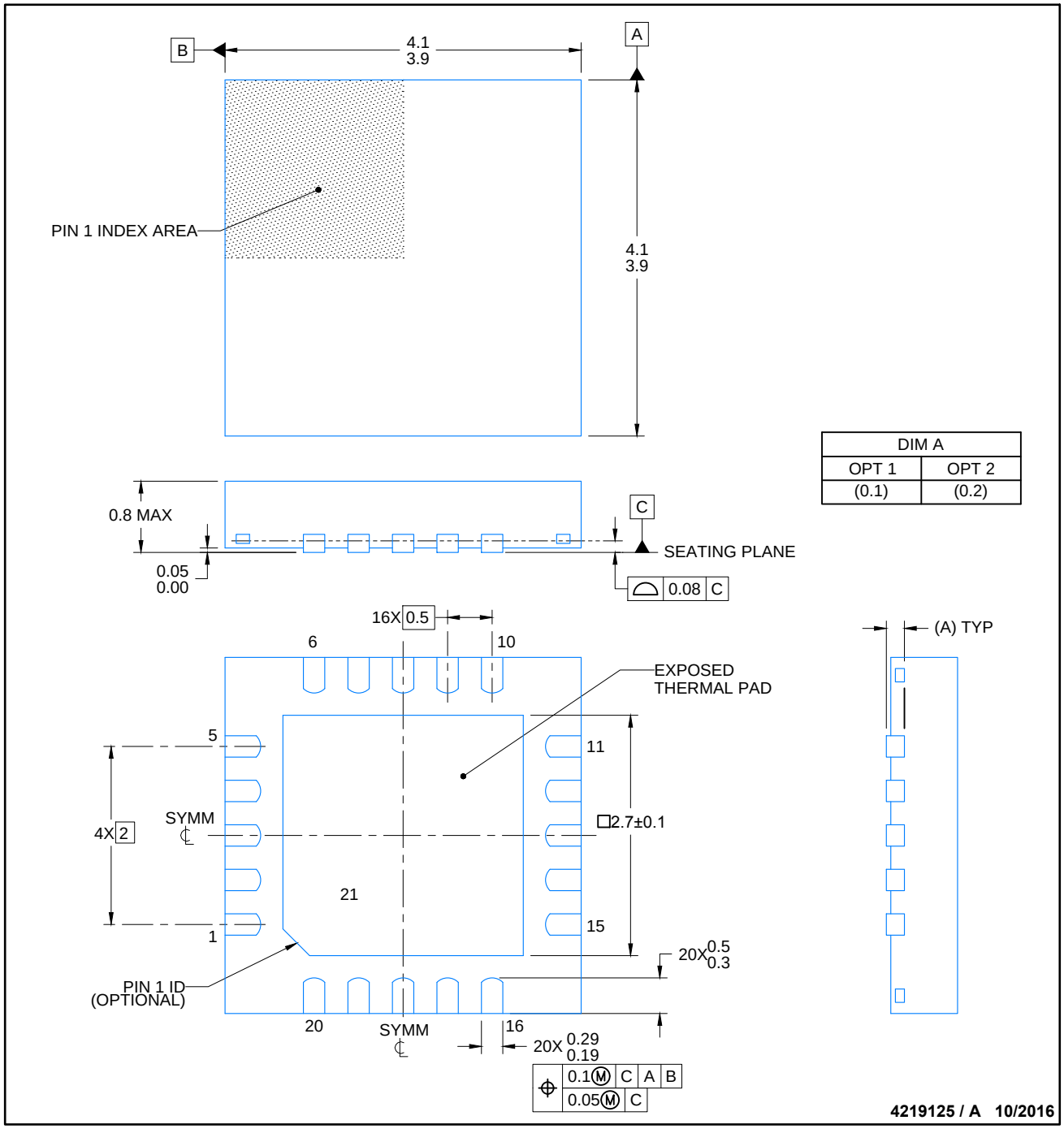
SCALE	SIZE		REV	PAGE
15X	A	4219125	A	1 OF 5

PACKAGE OUTLINE

RTJ0020D

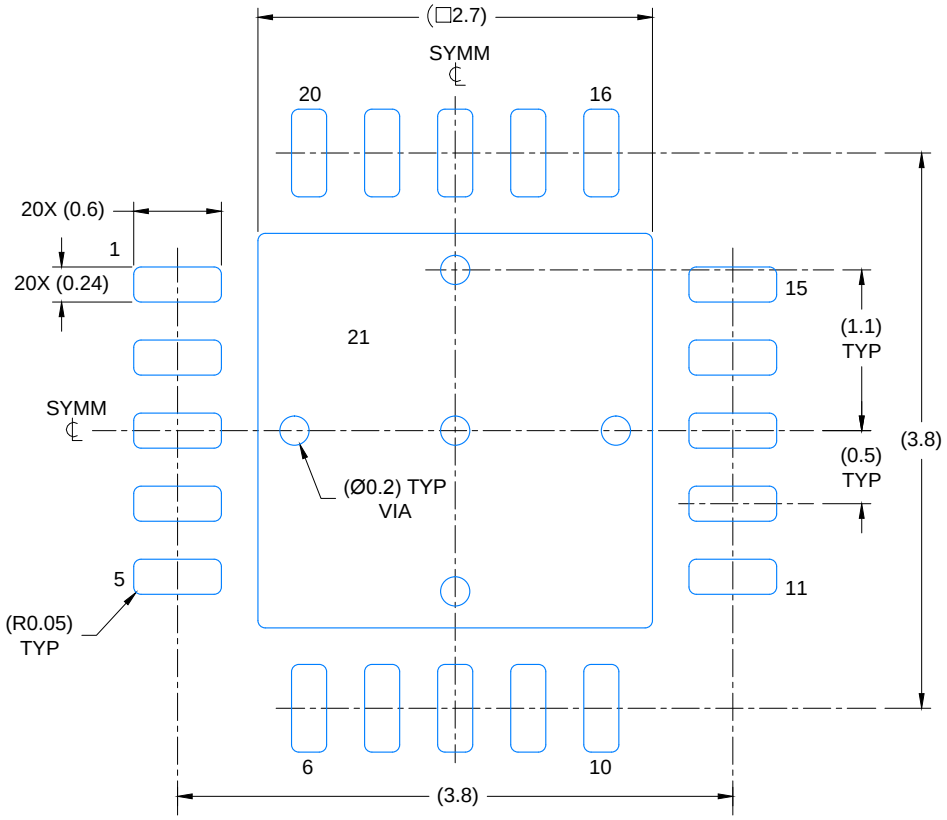
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



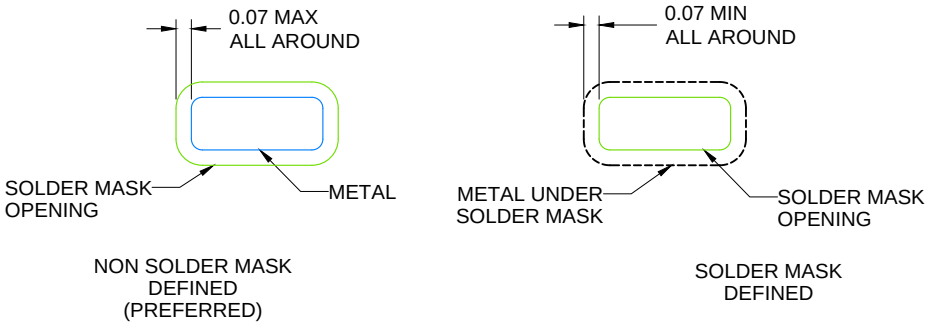
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X

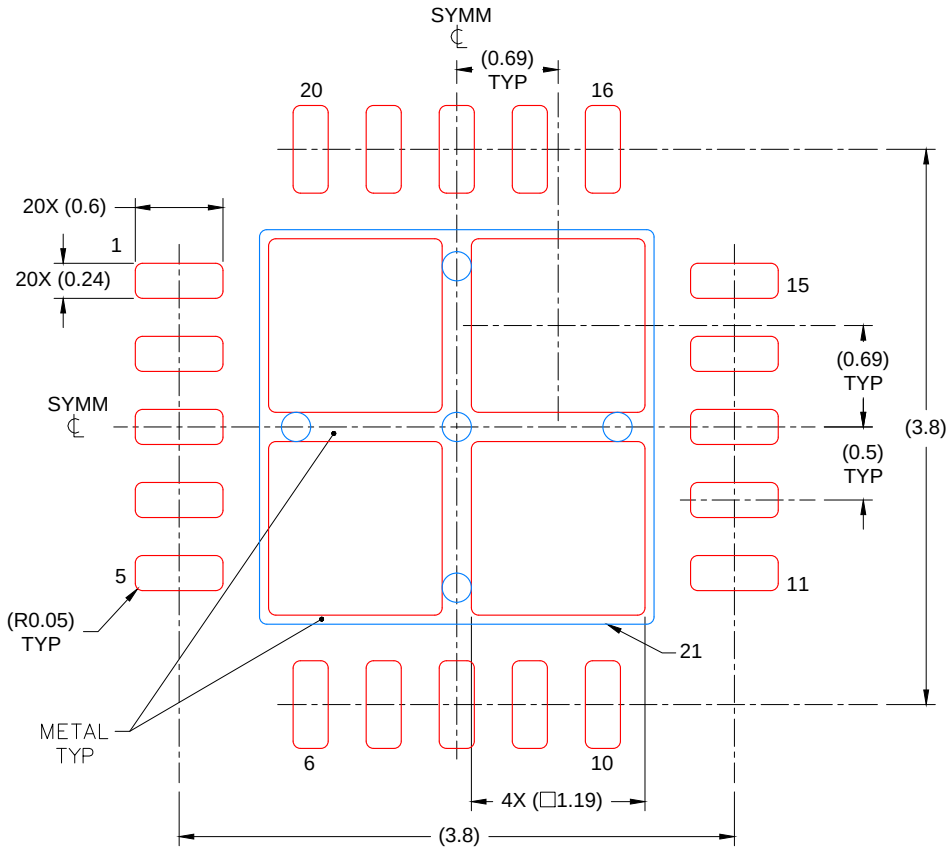


SOLDER MASK DETAILS

4219125 / A 10/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

4219125 / A 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTSMAN
A	RELEASE NEW DRAWING	2160736	10/24/2016	T. TANG / H. DENG

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