



# PIC16LF1566/1567

## 28/40/44-Pin 8-Bit Flash Microcontroller Product Brief

### Description

The PIC16LF1566/1567 microcontrollers deliver unique on-chip features for the design of mTouch® solutions and general purpose applications in 28/40/44-pin count packages. Two 10-bit high-speed ADCs with automated hardware CVD modules connect up to 34 analog channels to achieve a total sampling rate of 600k samples per second. This family provides mutual capacitance output drivers on all analog channels, two PWMs, two MSSP modules with low input-voltage options and one EUSART, which makes this family an excellent solution to implement low-power and noise-robust capacitive sensing and other front-end sampling applications with minimal software overhead.

### Core Features

- C Compiler Optimized RISC Architecture
- Only 49 Instructions
- Operating Speed:
  - 0-32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Up to Three 8-Bit Timers
- One 16-Bit Timer
- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Low-Power Brown-Out Reset (LPBOR)
- Programmable Watchdog Timer (WDT) up to 256s
- Programmable Code Protection

### Memory

- 8k Words Flash Program Memory
- 1024 Bytes Data SRAM Memory
- Direct, Indirect and Relative Addressing modes

### Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 3.6V
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

### eXtreme Low-Power (XLP) Features

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Operating Current:
  - 8 uA @ 32 kHz, 1.8V, typical
  - 32 uA/MHz @ 1.8V, typical

### Digital Peripherals

- PWM: Two 10-bit Pulse-Width Modulators
  - Output on up to five pins per PWM at the same time
- Dual Master Synchronous Serial Port (MSSP) with SPI and I<sup>2</sup>C:
  - 7-bit address masking
  - SMBus/PMBus™ compatibility
  - Configurable low input voltage threshold for I<sup>2</sup>C
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART):

- RS-232, RS-485, and LIN compatible
- Auto-Baud Detect
- Auto-wake-up on start
- Up to 35 I/O Pins and One Input Pin:
  - Individually programmable pull-ups
  - Interrupt-on-change with edge-select

### Intelligent Analog Peripherals

- Dual 10-Bit Analog-to-Digital Converter (ADC):
  - Up to 35 external channels
  - Conversion available during Sleep
  - Temperature indicator
  - Simultaneous sampling on two ADCs
  - Connect multiple channels together for sampling
    - External conversion trigger
    - Fixed Voltage Reference as a channel
    - External pin as positive ADC voltage reference
  - Combined 600k samples per second
- Hardware Capacitive Voltage Divider (CVD)
  - Double-sample conversions
  - Two sets of result registers
  - 7-bit precharge timer
  - 7-bit acquisition timer
  - Two guard ring output drives
  - Mutual capacitance TX output on any analog channel
    - 30 pF adjustable sample and hold capacitor
- Internal Voltage Reference Module

### Clocking Structure

- 16 MHz Internal Oscillator Block:
  - ±1% at calibration
  - Selectable frequency range from 0 to 32 MHz
- 31 kHz Low-Power Internal Oscillator
- External Oscillator Block with:
  - Two external clock modes up to 32 MHz
- Oscillator Start-up Timer (OST)

### Programming/Debug Features

- In-Circuit Debug Integrated On-Chip
- Emulation Header for Advanced Debug:
  - Provides trace, background debug and up to 32 hardware break points
- In-Circuit Serial Programming™ (ICSP™) via Two Pins

# PIC16LF1566/1567

## PIC16LF1566/1567 FAMILY TYPES

Device	Data Sheet Index	Program Memory Flash (words)	Data EEPROM (bytes)	SRAM (bytes)	I/Os <sup>(1)</sup>	10-bit ADCs <sup>(4)</sup>	Analog Channels <sup>(2)(3)</sup> CVD RX Channels	CVD TX Channels <sup>(6)</sup>	Timers 8/16-bit	EUSART	MSSP	PWM	Debug <sup>(6)</sup>
PIC12LF1552	(A)	2048	0	256	6	1	4	1	1 / 0	—	1	—	—
PIC16LF1554	(B)	4096	0	256	12	2	10	2	2 / 1	1	1	2	I
PIC16LF1559	(B)	8192	0	512	18	2	16	2	2 / 1	1	1	2	I
PIC16LF1566	(C)	8192	0	1024	25	2	23	23	3 / 1	1	2	2	I
PIC16LF1567	(C)	8192	0	1024	36	2	34	34	3 / 1	1	2	2	I

**Note 1:** The  $\overline{\text{MCLR}}$  pin is input-only.

**2:** Analog channels are split between the available ADCs.

**3:** Maximum usable analog channels assuming one pin must be assigned to output.

**4:** If  $V_{DD} > 2.4V$ , ADC may be overclocked 4x ( $T_{AD} = 0.25 \mu s$ ).

**5:** Includes functionality of ADxGRDA output pin.

**6:** Debugging Methods: (I) – Integrated on Chip.

**Data Sheet Index** (Unshaded devices are described in this document.)

**A:** DS40001674 [PIC12LF1552 Data Sheet, 8-Pin Flash, 8-Bit Microcontrollers](#)

**B:** DS40001761 [PIC16LF1554/1559 Data Sheet, 20-Pin Flash, 8-Bit Microcontrollers with XLP Technology](#)

**C:** Future Release [PIC16\(L\)F1556/1567 Data Sheet, 28/40/44-Pin, 8-bit Flash Microcontrollers](#)

**Note:** For other small form-factor package availability and marking information, please visit [www.microchip.com/packaging](http://www.microchip.com/packaging) or contact your local sales office.

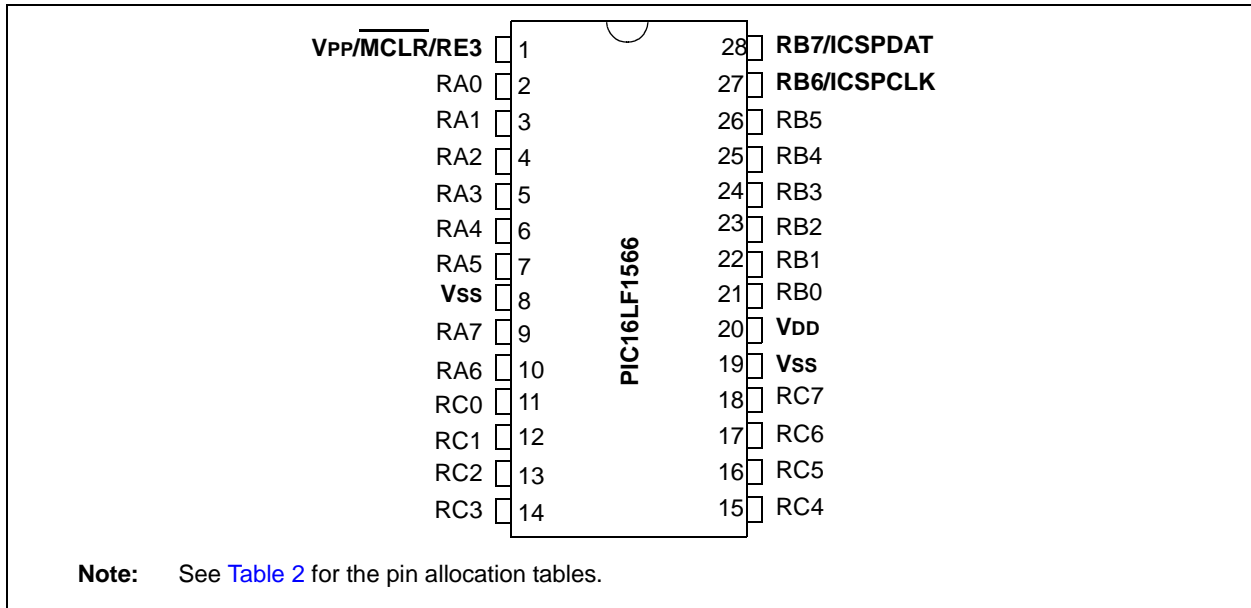
**TABLE 1: PACKAGES**

Device	SPDIP	SOIC	SSOP	UQFN (4x4x0.5)	PDIP	UQFN (5x5x0.5)	TQFP (10x10x1)
PIC16LF1566	X	X	X	X	—	—	—
PIC16LF1567	—	—	—	—	X	X	X

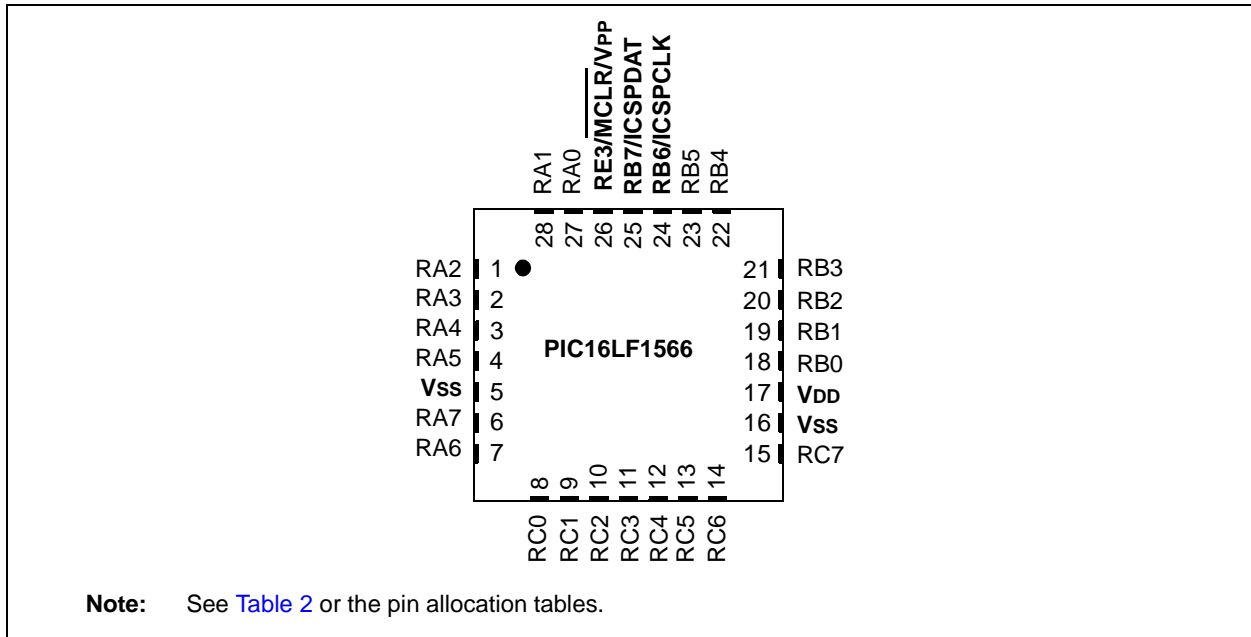
**Note:** Pin details are subject to change.

## PIN DIAGRAMS

**FIGURE 1: 28-PIN SPDIP, SOIC, SSOP DIAGRAM FOR PIC16LF1566**

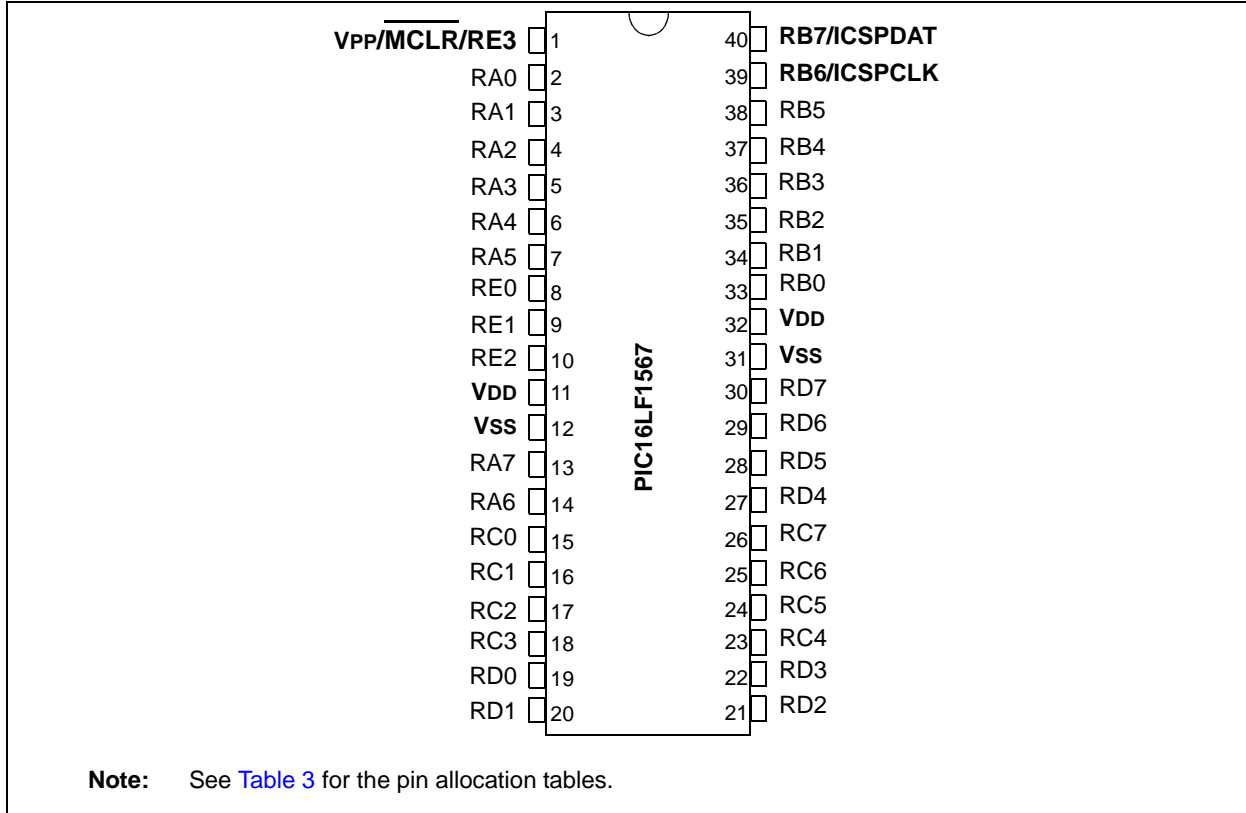


**FIGURE 2: 28-PIN UQFN DIAGRAM FOR PIC16LF1566**

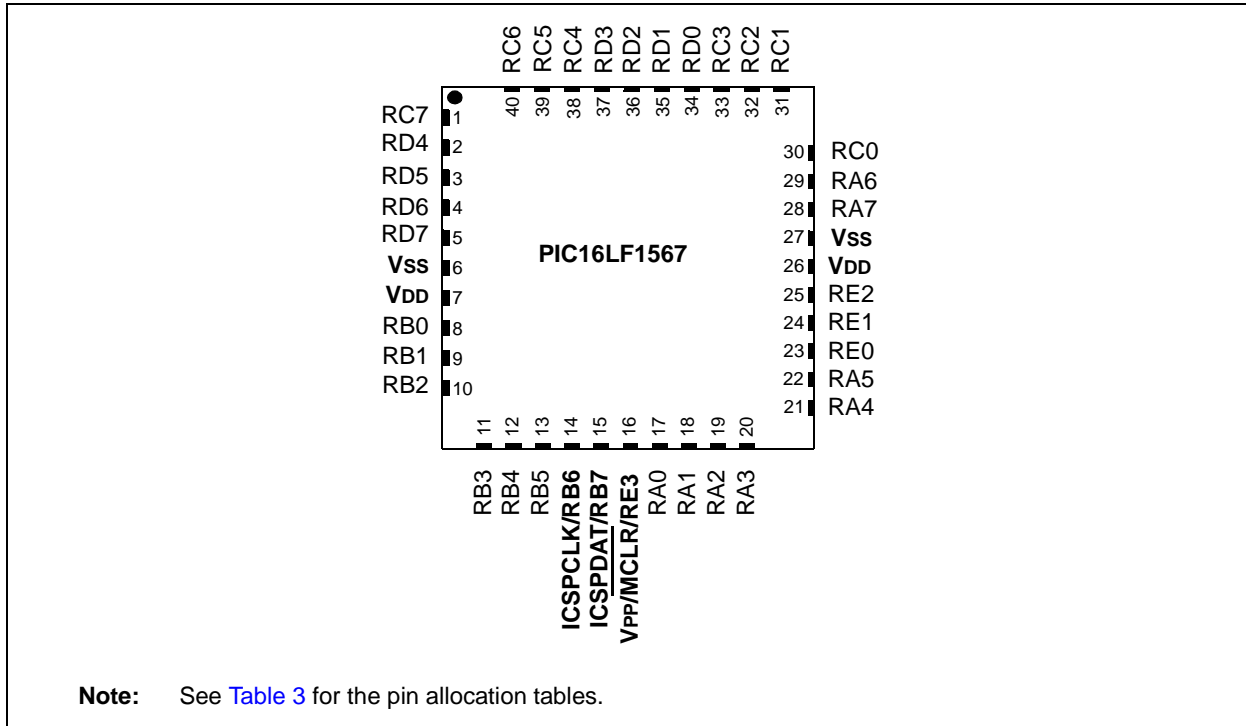


# PIC16LF1566/1567

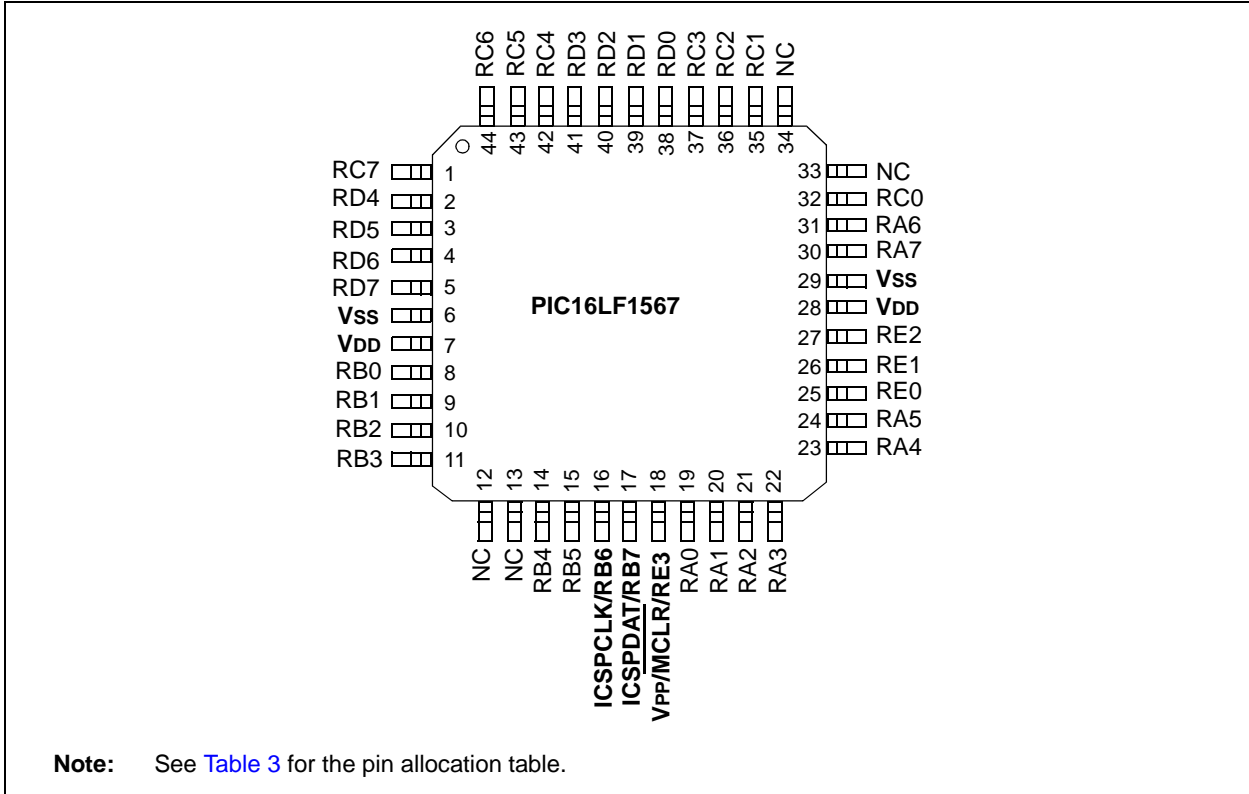
**FIGURE 3: 40-PIN PDIP DIAGRAM FOR PIC16LF1567**



**FIGURE 4: 40-PIN UQFN DIAGRAM FOR PIC16LF1567**



**FIGURE 5: 44-PIN TQFP DIAGRAM FOR PIC16LF1567**



# PIC16LF1566/1567

## PIN ALLOCATION TABLES

TABLE 2: 28-PIN ALLOCATION TABLE (PIC16LF1566)

I/O	28-Pin SPDIP/SOIC/SSOP	28-Pin UQFN	Analog Channel	ADC and CVD	Timers	PWM	EUSART	MSSP	Interrupt	Pull-up	Basic
RA0	2	27	AN20	—	—	PWM10	—	SS1 <sup>(1)</sup>	—	—	—
RA1	3	28	AN10	—	—	PWM11	—	SS2	—	—	—
RA2	4	1	AN0	—	—	PWM12	—	—	—	—	—
RA3	5	2	AN1	VREF+	—	PWM13	—	—	—	—	—
RA4	6	3	AN2	—	T0CKI	—	—	—	—	—	—
RA5	7	4	AN21	—	—	—	—	SS1 <sup>(1)</sup>	—	—	—
RA6	10	7	AN22	ADTRIG	—	—	—	—	—	—	CLKOUT
RA7	9	6	AN11	—	—	—	—	—	—	—	CLKIN
RB0	21	18	AN16	—	—	PWM20	—	—	INT IOC	Y	—
RB1	22	19	AN27	—	—	PWM21	—	—	IOC	Y	—
RB2	23	20	AN17	—	—	PWM22	—	—	IOC	Y	—
RB3	24	21	AN28	—	—	PWM23	—	—	IOC	Y	—
RB4	25	22	AN18	AD1GRDA <sup>(1)</sup> AD2GRDA <sup>(1)</sup>	—	—	—	—	IOC	Y	—
RB5	26	23	AN29	AD1GRDA <sup>(1)</sup> AD2GRDA <sup>(1)</sup>	T1G	—	—	—	IOC	Y	—
RB6	27	24	AN19	AD1GRDB <sup>(1)</sup> AD2GRDB <sup>(1)</sup>	—	—	—	—	IOC	Y	ICSPCLK ICDCLK
RB7	28	25	AN40	AD1GRDB <sup>(1)</sup> AD2GRDB <sup>(1)</sup>	—	—	—	—	IOC	Y	ICSPDAT ICDDAT
RC0	11	8	AN12	—	T1CKI	—	—	SDO2	—	—	—
RC1	12	9	AN23	—	—	PWM2	—	SCL2 SCK2	—	—	—
RC2	13	10	AN13	—	—	PWM1	—	SDA2 SDI2	—	—	—
RC3	14	11	AN24	—	—	—	—	SCL1 SCK1	—	—	—
RC4	15	12	AN14	—	—	—	—	SDA1 SDI1	—	—	—
RC5	16	13	AN25	—	—	—	—	SDO1 I2CLVL	—	—	—

**TABLE 2: 28-PIN ALLOCATION TABLE (PIC16LF1566) (CONTINUED)**

I/O	28-Pin SPDIP/SOIC/SSOP	28-Pin UQFN	Analog Channel	ADC and CVD	Timers	PWM	EUSART	MSSP	Interrupt	Pull-up	Basic
RC6	17	14	AN15	—	—	—	TX CK	—	—	—	—
RC7	18	15	AN26	—	—	—	RX DT	—	—	—	—
RE3	1	26	—	—	—	—	—	—	—	Y	$\overline{\text{MCLR}}$ V <sub>PP</sub>
VDD	20	17	—	—	—	—	—	—	—	—	VDD
VSS	8	5	—	—	—	—	—	—	—	—	VSS
VSS	19	16	—	—	—	—	—	—	—	—	VSS

**Note 1:** Pin functions can be assigned to one of two pin locations via software.

# PIC16LF1566/1567

**TABLE 3: 40/44-PIN ALLOCATION TABLE (PIC16LF1567)**

I/O	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	Analog Channel	ADC and CVD	Timers	PWM	EUSART	MSSP	Interrupt	Pull-Up	Basic
RA0	2	17	19	AN20	—	—	PWM10	—	SS1 <sup>(1)</sup>	—	—	—
RA1	3	18	20	AN10	—	—	PWM11	—	SS2	—	—	—
RA2	4	19	21	AN0	—	—	PWM12	—	—	—	—	—
RA3	5	20	22	AN1	VREF+	—	PWM13	—	—	—	—	—
RA4	6	21	23	AN2	—	TOCKI	—	—	—	—	—	—
RA5	7	22	24	AN21	—	—	—	—	SS1 <sup>(1)</sup>	—	—	—
RA6	14	29	31	AN22	ADTRIG	—	—	—	—	—	—	CLKOUT
RA7	13	28	30	AN11	—	—	—	—	—	—	—	CLKIN
RB0	33	8	8	AN16	—	—	PWM20	—	—	INT IOC	Y	—
RB1	34	9	9	AN27	—	—	PWM21	—	—	IOC	Y	—
RB2	35	10	10	AN17	—	—	PWM22	—	—	IOC	Y	—
RB3	36	11	11	AN28	—	—	PWM23	—	—	IOC	Y	—
RB4	37	12	14	AN18	AD1GRDA <sup>(1)</sup> AD2GRDA <sup>(1)</sup>	—	—	—	—	IOC	Y	—
RB5	38	13	15	AN29	AD1GRDA <sup>(1)</sup> AD2GRDA <sup>(1)</sup>	T1G	—	—	—	IOC	Y	—
RB6	39	14	16	AN19	AD1GRDB <sup>(1)</sup> AD2GRDB <sup>(1)</sup>	—	—	—	—	IOC	Y	ICSPCLK ICDCLK
RB7	40	15	17	AN40	AD1GRDB <sup>(1)</sup> AD2GRDB <sup>(1)</sup>	—	—	—	—	IOC	Y	ICSPDAT ICDDAT
RC0	15	30	32	AN12	—	T1CKI	—	—	SDO2	—	—	—
RC1	16	31	35	AN23	—	—	PWM2	—	SCL2 SCK2	—	—	—
RC2	17	32	36	AN13	—	—	PWM1	—	SDA2 SDI2	—	—	—
RC3	18	33	37	AN24	—	—	—	—	SCL1 SCK1	—	—	—
RC4	23	38	42	AN14	—	—	—	—	SDA1 SDI1	—	—	—
RC5	24	39	43	AN25	—	—	—	—	SDO1 I <sup>2</sup> CLVL	—	—	—
RC6	25	40	44	AN15	—	—	—	TX CK	—	—	—	—
RC7	26	1	1	AN26	—	—	—	RX DT	—	—	—	—
RD0	19	34	38	AN42	—	—	—	—	—	—	—	—



# PIC16LF1566/1567

**TABLE 3: 40/44-PIN ALLOCATION TABLE (PIC16LF1567) (CONTINUED)**

I/O	40-Pin PDIP	40-Pin UQFN	44-Pin TQFP	Analog Channel	ADC and CVD	Timers	PWM	EUSART	MSSP	Interrupt	Pull-Up	Basic
RD1	20	35	39	AN32	—	—	—	—	—	—	—	—
RD2	21	36	40	AN43	—	—	—	—	—	—	—	—
RD3	22	37	41	AN33	—	—	—	—	—	—	—	—
RD4	27	2	2	AN34	—	—	—	—	—	—	—	—
RD5	28	3	3	AN44	—	—	—	—	—	—	—	—
RD6	29	4	4	AN35	—	—	—	—	—	—	—	—
RD7	30	5	5	AN45	—	—	—	—	—	—	—	—
RE0	8	23	25	AN30	—	—	—	—	—	—	—	—
RE1	9	24	26	AN41	—	—	—	—	—	—	—	—
RE2	10	25	27	AN31	—	—	—	—	—	—	—	—
RE3	1	16	18	—	—	—	—	—	—	—	Y	MCLR VPP
VDD	11	7	7	—	—	—	—	—	—	—	—	VDD
VDD	32	26	28	—	—	—	—	—	—	—	—	VDD
VSS	12	6	6	—	—	—	—	—	—	—	—	VSS
VSS	31	27	29	—	—	—	—	—	—	—	—	VSS

**Note 1:** Pin functions can be assigned to one of two pin locations via software.

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