# MPQ8634B

**16V, 20A, Sync, Step-Down Converter with Adjustable Current Limit, Programmable Frequency, and Voltage Tracking**

The Future of Analog IC Technology

## DESCRIPTION

The MPQ8634B is a fully integrated, high-frequency, synchronous, buck converter. The MPQ8634B offers a very compact solution that achieves up to 20A output current with excellent load and line regulation over a wide input supply range. The MPQ8634B operates at high efficiency over a wide output current load range.

The MPQ8634B adopts an internally compensated constant-on-time (COT) control mode that provides fast transient response and eases loop stabilization.

The operating frequency can be set to 600kHz, 800kHz, or 1000kHz easily with MODE configuration, allowing the MPQ8634B's frequency to remain constant regardless of the input/output voltages.

The output voltage start-up ramp is controlled by an internal 1.5ms timer. It can be increased by adding a capacitor on TRK/REF. An open-drain power good (PGOOD) signal indicates when the output is within its nominal voltage range. PGOOD is clamped at around 0.7V with an external pull-up voltage when the input supply fails to power the MPQ8634B.

Fully integrated protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP).

The MPQ8634B requires a minimal number of readily available, standard, external components and is available in a QFN-21 (3mmx4mm) package.

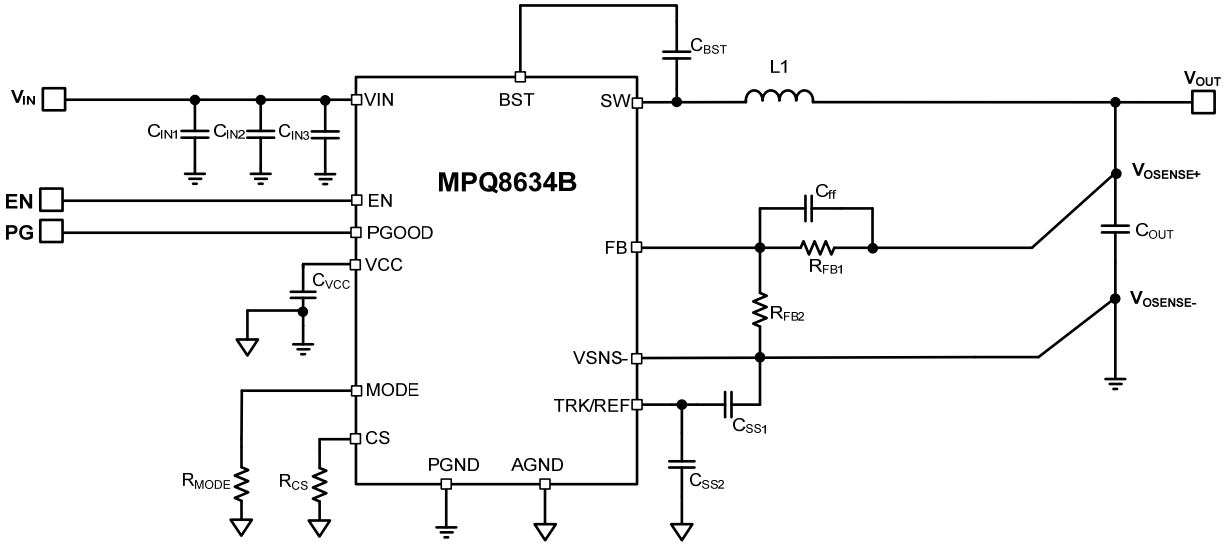
## FEATURES

- Wide Input Voltage Range:
  - 2.85V to 16V with External 3.3V VCC Bias
  - 4V to 16V with Internal VCC Bias or External 3.3V VCC Bias
- Differential Output Voltage Remote Sense
- Programmable Accurate Current Limit Level
- 20A Output Current
- Low $R_{DS(ON)}$ Integrated Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- Adaptive COT for Ultrafast Transient Response
- Stable with Zero ESR Output Capacitor
- 0.5% Reference Voltage over 0°C to +70°C Junction Temperature Range
- 1% Reference Voltage from -40°C to +125°C Junction Temperature Range
- Selectable Pulse-Skip Mode or Forced CCM Operation
- Excellent Load Regulation
- Output Voltage Tracking
- Output Voltage Discharge
- PGOOD Actively Clamped at a Low Level during Power Failure
- Programmable Soft-Start Time from 1.5ms
- Pre-Bias Start-Up
- Selectable Switching Frequency from 600kHz, 800kHz, and 1000kHz
- Non-Latch OCP, UVP, UVLO, Thermal Shutdown, and Latch-Off for OVP
- Output Adjustable from 0.9V to 90%*VIN, up to 6V Max
- Available in a QFN-21 (3mmx4mm) Package

## APPLICATIONS

- Telecom and Networking Systems
- Servers, Cloud-Computing, Storage
- Base Stations
- General Purpose Point-of-Load (PoL)
- 12V Distribution Power Systems
- High-end TV
- Game Consoles and Graphic Cards

## TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number | Package | Top Marking |
|---|---|---|
| MPQ8634BGLE* | QFN-21 (3mmx4mm) | *See Below* |

* For Tape & Reel, add suffix –Z (e.g. MPQ8634BGLE–Z)

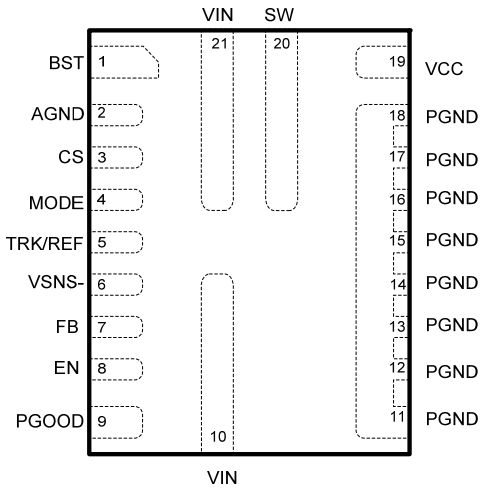
## TOP MARKING

MPYW
8634
BLLL
E

MP: MPS prefix
Y: Year code
W: Week code
8634B: First five digits of the part number
LLL: Lot number
E: MPQ8634BGLE

## PACKAGE REFERENCE

**TOP VIEW**




**QFN-21 (3mmx4mm)**

## ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (VIN) ..... 18V
$V_{SW}$ (DC) ..... -0.3V to VIN + 0.3V
$V_{SW}$ (25 ns) (2) ..... -3V to 25V
$V_{SW}$ (25ns) ..... -5V to 25V
$V_{BST}$ ..... $V_{SW}$ + 4V
VCC, EN ..... 4.5V
All other pins ..... -0.3 V to 4.3V
Junction temperature ..... 170°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +170°C

### *Recommended Operating Conditions* (3)

Supply voltage (VIN) ..... 4V to 16V
$V_{IN(DC)}$ - $V_{SW(DC)}$ (4) ..... -0.3V to VIN + 0.3V
$V_{SW(DC)}$ (4) ..... -0.3V to VIN + 0.3V
Output voltage ($V_{OUT}$) ..... 0.9V to 6V
External VCC bias ($V_{CC\_EXT}$) ..... 3.12V to 3.6V
Maximum output current ($I_{OUT\_MAX}$) ..... 20A
Maximum output current limit ($I_{OC\_MAX}$) ..... 24A
Maximum peak inductor current ($I_{L\_PEAK}$) ..... 28A
EN voltage ($V_{EN}$) ..... 3.6V
Operating junction temp. ($T_J$) .... -40°C to +125°C

### *Thermal Resistance* (5)

| | $\theta_{JB}$ | $\theta_{JC\_TOP}$ | |
|---|---|---|---|
| QFN-21 (3mmx4mm) ..... | 8 ..... | 18 ..... | °C/W |

**NOTES:**

1) Exceeding these ratings may damage the device.
2) Measured by using differential oscilloscope probe.
3) The device is not guaranteed to function outside of its operating conditions.
4) The voltage rating can be in the range of -3V to 23V for a period of 25ns or less with a maximum repetition rate of 1000kHz when the input voltage is 16V.
5) $\theta_{JB}$: Thermal resistance from the junction to the board around the PGND soldering point.
   $\theta_{JC\_TOP}$: Thermal resistance from the junction to the top of the package.

## ELECTRICAL CHARACTERISTICS

**VIN = 12 V, $T_J$ = -40°C to +125°C, unless otherwise noted.**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Supply Current** | | | | | | |
| Supply current (shutdown) | $I_{IN}$ | $V_{EN}$ = 0V | | 0 | 10 | μA |
| Supply current (quiescent) | $I_{IN}$ | $V_{EN}$ = 2V, $V_{FB}$ = 1V | | 650 | 850 | μA |
| **MOSFET** | | | | | | |
| Switch leakage | $SW_{LKG\_HS}$ | $V_{EN}$ = 0V, $V_{SW}$ = 0V | | 0 | 10 | μA |
| | $SW_{LKG\_LS}$ | $V_{EN}$ = 0V, $V_{SW}$ = 12V | | 0 | 30 | |
| HS on-state resistance | $R_{DS\_ON\_HS}$ | $V_{EN}$ = 2V @ 25°C | | 8.6 | | mΩ |
| LS on-state resistance | $R_{DS\_ON\_LS}$ | $V_{EN}$ = 2V @ 25°C | | 2.5 | | mΩ |
| **Current Limit** | | | | | | |
| Current limit threshold | $V_{LIM}$ | | 1.15 | 1.2 | 1.25 | V |
| $I_{CS}$ to $I_{OUT}$ ratio | $I_{CS}/I_{OUT}$ | $I_{OUT}$ ≥ 2A | 9 | 10 | 11 | μA/A |
| Low-side negative current limit | $I_{LIM\_NEG}$ | | | -10 | | A |
| Negative current limit timeout (6) | $t_{NCL\_Timer}$ | | | 200 | | ns |
| **Switching Frequency** | | | | | | |
| Switching frequency (7) | $f_{SW}$ | MODE = GND, $I_{OUT}$ = 0A, $V_{OUT}$ = 1V | 480 | 600 | 720 | kHZ |
| | | MODE = 30.1kΩ, $I_{OUT}$ = 0A, $V_{OUT}$ = 1V | 680 | 800 | 920 | kHZ |
| | | MODE = 60.4kΩ, $I_{OUT}$ = 0A, $V_{OUT}$ = 1V | 850 | 1000 | 1150 | kHZ |
| Minimum on time (6) | $T_{ON\_MIN}$ | | | | 50 | ns |
| Minimum off time (6) | $T_{OFF\_MIN}$ | $V_{FB}$ = 800mV | | | 180 | ns |
| **Over-Voltage (OVP) and Under-Voltage Protection (UVP)** | | | | | | |
| OVP threshold | $V_{OVP}$ | | 113% | 116% | 119% | $V_{REF}$ |
| UVP threshold | $V_{UVP}$ | | 77% | 80% | 83% | $V_{REF}$ |
| **Feedback Voltage and Soft Start (SS)** | | | | | | |
| Feedback voltage | $V_{REF}$ | $T_J$ = -40°C to +125°C | 891 | 900 | 909 | mV |
| | | $T_J$ = 0°C to +70°C | 895 | 900 | 905 | mV |
| TRK/REF sourcing current | $I_{TRACK\_Source}$ | $V_{TRK/REF}$ = 0V | | 42 | | μA |
| TRK/REF sinking current | $I_{TRACK\_Sink}$ | $V_{TRK/REF}$ = 1V | | 12 | | μA |
| Soft-start time | $t_{SS}$ | $C_{TRACK}$ = 1nF | 1 | 1.5 | | ms |
| **Error Amplifier (EA)** | | | | | | |
| Error amplifier offset | $V_{OS}$ | | -3 | 0 | 3 | mV |
| Feedback current | $I_{FB}$ | $V_{FB}$ = REF | | 50 | 100 | nA |
| **Enable AND UVLO** | | | | | | |
| Enable input rising threshold | $VIH_{EN}$ | | 1.17 | 1.22 | 1.27 | V |
| Enable hysteresis | $V_{EN\text{-}HYS}$ | | | 200 | | mV |
| Enable input current | $I_{EN}$ | $V_{EN}$ = 2V | | 0 | | μA |
| Soft shutdown discharge MOSFET | $R_{ON\_DISCH}$ | | | 80 | 150 | Ω |

## ELECTRICAL CHARACTERISTICS *(continued)*

**VIN = 12V, $T_J$ = -40°C to +125°C, unless otherwise noted.**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **VIN UVLO** | | | | | | |
| VIN under-voltage lockout threshold rising | $VIN_{VTH\_RISE}$ | VCC = 3.3V | 2.1 | 2.4 | 2.7 | V |
| VIN under-voltage lockout threshold falling | $VIN_{VTH\_FALL}$ | | 1.55 | 1.85 | 2.15 | |
| **VCC Regulator** | | | | | | |
| VCC under-voltage lockout threshold rising | $VCC_{VTH\_RISE}$ | | 2.65 | 2.8 | 2.95 | V |
| VCC under-voltage lockout threshold falling | $VCC_{VTH\_FALL}$ | | 2.35 | 2.5 | 2.65 | |
| VCC regulator | $V_{CC}$ | | 2.88 | 3.00 | 3.12 | V |
| VCC load regulation | | $I_{CC}$ = 25 mA | | 0.5 | | % |
| **Power Good (PGOOD)** | | | | | | |
| Power good high threshold | $PG_{Vth\_Hi\_Rise}$ | FB from low to high | 89% | 92.5% | 95% | $V_{REF}$ |
| | | | | | | |
| Power good low threshold | $PG_{Vth\_Lo\_Rise}$ | FB from low to high | 113% | 116% | 119% | $V_{REF}$ |
| | $PG_{Vth\_Lo\_Fall}$ | FB from high to low | 77% | 80% | 83% | $V_{REF}$ |
| Power good low to high delay | $PG_{Td}$ | $T_J$ = 25°C | 0.63 | 0.9 | 1.17 | ms |
| Power good sink current capability | $V_{PG}$ | $I_{PG}$ = 10mA | | | 0.5 | V |
| Power good leakage current | $I_{PG\_LEAK}$ | $V_{PG}$ = 3.3V | | | 3 | µA |
| Power good low-level output voltage | $V_{OL\_100}$ | VIN = 0V, pull PGOOD up to 3.3V through a 100kΩ resistor @ 25°C | | 650 | 800 | mV |
| | $V_{OL\_10}$ | VIN = 0V, pull PGOOD up to 3.3V through a 10kΩ resistor @ 25°C | | 750 | 900 | mV |
| **Thermal Protection** | | | | | | |
| Thermal shutdown (6) | $T_{SD}$ | | 150 | 160 | | °C |

**NOTES:**

6) Guaranteed by design.

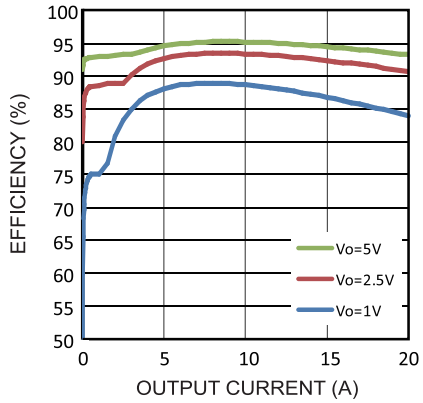
7) Guaranteed by design over temperature.

## TYPICAL PERFORMANCE CHARACTERISTICS

**VIN = 12V, $T_A$ = 25˚C, $V_{OUT}$ = 1V, $F_S$ = 800kHz unless otherwise noted.**

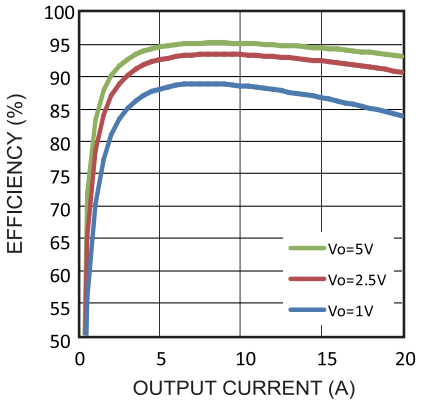
### Efficiency

Pulse Skip, 0.4µH, 800kHz



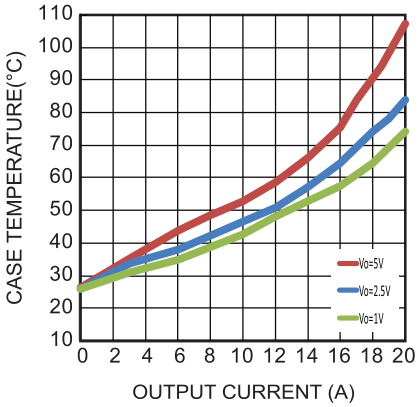

### Efficiency

Forced CCM, 0.4µH, 800kHz



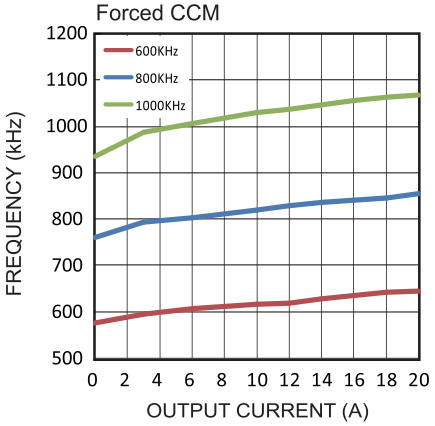

### Thermal Results

800kHz, No Air-Flow

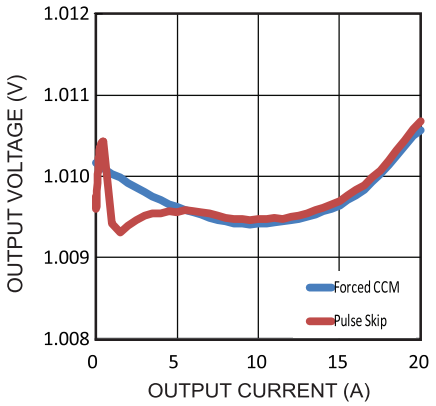



### Switching Frequency vs. Output Current

Forced CCM

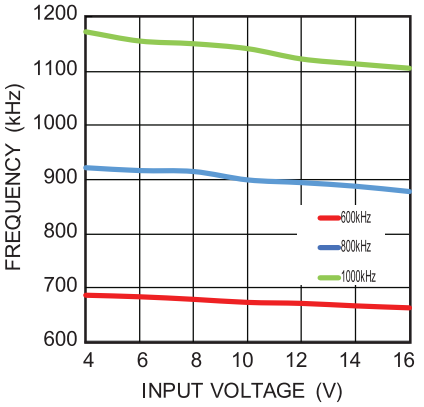



### Output Voltage Load Regulation



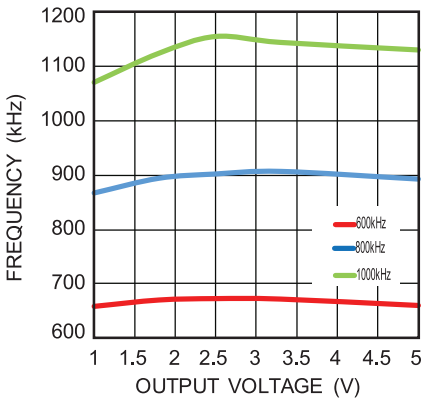

### Switching Frequency vs. Input Voltage

$V_{OUT}$=1V, 3A Load




### Switching Frequency vs. Output Voltage

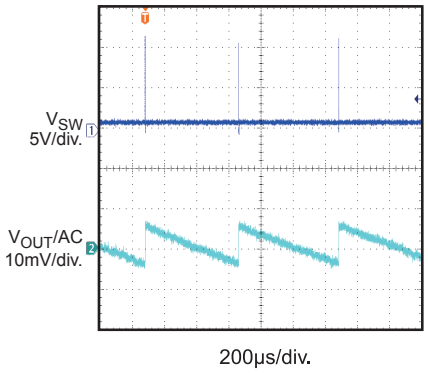
$V_{OUT}$=12V, 3A Load



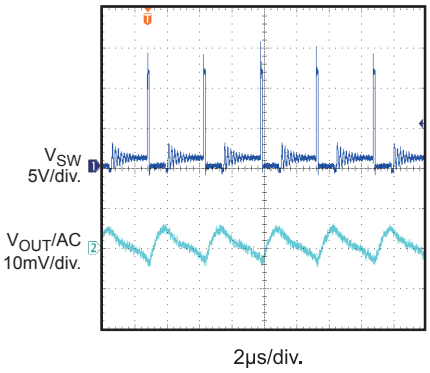
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**VIN = 12V, $T_A$ = 25˚C, $V_{OUT}$ = 1V, $F_S$ = 800kHz unless otherwise noted.**

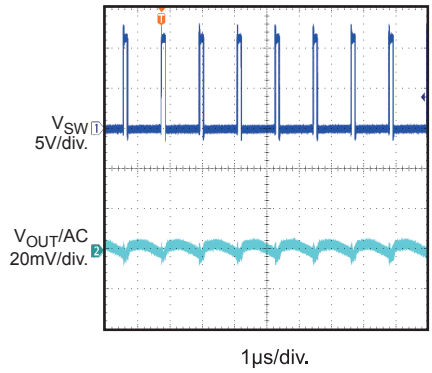
### Steady State
$I_{OUT}$ = 0A, Pulse Skip



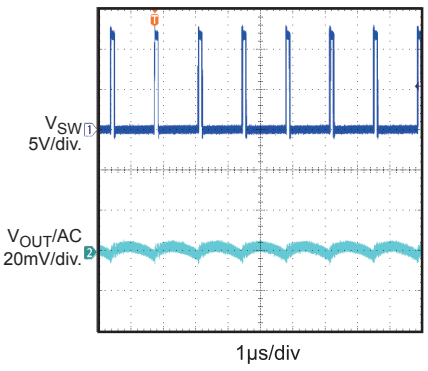

### Steady State
$I_{OUT}$ = 0.5A, Pulse Skip



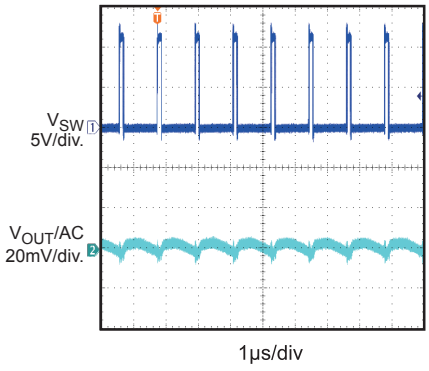

### Steady State
$I_{OUT}$ = 20A, Pulse Skip



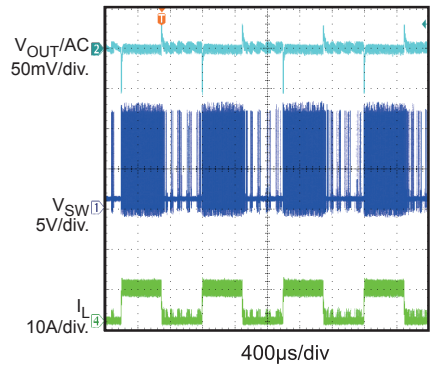

### Steady State
$I_{OUT}$ = 0A, Forced CCM



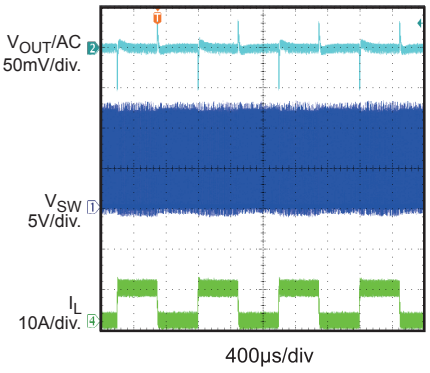

### Steady State
$I_{OUT}$ = 20A, Forced CCM



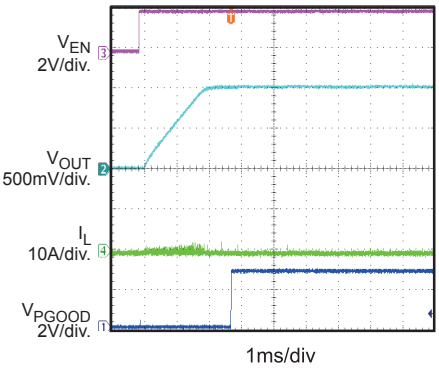

### Load Transient
$I_{OUT}$ =0A~8A, Pulse Skip



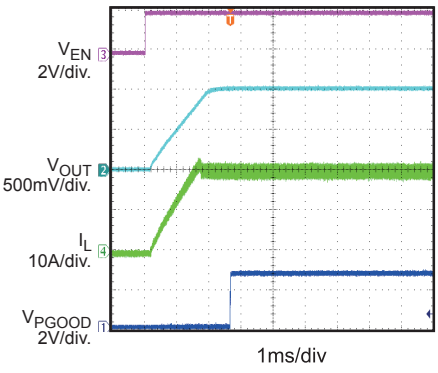

### Load Transient
$I_{OUT}$=0A~8A, Forced CCM




### Power Up through EN
$I_{OUT}$ = 0A, Pulse Skip



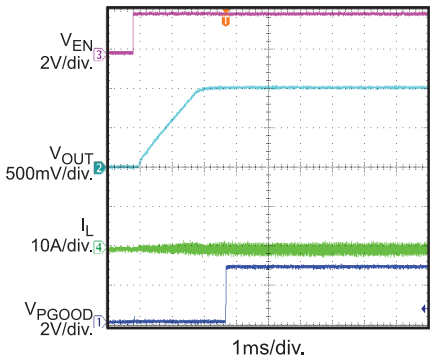

### Power Up through EN
$I_{OUT}$ = 20A, Pulse Skip



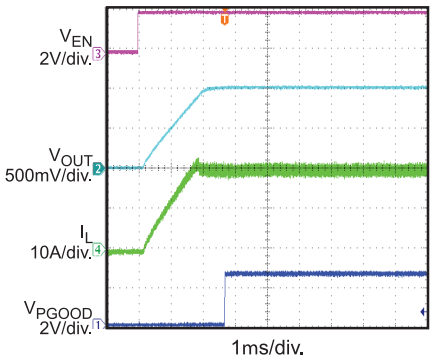
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**VIN = 12V, $T_A$ = 25˚C, $V_{OUT}$ = 1V, $F_S$ = 800kHz unless otherwise noted.**

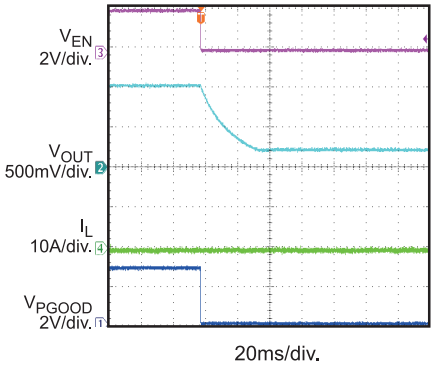
### Power Up through EN
$I_{OUT}$ = 0A, Forced CCM



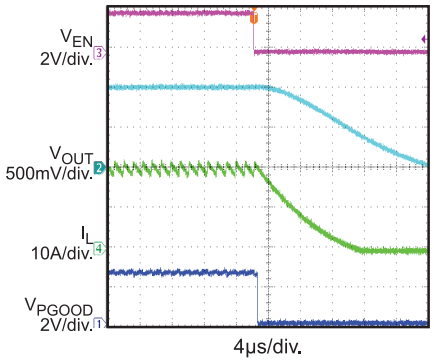

### Power Up through EN
$I_{OUT}$ = 20A, Forced CCM



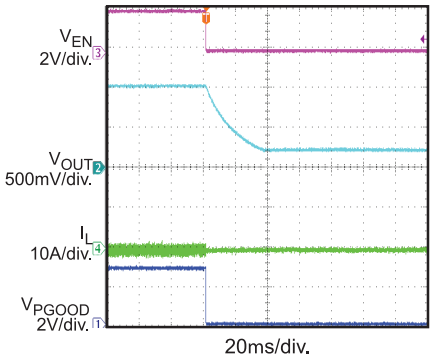

### Power Down through EN
$I_{OUT}$=0A, Pulse Skip



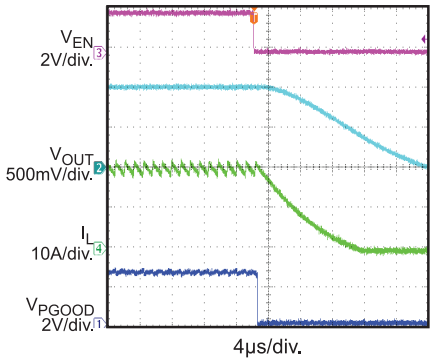

### Power Down through EN
$I_{OUT}$ = 20A, Pulse Skip



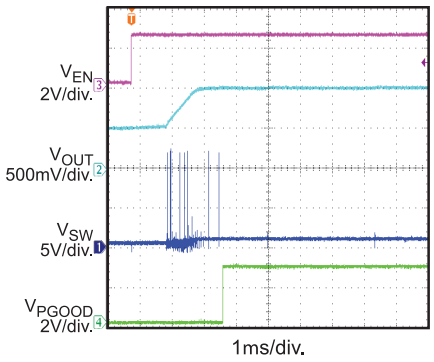

### Power Down through EN
$I_{OUT}$ = 0A, Forced CCM



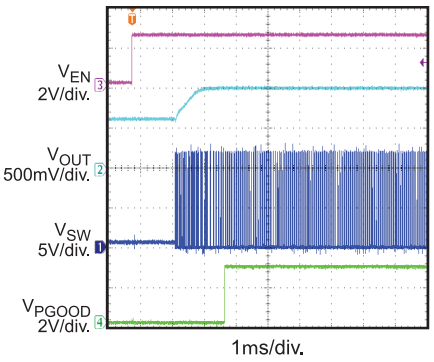

### Power Down through EN
$I_{OUT}$ = 20A, Forced CCM



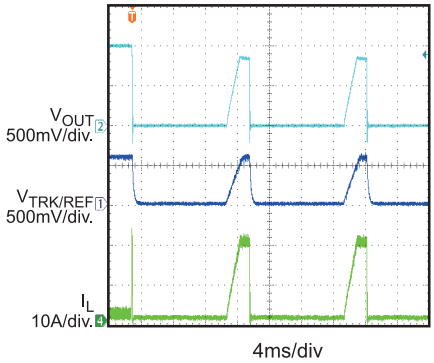

### Pre-Bias Start-Up
Pulse Skip




### Pre-Bias Start-Up
Forced CCM



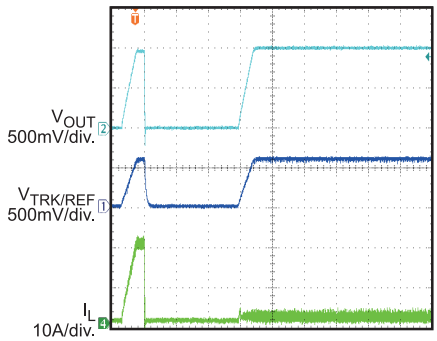

### Over-Current
Protection Entry



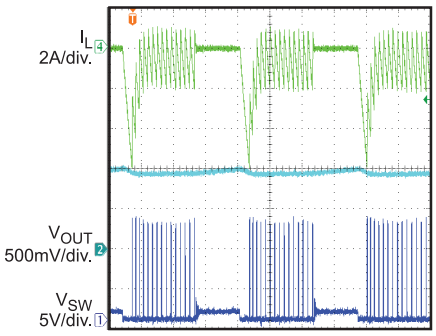
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**Performance waveforms are tested on the evaluation board.**

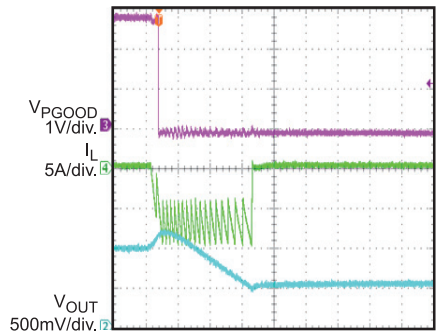
### Over-Current
Protection Recovery



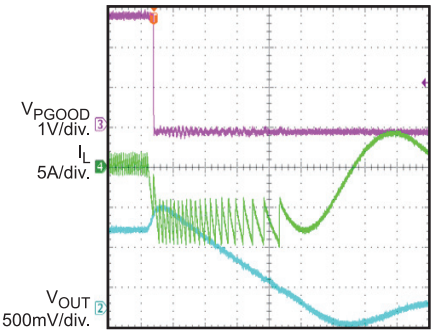

### OSM Operation
Pulse Skip Mode




### Over-Voltage Protection
Pulse Skip Mode




### Over-Voltage Protection
Forced CCM



## PIN FUNCTIONS

| PIN # | Name | Description |
|---|---|---|
| 1 | BST | **Bootstrap.** Connect a capacitor between SW and BS to form a floating supply across the high-side switch driver. |
| 2 | AGND | **Analog ground.** Select AGND as the control circuit reference point. |
| 3 | CS | **Current limit.** Connect a resistor to ground to set the current limit trip point. See Equation 4 for additional details. |
| 4 | MODE | **Operation mode selection.** Program MODE to select continuous conduction mode (CCM), pulse-skip mode, and the operating switching frequency (See Table 1 for additional details.). |
| 5 | TRK/REF | **External tracking voltage input.** The output voltage tracks this input signal. Decouple TRK/REF with a ceramic capacitor as close to TRK/REF as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics. The capacitance of this capacitor determines the soft-start time (See Equation 2 and 3 for additional details.). |
| 6 | VSNS- | **Differential remote sense negative input.** Connect VSNS- to the negative side of the voltage sense point directly. Short VSNS- to AGND if the remote sense is not being used. |
| 7 | FB | **Feedback (differential remote sense positive input).** An external resistor divider from the output to VSNS- tapped to FB sets the output voltage. Place the resistor divider as close to FB as possible. Vias should be avoided on the FB traces. |
| 8 | EN | **Enable.** EN is an input signal that turns the regulator on or off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. Connect EN to VIN through a pull-up resistor or a resistive voltage divider for automatic start-up. Do not float EN. |
| 9 | PGOOD | **Power good output.** PGOOD is an open-drain signal. A pull-up resistor connected to a DC voltage is required to indicate high if the output voltage is within regulation. There is ~1ms of delay from FB ≥ 92.5% to when PGOOD is asserted. |
| 10, 21 | VIN | **Input voltage.** VIN supplies power for the internal MOSFET and regulator. Input capacitors are needed to decouple the input rail. Make the connection using wide PCB traces. |
| 11-18 | PGND | **System ground.** PGND is the reference ground of the regulated output voltage and requires careful consideration during PCB layout. Make the connection using wide PCB traces. |
| 19 | VCC | **Internal 3V LDO output.** The driver and control circuits are powered from VCC. Decouple VCC with a minimum 1μF ceramic capacitor as close to VCC as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics. |
| 20 | SW | **Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is driven up to VIN by the high-side switch during the on-time of the PWM duty cycle. The inductor current drives SW low during the off-time. Make the connection using wide PCB traces. |

## BLOCK DIAGRAM

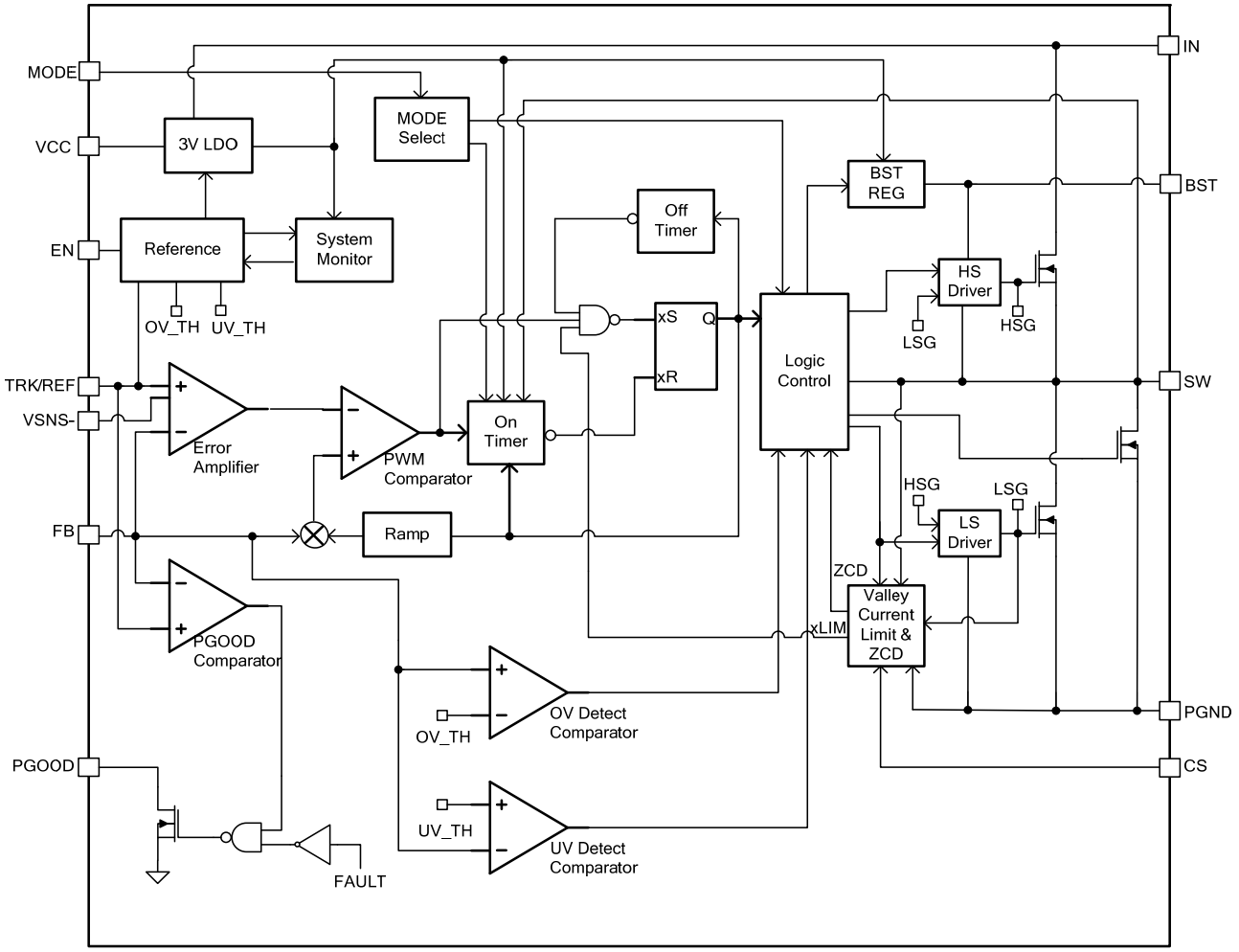



**Figure 1: Functional Block Diagram**

# OPERATION

## Constant-On-Time (COT) Control

The MPQ8634B employs constant-on-time (COT) control to achieve a fast load transient response (see Figure 2).

The operational amplifier (AMP) corrects any error voltage between FB and the reference voltage ($V_{REF}$). The MPQ8634B can use AMP to provide excellent load regulation over the entire load range, no matter it the device is operating in forced continuous conduction mode (CCM) or pulse-skip mode.

The dedicated VSNS- pin helps provide differential output voltage remote sense. The pair of the remote sense trace should be kept at a low impedance to achieve the best performance.

The MPQ8634B has an internal ramp compensation that supports a low ESR MLCC output capacitor solution. The adaptive internal ramp is optimized so that the MPQ8634B is stable in the entire operating input/output voltage range with the proper design of the output L/C filter.

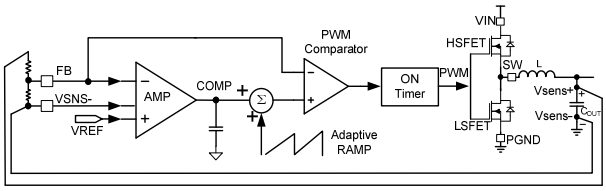



**Figure 2: COT Control**

## Pulse-Width Modulation (PWM) Operation

Figure 3 shows how the pulse-width modulation (PWM) is generated. AMP corrects any error between FB and REF and generates a fairly smooth DC voltage (COMP). The internal ramp is superimposed onto COMP, which is compared with the FB signal. Whenever FB drops below the superimposed COMP, the integrated high-side MOSFET (HS-FET) is turned on. The HS-FET keeps on for a fixed turn-on time. The fixed on time is determined by the input voltage, output voltage, and selected switching frequency. After the on period elapses, the HS-FET turns off and turns on again when FB drops below the superimposed COMP. By repeating this operation, the MPQ8634B regulates the output voltage.

The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize conduction loss. A dead short occurs between VIN and PGND if both the HS-FET and the LS-FET are turned on at the same time. This is called a shoot-through. To prevent shoot-through, a dead time (DT) is generated internally between the HS-FET off and the LS-FET on period or the LS-FET off and the HS-FET on period.

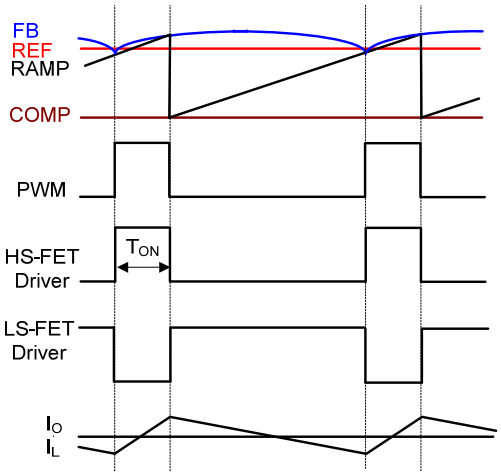



**Figure 3: Heavy-Load Operation (PWM)**

## Continuous Conduction Mode (CCM)

Continuous conduction mode (CCM) occurs when the output current is high and the inductor current is always above zero amps (see Figure 2). The MPQ8634B can also be configured to operate in forced CCM operation when the output current is low (See the MODE Selection section on page 14 for details).

In CCM operation, the switching frequency is fairly constant (PWM mode), and the output ripple remains almost the same throughout the entire load range.

## Pulse-Skip Operation

In light-load condition, the MPQ8634B can be configured to work in pulse-skip mode to optimize efficiency. When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the part transitions from CCM to pulse-skip mode if the MPQ8634B is configured so (see the MODE Selection section on page 14 for details).

Figure 4 shows pulse-skip mode operation in light-load condition. When FB drops below the superimposed COMP, the HS-FET turns on for a fixed interval. When the HS-FET turns off, the LS-FET turns on until the inductor current reaches zero. In pulse-skip mode operation, FB does not reach the superimposed COMP when the inductor current approaches zero. The LS-FET driver turns into tri-state (Hi-Z) when the inductor current reaches zero. A current modulator takes over the control of the LS-FET and limits the inductor current to less than -1 mA. The output capacitors discharge slowly to PGND through the LS-FET. In light-load condition, the HS-FET is not turned on as frequently in pulse-skip mode as it is in forced CCM. As a result, the efficiency in pulse-skip mode is improved greatly compared with that in forced CCM operation.

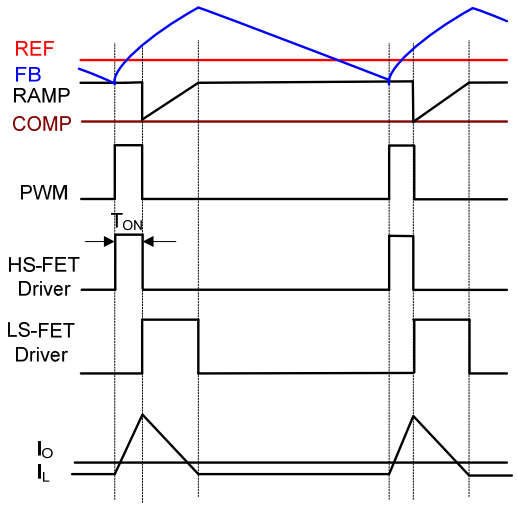



**Figure 4: Pulse Skip at Light Load**

As the output current increases from the light-load condition, the current modulator regulation time period becomes shorter. The HS-FET is turned on more frequently and the switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current is determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

Where $F_{SW}$ is the switching frequency.

The part enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

The MPQ8634B can be configured to operate in forced CCM, even if in a light-load condition (see Table 1).

## MODE Selection

The MPQ8634B provides both forced CCM operation and pulse-skip mode operation in a light-load condition. The MPQ8634B has three options for switching frequency selection: 600kHz, 800kHz, and 1000kHz. Select the operation mode under light-load condition and the switching frequency by choosing the resistance value of the resistor connected between MODE and AGND or VCC (see Table 1).

**Table 1: MODE Selection**

| MODE | Light-Load Mode | Switching Frequency |
|---|---|---|
| VCC | Pulse skip | 600kHz |
| 243kΩ (±20%) to AGND | Pulse skip | 800kHz |
| 121kΩ (±20%) to AGND | Pulse skip | 1000kHz |
| GND | Forced CCM | 600kHz |
| 30.1kΩ (±20%) to AGND | Forced CCM | 800kHz |
| 60.4kΩ (±20%) to AGND | Forced CCM | 1000kHz |

### Soft Start (SS)

The minimum soft-start time is limited at 1ms. This time can be increased by adding a SS capacitor between TRK/REF and VSNS-.

The total SS capacitor value can be determined with Equation (2) and Equation (3):

$$C_{REF}(nF) = \frac{t_{SS}(ms) \times 36(\mu A)}{0.9(V)} \quad (2)$$

$$C_{SS} = C_{SS1} + C_{SS2} \quad (3)$$

Where $C_{SS2}$ is recommended to be minimum of 22nF.

### Output Voltage Tracking and Reference

The MPQ8634B provides an analog input pin (TRK/REF) to track another power supply or accept an external reference. When an external voltage signal is connected to TRK/REF, it acts as a reference for the MPQ8634B output voltage. The FB voltage ($V_{FB}$) follows this external voltage signal exactly. The soft-start settings are ignored. The TRK/REF input signal can be in the range of 0.3V to 1.4V. During the initial start-up, TRK/REF must be at least 900mV to ensure proper operation. Afterward, it can be any value between 0.3V and 1.4V.

### Pre-Bias Start-Up

The MPQ8634B has been designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the IC disables switching for both the HS-FET and LS-FET until the voltage on the TRK/REF capacitor exceeds the sensed output voltage at FB. Before the TRK/REF voltage reaches the pre-biased FB level, if the BST voltage (from BST to SW) is lower than 2.3V, the LS-FET is turned on to allow the BST voltage to be charged through VCC. The LS-FET is turned on for very narrow pulses, so the drop in pre-biased level is negligible.

### Output Voltage Discharge

When the MPQ8634B is disabled through EN, it enables the output voltage discharge mode. This causes both the HS-FET and the LS-FET to latch off. A discharge MOSFET connected between SW and PGND is turned on to discharge the output voltage. The typical switch on resistance of this MOSFET is about 80Ω. Once $V_{FB}$ drops below 10%*REF, the discharge MOSFET is turned off.

### Current Sense and Over-Current Protection (OCP)

The MPQ8634B features an on-die current sense and a programmable positive current limit threshold. The current limit is active when the MPQ8634B is enabled. During the LS-FET on state, the SW current (inductor current) is sensed and mirrored to CS with the ratio of $G_{CS}$. By using a resistor ($R_{CS}$) from CS to AGND, the CS voltage ($V_{CS}$) is proportional to the SW current cycle-by-cycle.

The HS-FET is only allowed to turn on when $V_{CS}$ is below the internal over-current protection (OCP) voltage threshold ($V_{OCP}$) (during the LS-FET on state) to limit the SW valley current cycle-by-cycle.

Calculate the current limit threshold setting from $R_{CS}$ with Equation (4):

$$R_{CS}(\Omega) = \frac{V_{OCP}}{G_{CS} \times (I_{LIM} - \frac{(V_{IN} - V_O) \times V_O}{V_{IN}} \times \frac{1}{2 \times L \times f_s})} \quad (4)$$

Where $V_{OCP}$ is 1.2V, $G_{CS}$ is 10 μA/A, and $I_{LIM}$ is the desired output current limit (A).

After SS finishes, the MPQ8634A latches off if it detects an over-current condition for 31 consecutive cycles, or if the FB drops below the under-voltage protection (UVP) threshold. The MPQ8634B is enabled by recycling the power of VCC or EN.

### Negative Inductor Current Limit

When the LS-FET detects a -10A current, the part turns off the LS-FET for 200ns to limit the negative current. After 200ns, the LS-FET is turned on again.

### Output Sinking Mode (OSM)

The MPQ8634B employs output sinking mode (OSM) to regulate the output voltage to the targeted value. When $V_{FB}$ is higher than 105%*REF but is lower than the OVP threshold, OSM is triggered. During OSM operation, the LS-FET remains on until it reaches the -7.5A negative current limit. The LS-FET is momentarily turned off for 200ns and is then turned on again. The MPQ8634B maintains this operation until $V_{FB}$ drops below 102%*REF. Then the MPQ8634B exits OSM after 15 consecutive cycles of forced CCM.

### Over-Voltage Protection (OVP)

The MPQ8634B monitors the output voltage by connecting FB to the tap of the output voltage feedback resistor divider to detect an over-voltage condition. This provides latch-off over-voltage protection (OVP) mode.

If $V_{FB}$ exceeds 116% of $V_{REF}$, the device enters latch-off OVP mode. The HS-FET latches off and PGOOD latches low until the power of VCC or EN is recycled. Meanwhile, the LS-FET remains on until it reaches the low-side negative current limit (NOCP). Once it hits NOCP, the LS-FET is momentarily turned off for 200ns and is then turned on again. The MPQ8634B maintains this operation to bring down the output voltage. When $V_{FB}$ drops below 50% of $V_{REF}$, the LS-FET is turned off for pulse-skip mode and keeps turning on for forced CCM operation. If $V_{FB}$ rises back to more than 116% of $V_{REF}$, the LS-FET turns on again with NOCP until $V_{FB}$ drops back below 50% of $V_{REF}$. The power of EN or VIN must be recycled to clear the OVP fault.

The OVP function is enabled after TRK/REF reaches 900mV.

### Over-Temperature Protection (OTP)

The MPQ8634B has an over-temperature protection (OTP). The IC monitors the junction temperature internally. If the junction temperature exceeds the threshold value (typically 160°C ), the converter shuts off. This is a latch-off protection. Enable the part by recycling the power of VCC or EN.

The OTP function is effective once the MPQ8634B is enabled.

### Output Voltage Setting and Remote Output Voltage Sensing

First choose a value for R1. Then R2 can be determined with Equation (5):

$$R_2(k\Omega) = \frac{V_{REF}}{V_O - V_{REF}} \times R_1(k\Omega) \quad (5)$$

Where $V_{REF}$ is 900mV.

To optimize the load transient response, a feed-forward capacitor ($C_{FF}$) is recommended in parallel with R1. R1 and $C_{FF}$ add an extra zero to the system, which improves loop response. R1 and $C_{FF}$ are selected so that the zero formed by R1 and $C_{FF}$ is located around 20kHz ~ 60kHz. See Equation (6):

$$f_Z = \frac{1}{2\pi \times R1 \times C_{FF}} \quad (6)$$

### Power Good (PGOOD)

The MPQ8634B has a power good (PGOOD) output. PGOOD is the open-drain of a MOSFET. Connect PGOOD to VCC or another external voltage source (less than 3.6V) through a pull-up resistor (typically 10kΩ). After applying the input voltage, the MOSFET turns on, so PGOOD is pulled to GND before TRK/REF is ready. After $V_{FB}$ reaches 92.5% of $V_{REF}$, PGOOD is pulled high after 0.8ms of delay.

When $V_{FB}$ drops to 80% of $V_{REF}$ or exceeds 116% of the nominal $V_{REF}$, PGOOD is latched low. PGOOD can only be pulled high again after a new soft start.

If the input supply fails to power the MPQ8634B, PGOOD is clamped low, even though PGOOD is tied to an external DC source through a pull-up resistor. The relationship between the PGOOD voltage and the pull-up current is shown in Figure 5.

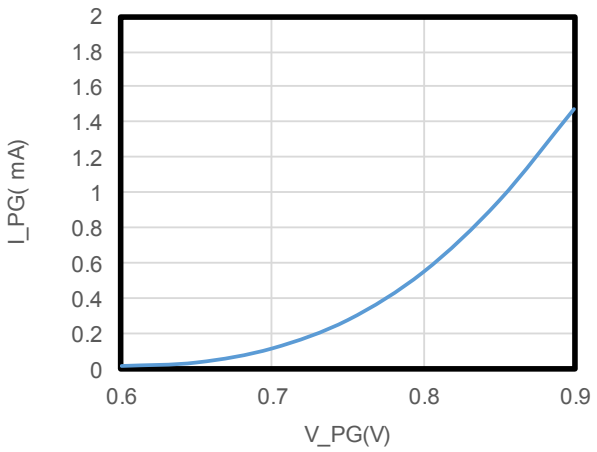



**Figure 5: PGOOD Clamped Voltage vs. Pull-Up Current**

### Enable (EN) Configuration

The MPQ8634B turns on when EN goes high. The MPQ8634B turns off when EN goes low. EN cannot be left floating for proper operation. EN can be driven by an analog or digital control logic signal to enable or disable the MPQ8634B.

The MPQ8634B provides accurate EN thresholds, so a resistor divider from VIN to AGND can be used to program the input voltage at which the MPQ8634B is enabled. This is highly recommended for applications where there is no dedicated EN control logic signal to avoid possible UVLO bouncing during power-up and power-down. The resistor divider values can be determined by Equation (7):

$$V_{IN\_START}(V) = VIH_{EN} \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (7)$$

Where $VIH_{EN}$ is 1.22V, typically.

$R_{UP}$ and $R_{DOWN}$ should be chosen so that the EN voltage ($V_{EN}$) does not exceed 3.6V when VIN reaches the maximum value.

EN can also be connected to VIN directly through a pull-up resistor ($R_{UP}$). $R_{UP}$ should be chosen so that the maximum current going to EN is 50μA. $R_{UP}$ can be calculated with Equation (8):

$$R_{UP}(k\Omega) = \frac{VIN_{MAX}(V)}{0.05(mA)} \quad (8)$$

# APPLICATION INFORMATION

### Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use ceramic capacitors for the best performance. During layout, place the input capacitors as close to VIN as possible.

The capacitance can vary significantly with the temperature. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable over a wide temperature range and offer very low ESR.

The capacitors must have a ripple current rating that exceeds the converter's maximum input ripple current. Estimate the input ripple current with Equation (9):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (9)$$

The worst-case condition occurs at VIN = $2V_{OUT}$, shown in Equation (10):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (10)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half the maximum load current. The input capacitor value determines the converter input voltage ripple. If there is an input voltage ripple requirement in the system, select an input capacitor that meets the specification.

Estimate the input voltage ripple with Equation (11):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

The worst-case condition occurs at VIN = $2V_{OUT}$, shown in Equation (12):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (12)$$

### Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use POSCAP or ceramic capacitors.

Estimate the output voltage ripple with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (13)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The capacitance also dominates the output voltage ripple. For simplification, estimate the output voltage ripple with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (14)$$

The ESR dominates the switching frequency impedance for the POSCAP capacitors. For simplification, the output ripple can be approximated with Equation (15):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (15)$$

### Selecting the Inductor

The inductor supplies constant current to the output load while being driven by the switching input voltage. A larger value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. Select an inductor value that allows the inductor peak-to-peak ripple current to be 30 - 40% of the maximum switch current limit. Also design for a peak inductor current that is below the maximum switch current limit. Calculate the inductance value using Equation (16):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_{L}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (16)$$

Where $\Delta I_L$ is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (17):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (17)$$

## PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For optimal performance, refer to Figure 6 and follow the guidelines below.

1. Place the input MLCC capacitors as close to VIN and PGND as possible.
2. Place the major MLCC capacitors on the same layer as the MPQ8634B.
3. Maximize the VIN and PGND copper plane to minimize parasitic impedance.
4. Place as many PGND vias as possible as close to PGND as possible to minimize both parasitic impedance and thermal resistance.
5. Place the VCC decoupling capacitor close to the device.
6. Connect AGND and PGND at the point of the VCC capacitor's ground connection.
7. Place the BST capacitor as close to BST and SW as possible with 20 mil or wider traces to route the path. It is recommended to use a bootstrap capacitor of 0.1μF to 1μF.
8. Place the REF capacitor close to TRK/REF to VSNS-.
9. Place via at least 10mm away from the positive side of the first input decoupling capacitor close to the IC if it must be placed on the PGOOD pad.
10. Place the OSENSE capacitor in between the output sense lines and close to the device.

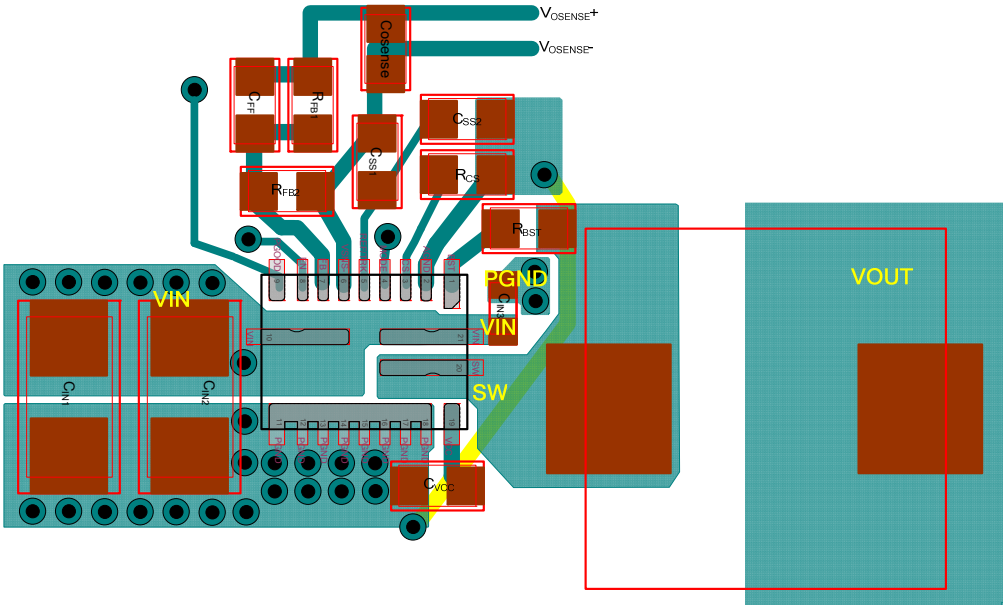
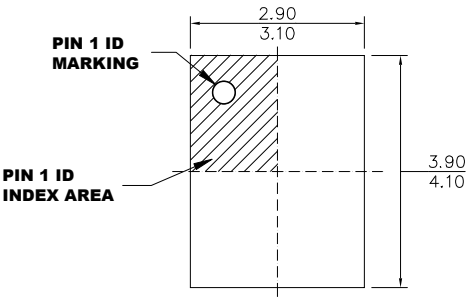


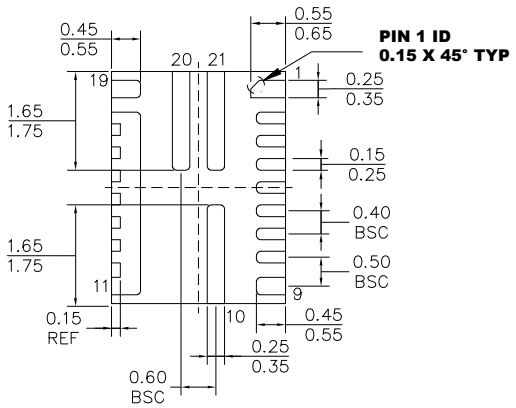

**Figure 6: Recommended PCB Layout**

# PACKAGE INFORMATION

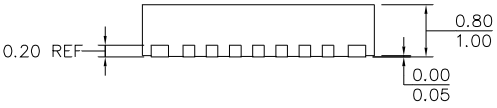
**QFN-21 (3mmx4mm)**



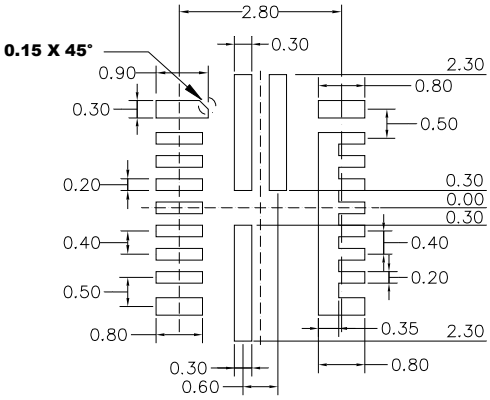

**TOP VIEW**




**BOTTOM VIEW**




**SIDE VIEW**




**RECOMMENDED LAND PATTERN**

**NOTE:**

**1) LAND PATTERN OF PIN1,9,10,11,19,20 AND 21 HAVE THE SAME WIDTH.**
**2) ALL DIMENSIONS ARE IN MILLIMETERS.**
**3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.**
**4) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.**
**5) JEDEC REFERENCE IS MO-220.**
**6) DRAWING IS NOT TO SCALE.**