

<b>PCN Number:</b>	20191117000	<b>PCN Date:</b>	Jan. 14, 2020
<b>Title:</b>	Datasheet for LMX2595		
<b>Customer Contact:</b>	PCN Manager	<b>Dept:</b>	Quality Services
<b>Change Type:</b>			
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Design
<input type="checkbox"/>	Assembly Process	<input checked="" type="checkbox"/>	Data Sheet
<input type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change
<input type="checkbox"/>	Mechanical Specification	<input type="checkbox"/>	Test Site
<input type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Material
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Materials
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Process

### Notification Details

#### Description of Change:

Texas Instruments Incorporated is announcing an information only notification. The product datasheet(s) is being updated as summarized below. The following change history provides further details.



LMX2595

SNAS736C –JUNE 2017–REVISED APRIL 2019

#### Changes from Revision B (March 2018) to Revision C

Page

- Changed the maximum output frequency from 19 GHz to 20 GHz everywhere in the data sheet. The newly recommended value for the DBLR\_IBIAS\_CTRL1 (R25[15:0]) extended the output frequency range and improved high frequency performance. The old value (1572) for the DBLR\_IBIAS\_CTRL1 still supports up to 19-GHz output and specs characterized in the *Electrical Characteristics* table. The new value (3115) provides a bonus in performance. . . . . 1
- Deleted the recommended bypass capacitor values for Vcc pins 7, 11, 15, 21, 26 and 37, as these capacitor values are not mandatory and the power supply filtering design is up to the user..... 7
- Added test condition "DBLR\_IBIAS\_CTRL1 = 1572" for P<sub>OUT</sub>, L<sub>VCO2X</sub> and H1/2, in order to emphasize that these data are taken while DBLR\_IBIAS\_CTRL1 is set to the old value (1572). With this register set to 3115, these specs can be improved. The details can be found in the applications section..... 9
- Added a new row for VCO doubler output range in EC table with DBLR\_IBIAS\_CTRL1 set to 3115. The frequency range is extended to 20 GHz..... 9
- Added table note for EC table stating that the performance of 1/2 harmonic, output power and noise floor with doubler enabled can be improved by setting DBLR\_IBIAS\_CTRL1 = 3115. .... 9
- Changed all the 'FRAC\_ORDER' to 'MASH\_ORDER' to avoid confusion..... 10
- Changed the names of timing specs to align with timing diagram: changed t<sub>CE</sub> to t<sub>ES</sub>, t<sub>CS</sub> to t<sub>DCS</sub>, t<sub>CH</sub> to t<sub>CDH</sub>, and t<sub>CES</sub> to t<sub>ECS</sub>..... 12
- Changed the names of timing specs to align with timing diagram: changed t<sub>ES</sub> to t<sub>CE</sub>, t<sub>CES</sub> to t<sub>ECS</sub>, added t<sub>DCS</sub> and t<sub>CDH</sub>, and changed t<sub>CS</sub> to t<sub>CR</sub>..... 13
- Changed the serial data input timing diagram and corrected the typo for 'SCK'..... 13
- Deleted the note 'The CSB transition from high to low must occur when SCK is low' from the serial data input timing diagram, because SPI mode 4 (CPOL = 1, CPHA = 1) is also supported, and SCK is held high when idle in mode 4 ..... 13
- Added note for the serial data input timing diagram to explain the t<sub>CE</sub> requirement for mode 4 (CPOL = 1, CPHA = 1) of SPI, because the diagram only indicated SPI mode 1 (CPOL = 0, CPHA = 0)..... 13
- Changed the serial data readback timing diagram..... 14
- Changed the note about MUXout clocking out and emphasized the effect of t<sub>CR</sub> on the readback data available time ..... 14
- Added phase noise plot for 16-, 17- and 20-GHz frequency output ..... 15
- Changed the phase noise plot for 18- and 19-GHz frequency output after changing DBLR\_IBIAS\_CTRL1

(R25[15:0]) to the new value .....	15
• Changed the $f_{OUT}$ test conditions in the <i>Closed-Loop Phase Noise at 3.5 GHz</i> graph from: 14 GHz / 2 = 3.5 GHz to: 14 GHz / 4 = 3.5 GHz .....	16
• Changed the <i>Output Power vs Pull-up</i> graph. Output power below 15GHz is shown in "output power across frequency"; output power above 15GHz is shown in "output power vs temperature with doubler". .....	17
• Split the <i>Output Power vs Temperature</i> typical performance plot into two plots: <i>Output Power vs Temperature Without Doubler</i> , which goes up to 15 GHz, and <i>Output Power vs Temperature With Doubler</i> that is between 15 GHz and 21 GHz. The data for "without doubler" is unchanged because change of DBLR_IBIAS_CTRL1 does not impact performance under 15 GHz, while the data for "with doubler" plot is taken with DBLR_IBIAS_CTRL1 (R25[15:0]) set to the new value (3115).....	17
• Added <i>Normalized Output Power Across OUTA_PWR With Resistor Pullup</i> graph.....	17
• Changed "Vtune" to "Indirect Vtune" when LD_TYPE = 1 .....	23
• Changed description for LD_TYPE. ....	23
• Added description of Indirect Vtune. ....	24
• Added description for the 'no assist' mode, mphasized the effect of VCO_SEL, VCO_DACISSET_STRT and VCO_CAPCTRL_STRT under 'no assist' mode, and added recommended values for these registers .....	25
• Added description for the 'full assist' mode to allow the user to set VCO amplitude and capcode using linear interpolation under certain conditions.....	25
• Changed <i>OUTx_PWR Recommendations for Resistor Pullup</i> table .....	27
• Added description for category 3 of SYNC feature stating that FCAL_EN needs to be 1.....	31
• Changed description of MASH_SEED .....	31
• Added 10-ms wait time before re-programming register R0 in recommended initial power-up sequence .....	42
• Added the <i>General Programming Requirements</i> section based on frequently asked questions.....	42
• Changed register R4 in the register map to: exposed ACAL_CMP_DLY .....	43
• Changed the register R20[14] value from 0 to 1 in the full register map to match the R20 register description .....	43
• Changed register R25 in the register map; exposed the register 'DBLR_IBIAS_CTRL1.....	44
• Changed the R0[14] register field name in the register map from VCO_PHASE_SYNC_EN to VCO_PHASE_SYNC. to align with the rest of the data sheet .....	48
• Added recommended value for register CAL_CLK_DIV when lock time is not of concern.....	48
• Changed the typo for register 'VCO_DACISSET' in the register map. Bit 0 of this register was not included in the map. The full register map and register description were correct .....	50
• Added description to the R4[15:8]: ACAL_CMP_DLY register.....	50
• Deleted the bit description '0: disabled; 1: enabled' for register 'PLL_N' .....	51
• Added description to the R60[15:0] LD_DLY register .....	53
• Added description for register R25[15:0]: DBLR_IBIAS_CTRL1 and changed the default register value from 0x0624 to 0x0C2B.....	55
• Changed the R31[14] register name from CHDIV_DIV2 to SEG1_EN to align with the naming in the TICS Pro GUI .....	55
• Changed the R105[1:0] field name from RAMP_NEXT_TRIG to RAMP1_NEXT_TRIG .....	60
• Added application section "Performance Comparison Between 1572 (0x0624) and 3115 (0x0C2B) For Register DBLR_IBIAS_CTRL1 (R25[15:0])" to compare the performance with old and new DBLR_IBIAS_CTRL1 (R25[15:0]) values. ....	62
• Added the <i>Bias Levels of Pins</i> table.....	67

The datasheet number will be changing.

Device Family	Change From:	Change To:
LMX2595	SNAS736B	SNAS736C

These changes may be reviewed at the datasheet links provided.

<http://www.ti.com/product/LMX2595>

**Reason for Change:**

To accurately reflect device characteristics.

<b>Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):</b>			
No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.			
<b>Changes to product identification resulting from this PCN:</b>			
None.			
<b>Product Affected:</b>			
LMX2595RHAR	LMX2595RHAT		

For questions regarding this notice, e-mails can be sent to the contacts shown below or your local Field Sales Representative.

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