

# ON Semiconductor

## Is Now

# onsemi™

To learn more about onsemi™, please visit our website at  
[www.onsemi.com](http://www.onsemi.com)

---

**onsemi** and **onsemi** and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.

# CS8147

## 10 V/5.0 V Low Dropout Dual Regulator with ENABLE

The CS8147 is a 10 V/5.0 V dual output linear regulator. The 10V  $\pm 5.0\%$  output sources 500 mA and the 5.0 V  $\pm 3\%$  output sources 70 mA. The secondary output is inherently stable and does not require an external capacitor.

The on board ENABLE function controls the regulator's two outputs. When ENABLE is high, the regulator is placed in SLEEP mode. Both outputs are disabled and the regulator draws only 70  $\mu$ A of quiescent current.

The regulator is protected against overvoltage conditions. Both outputs are protected against short circuit and thermal runaway conditions.

The CS8147 is packaged in a 5 lead TO-220 with copper tab. The copper tab can be connected to a heat sink if necessary.

### Features

- Two Regulated Outputs
  - 10 V  $\pm 5.0\%$ ; 500 mA
  - 5.0 V  $\pm 3.0\%$ ; 70 mA
- 70  $\mu$ A SLEEP Mode Current
- Inherently Stable Secondary Output (No Output Capacitor Required)
- Fault Protection
  - Overvoltage Shutdown
  - Reverse Battery
  - 60 V Peak Transient
  - -50 V Reverse Transient
  - Short Circuit
  - Thermal Shutdown
- CMOS Compatible ENABLE Input with Low ( $I_{OUT(max)}$ ) Input Current

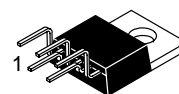


ON Semiconductor™

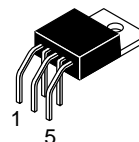
<http://onsemi.com>



TO-220  
FIVE LEAD  
T SUFFIX  
CASE 314D



TO-220  
FIVE LEAD  
TVA SUFFIX  
CASE 314K



TO-220  
FIVE LEAD  
THA SUFFIX  
CASE 314A

### PIN CONNECTIONS AND MARKING DIAGRAM



Tab = GND  
Pin 1. ENABLE  
2.  $V_{IN}$   
3. GND  
4.  $V_{OUT1}$  (10 V)  
5.  $V_{OUT2}$  (5.0 V)

A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
CS8147YT5	TO-220* STRAIGHT	50 Units/Rail
CS8147YTVA5	TO-220* VERTICAL	50 Units/Rail
CS8147YTHA5	TO-220* HORIZONTAL	50 Units/Rail

\*Five lead.

# CS8147

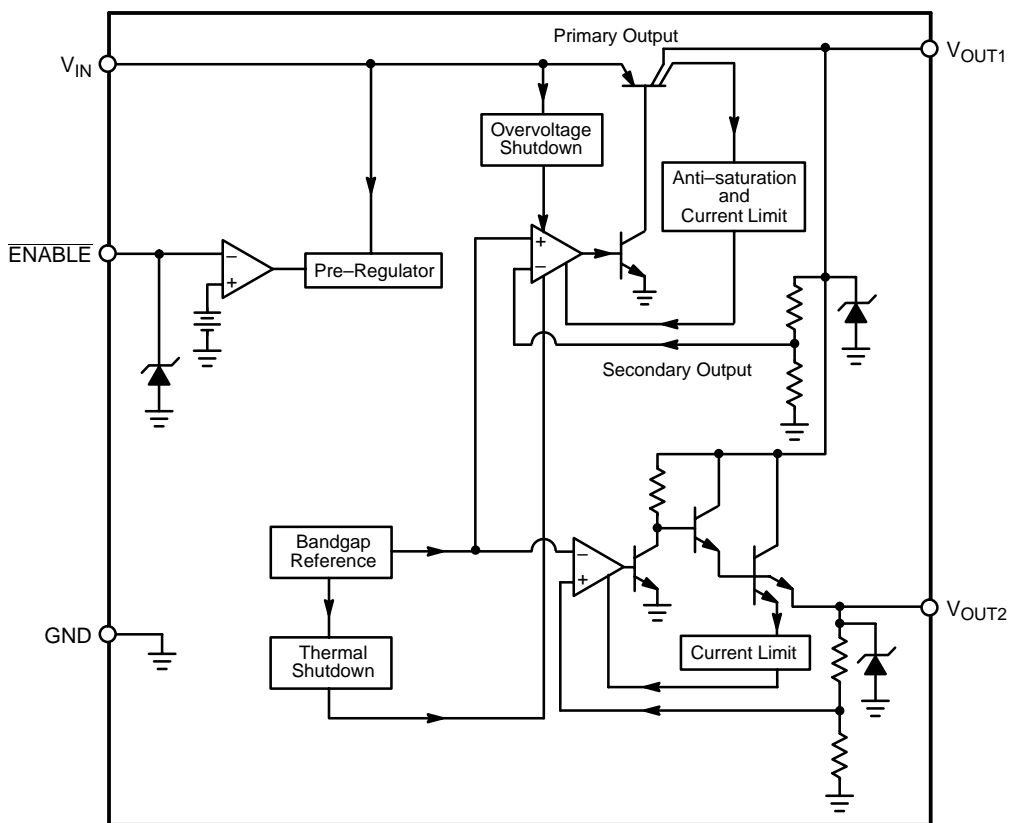


Figure 1. Block Diagram

## ABSOLUTE MAXIMUM RATINGS\*

Rating	Value	Unit
Input Voltage:	DC	-18 to 26
	Positive Peak Transient Voltage (Note 1.)	60
	Negative Peak Transient Voltage	-50
ESD (Human Body Model)	2.0	kV
ENABLE Input	-0.3 to 10	V
Internal Power Dissipation	Internally Limited	-
Junction Temperature Range	-40 to +150	°C
Storage Temperature Range	-65 to +150	°C
Lead Temperature Soldering:	Wave Solder (through hole styles only) (Note 2.)	260 peak

1. 46 V Load Dump @  $V_{IN} = 14$  V

2. 10 second maximum.

\*The maximum package power dissipation must be observed.

# CS8147

**ELECTRICAL CHARACTERISTICS for  $V_{OUT}$ :** ( $V_{IN} = 14\text{ V}$ ,  $I_{OUT1} = I_{OUT2} = 5.0\text{ mA}$ ,  $-40^{\circ}\text{C} < T_J < 150^{\circ}\text{C}$ ,  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ ,  $\overline{\text{ENABLE}} = \text{LOW}$ ; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
<b>Primary Output (<math>V_{OUT1}</math>)</b>					
Output Voltage	$13\text{ V} \leq V_{IN} \leq 26\text{ V}$ , $I_{OUT1} \leq 500\text{ mA}$	9.50	10.00	10.5	V
Dropout Voltage	$I_{OUT1} = 500\text{ mA}$	–	0.5	0.7	V
Line Regulation	$11\text{ V} \leq V_{IN} \leq 18\text{ V}$ , $I_{OUT1} = 250\text{ mA}$	–	45	90	mV
Load Regulation	$5.0\text{ mA} \leq I_{OUT1} \leq 500\text{ mA}$	–	15	75	mV
Quiescent Current	$I_{OUT1} \leq 1.0\text{ mA}$ , No Load on $V_{OUT2}$ , $V_{IN} = 18\text{ V}$ $I_{OUT1} = 500\text{ mA}$ , No Load on $V_{OUT2}$ , $V_{IN} = 11\text{ V}$	– –	3.0 60	7.0 120	mA mA
Quiescent Current	$\overline{\text{ENABLE}} = \text{HIGH}$ , $V_{OUT1}$ , $V_{OUT2} = \text{OFF}$	–	70	200	$\mu\text{A}$
Current Limit	–	0.55	0.80	–	A
Long Term Stability	–	–	50	–	mV/khr
Overshoot Shutdown	$V_{OUT1}$ and $V_{OUT2}$	32	36	40	V

<b>Secondary Output (<math>V_{OUT2}</math>)</b>					
Output Voltage	$6.0\text{ V} \leq V_{IN} \leq 26\text{ V}$ , $1.0\text{ mA} \leq I_{OUT2} \leq 70\text{ mA}$	4.85	5.00	5.15	V
Dropout Voltage	$I_{OUT2} \leq 70\text{ mA}$	–	1.5	2.5	V
Line Regulation	$11 \leq V_{IN} \leq 18\text{ V}$ , $I_{OUT} = 70\text{ }\mu\text{A}$	–	4.0	50	mV
Load Regulation	$1.0\text{ mA} \leq I_{OUT2} \leq 70\text{ mA}$ , $V_{IN} = 14\text{ V}$	–	10	50	mV
Current Limit	–	–	150	–	mA

<b>ENABLE Function (<math>\overline{\text{ENABLE}}</math>)</b>					
Input $\overline{\text{ENABLE}}$ Threshold	$V_{OUT2(\text{ON})}$ $V_{OUT1(\text{OFF})}$	– 0.8	1.40 1.40	2.50 –	V V
Input $\overline{\text{ENABLE}}$ Current	Input Voltage Range 0 to 5.0 V	–10	–	10	$\mu\text{A}$

## PACKAGE PIN DESCRIPTION

PACKAGE LEAD #	LEAD SYMBOL	FUNCTION
5 Lead TO–220		
1	ENABLE	CMOS compatible input lead; switches $V_{OUT1}$ and $V_{OUT2}$ on and off. When $\overline{\text{ENABLE}}$ is low, $V_{OUT1}$ and $V_{OUT2}$ are active.
2	$V_{IN}$	Supply voltage, usually direct from battery.
3	GND	Ground connection.
4	$V_{OUT1}$	Regulated output 10 V, 500 mA (typ).
5	$V_{OUT2}$	Secondary output 5.0 V, 70 mA (typ).

TYPICAL PERFORMANCE CHARACTERISTICS

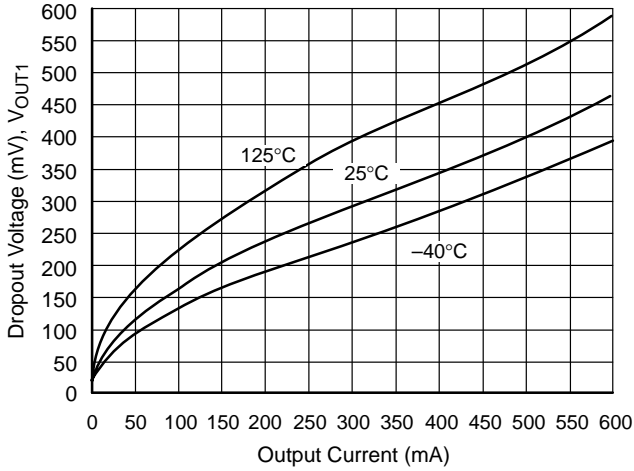


Figure 2. Dropout Voltage vs. Output Current ( $V_{OUT1}$ )

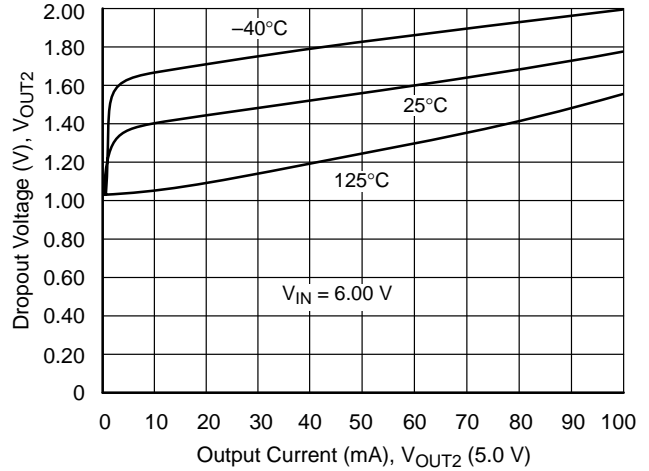


Figure 3. Dropout Voltage vs. Output Current ( $V_{OUT2}$ )

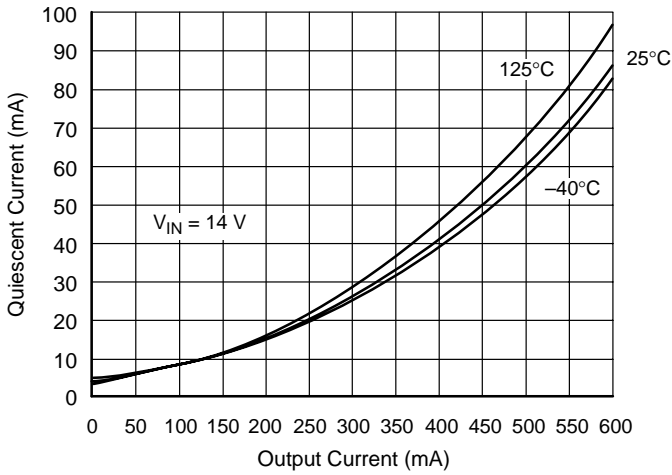


Figure 4. Quiescent Current vs. Output Current ( $V_{OUT1}$ )

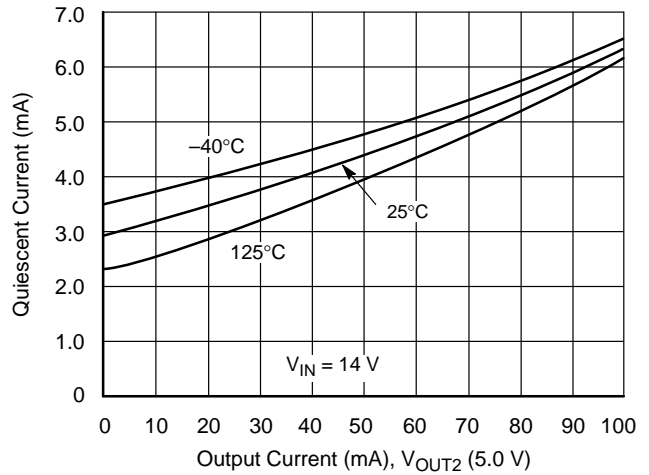


Figure 5. Quiescent Current vs. Output Current ( $V_{OUT2}$ )

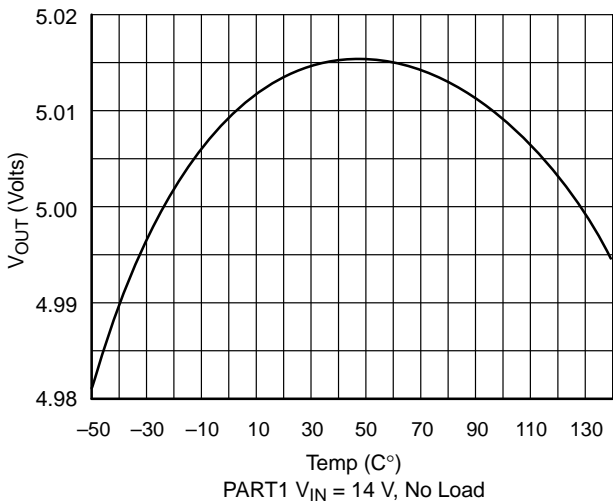


Figure 6.  $V_{OUT2}$  vs. Temperature

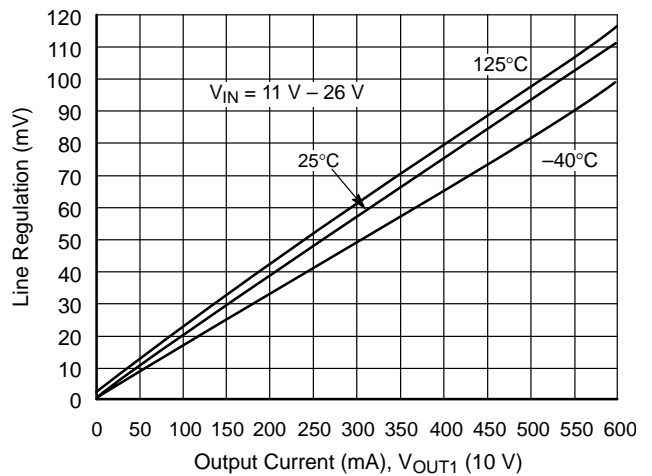


Figure 7. Line Regulation vs. Output Current ( $V_{OUT1}$ )

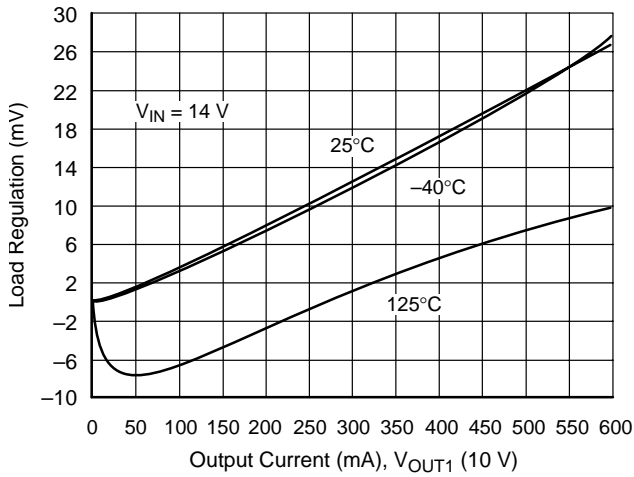


Figure 8. Load Regulation vs. Output Current ( $V_{OUT1}$ )

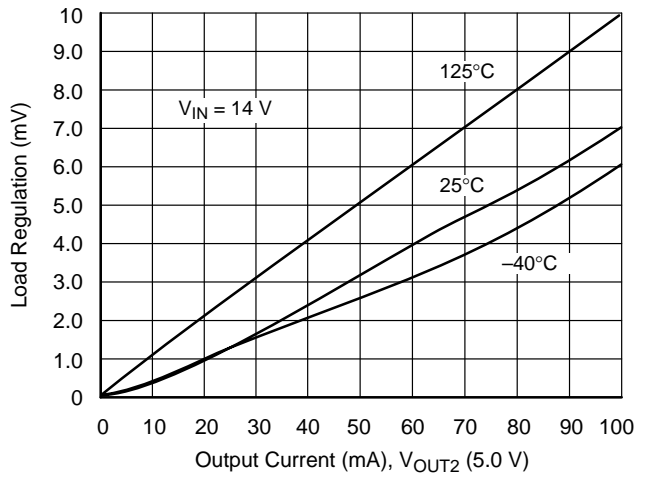


Figure 9. Load Regulation vs. Output Current ( $V_{OUT2}$ )

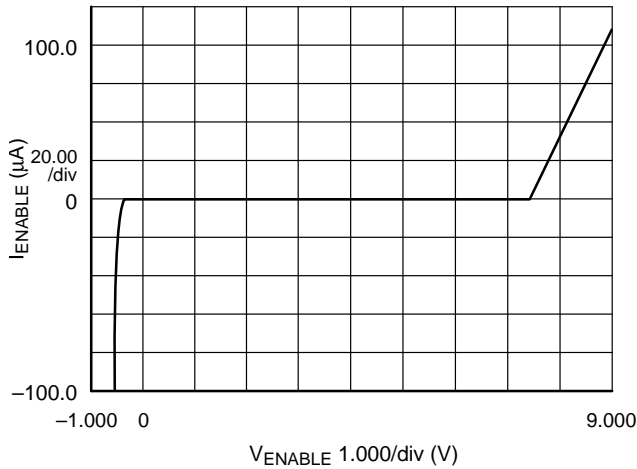


Figure 10.  $\overline{ENABLE}$  Input Current vs. Input Voltage

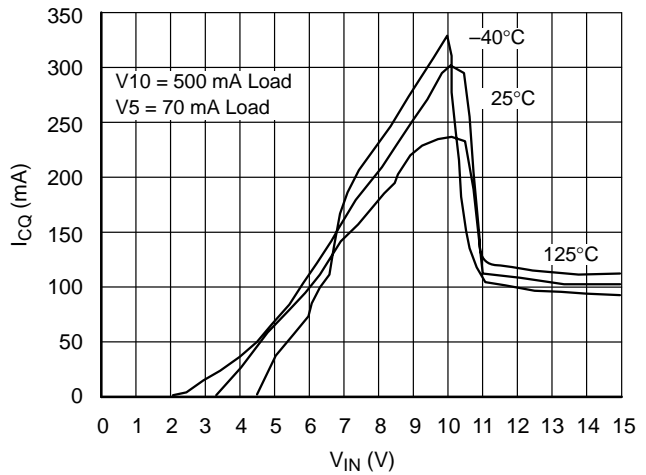


Figure 11. Quiescent Current ( $I_{CQ}$ ) vs.  $V_{IN}$  Overtemperature

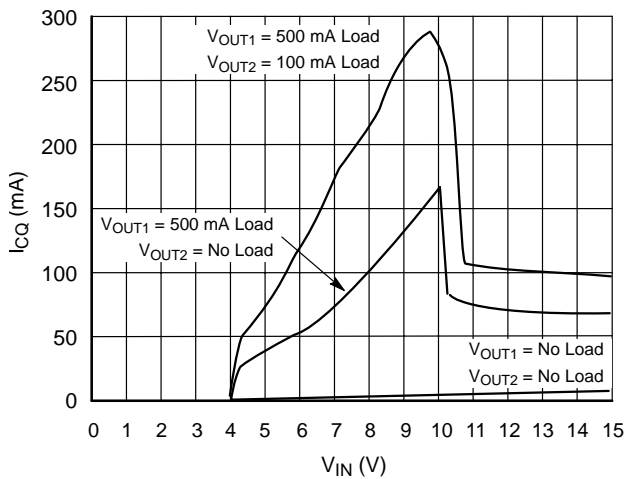


Figure 12. Quiescent Current ( $I_{CQ}$ ) vs.  $V_{IN}$  Over  $R_{LOAD}$

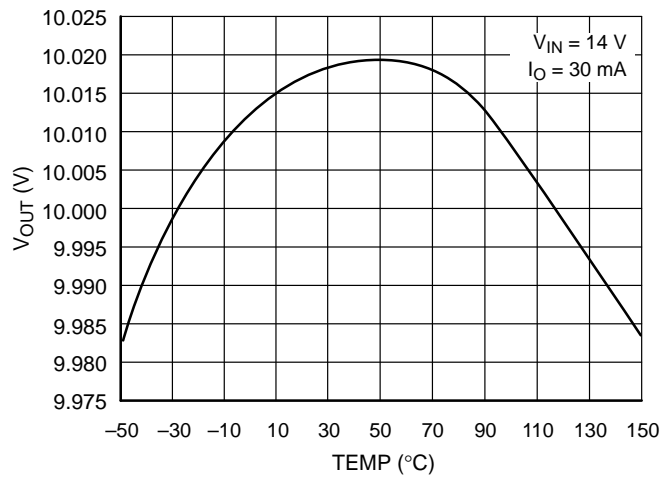


Figure 13.  $V_{OUT1}$  vs. Temperature

DEFINITION OF TERMS

**Dropout Voltage** – The input–output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

**Current Limit** – Peak current that can be delivered to the output.

**Input Voltage** – The DC voltage applied to the input terminals with respect to ground.

**Input Output Differential** – The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

**Line Regulation** – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

**Load Regulation** – The change in output voltage for a change in load current at constant chip temperature.

**Long Term Stability** – Output voltage stability under accelerated life–test conditions after 1000 hours with maximum rated voltage and junction temperature.

**Output Noise Voltage** – The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

**Quiescent Current** – The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

**Ripple Rejection** – The ratio of the peak–to–peak input ripple voltage to the peak–to–peak output ripple voltage.

**Temperature Stability of V<sub>OUT</sub>** – The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

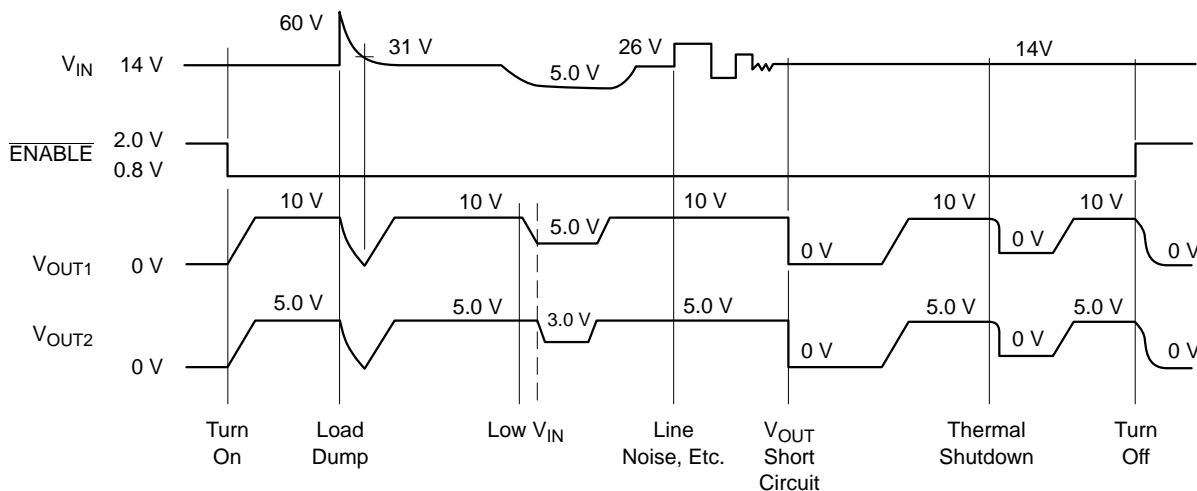
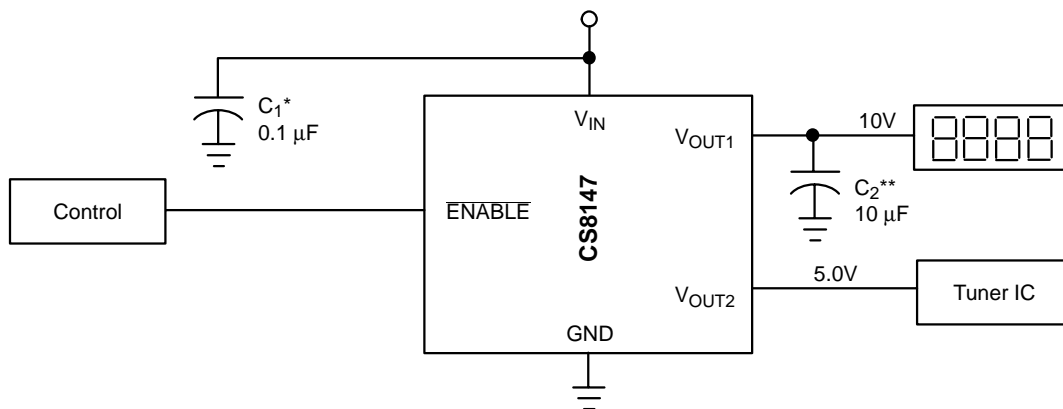


Figure 14. Typical Circuit Waveform



\* C<sub>1</sub> is required if the regulator is located away from the power source filter.

\*\* C<sub>2</sub> is required for stability.

Figure 15. Test & Applications Circuit

## APPLICATION NOTES

Since both outputs are controlled by the same  $\overline{\text{ENABLE}}$ , the CS8147 is ideal for applications where a sleep mode is required. Using the CS8147, a section of circuitry such as a display and nonessential 5.0 V circuits can be shut down under microprocessor control to conserve energy.

The test applications circuit diagram shows an automotive radio application where the display is powered by 10 V from  $V_{\text{OUT1}}$  and the Tuner IC is powered by 5.0 V from  $V_{\text{OUT2}}$ . Neither output is required unless both the ignition and the Radio On/OFF switch are on.

**Stability Considerations**

The secondary output  $V_{\text{OUT2}}$  is inherently stable and does not require a compensation capacitor. However a compensation capacitor connected between  $V_{\text{OUT1}}$  and ground is required for stability in most applications.

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures ( $-25^{\circ}\text{C}$  to  $-40^{\circ}\text{C}$ ), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor C2 shown in the test and applications circuit should work for most applications, however it is not necessarily the optimized solution.

To determine acceptable value for C2 for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

**Step 1:** Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

**Step 2:** With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

**Step 3:** Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

**Step 4:** Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase.

This point represents the worst case input voltage conditions.

**Step 5:** If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

**Step 6:** Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

**Step 7:** Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found for each output, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of  $\pm 20\%$  so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitors should be less than 50% of the maximum allowable ESR found in step 3 above.

**Calculating Power Dissipation in a Dual Output Linear Regulator**

The maximum power dissipation for a dual output regulator (Figure 16) is

$$P_{D(\text{max})} = (V_{\text{IN}(\text{max})} - V_{\text{OUT1}(\text{min})})I_{\text{OUT1}(\text{max})} + (V_{\text{IN}(\text{max})} - V_{\text{OUT2}(\text{min})})I_{\text{OUT2}(\text{max})} + V_{\text{IN}(\text{max})}I_{\text{Q}} \quad (1)$$

where:

$V_{\text{IN}(\text{max})}$  is the maximum input voltage,

$V_{\text{OUT1}(\text{min})}$  is the minimum output voltage from  $V_{\text{OUT1}}$ ,

$V_{\text{OUT2}(\text{min})}$  is the minimum output voltage from  $V_{\text{OUT2}}$ ,

$I_{\text{OUT1}(\text{max})}$  is the maximum output current, for the application,

$I_{\text{OUT2}(\text{max})}$  is the maximum output current, for the application, and

$I_{\text{Q}}$  is the quiescent current the regulator consumes at  $I_{\text{OUT}(\text{max})}$ .

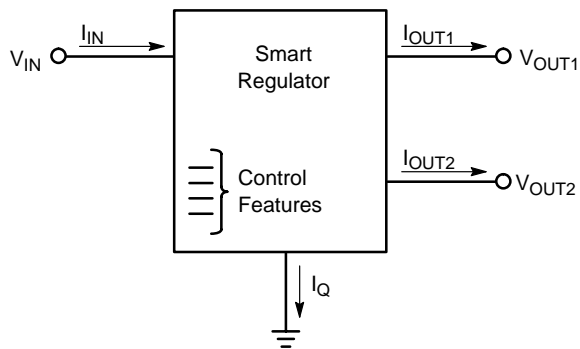
Once the value of  $P_{D(\text{max})}$  is known, the maximum permissible value of  $R_{\theta\text{JA}}$  can be calculated:

$$R_{\theta\text{JA}} = \frac{150^{\circ}\text{C} - T_{\text{A}}}{P_{\text{D}}} \quad (2)$$

The value of  $R_{\theta\text{JA}}$  can be compared with those in the package section of the data sheet. Those packages with  $R_{\theta\text{JA}}$ 's less than the calculated value in equation 2 will keep the die temperature below  $150^{\circ}\text{C}$ .

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.





**Figure 16. Dual Output Regulator With Key Performance Parameters Labeled.**

### Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of  $R_{\theta JA}$ :

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where:

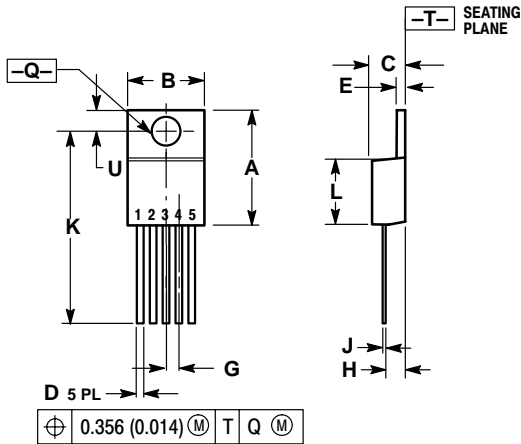
$R_{\theta JC}$  = the junction-to-case thermal resistance,  
 $R_{\theta CS}$  = the case-to-heatsink thermal resistance, and  
 $R_{\theta SA}$  = the heatsink-to-ambient thermal resistance.

$R_{\theta JC}$  appears in the package section of the data sheet. Like  $R_{\theta JA}$ , it too is a function of package type.  $R_{\theta CS}$  and  $R_{\theta SA}$  are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

# CS8147

## PACKAGE DIMENSIONS

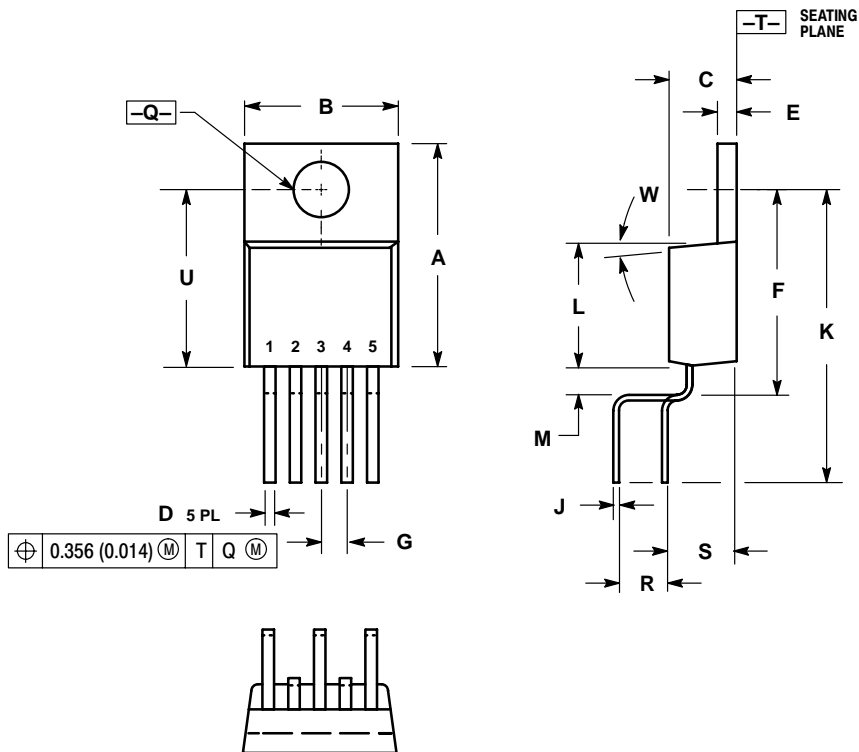
TO-220  
FIVE LEAD  
T SUFFIX  
CASE 314D-04  
ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
G	0.067 BSC		1.702 BSC	
H	0.087	0.112	2.210	2.845
J	0.015	0.025	0.381	0.635
K	0.990	1.045	25.146	26.543
L	0.320	0.365	8.128	9.271
Q	0.140	0.153	3.556	3.886
U	0.105	0.117	2.667	2.972

TO-220  
FIVE LEAD  
TVA SUFFIX  
CASE 314K-01  
ISSUE O

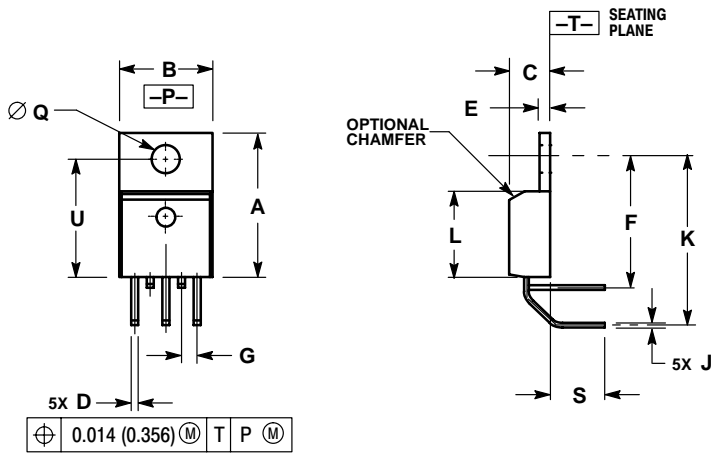


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.560	0.590	14.22	14.99
B	0.385	0.415	9.78	10.54
C	0.160	0.190	4.06	4.83
D	0.027	0.037	0.69	0.94
E	0.045	0.055	1.14	1.40
F	0.530	0.545	13.46	13.84
G	0.067 BSC		1.70 BSC	
J	0.014	0.022	0.36	0.56
K	0.785	0.800	19.94	20.32
L	0.321	0.337	8.15	8.56
M	0.063	0.078	1.60	1.98
Q	0.146	0.156	3.71	3.96
R	0.271	0.321	6.88	8.15
S	0.146	0.196	3.71	4.98
U	0.460	0.475	11.68	12.07
W	5°		5°	

# CS8147

## TO-220 FIVE LEAD THA SUFFIX CASE 314A-03 ISSUE E




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 0.043 (1.092) MAXIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
F	0.570	0.585	14.478	14.859
G	0.067 BSC		1.702 BSC	
J	0.015	0.025	0.381	0.635
K	0.730	0.745	18.542	18.923
L	0.320	0.365	8.128	9.271
Q	0.140	0.153	3.556	3.886
S	0.210	0.260	5.334	6.604
U	0.468	0.505	11.888	12.827

### PACKAGE THERMAL DATA

Parameter		TO-220	Unit
R <sub>θJC</sub>	Typical	2.4	°C/W
R <sub>θJA</sub>	Typical	50	°C/W

# Notes

**ON Semiconductor** and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

## PUBLICATION ORDERING INFORMATION

### NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** ONlit@hibbertco.com  
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

**EUROPE:** LDC for ON Semiconductor – European Support

**German Phone:** (+1) 303-308-7140 (Mon-Fri 2:30pm to 7:00pm CET)  
**Email:** ONlit-german@hibbertco.com  
**French Phone:** (+1) 303-308-7141 (Mon-Fri 2:00pm to 7:00pm CET)  
**Email:** ONlit-french@hibbertco.com  
**English Phone:** (+1) 303-308-7142 (Mon-Fri 12:00pm to 5:00pm GMT)  
**Email:** ONlit@hibbertco.com

**EUROPEAN TOLL-FREE ACCESS\*: 00-800-4422-3781**

\*Available from Germany, France, Italy, UK, Ireland

### CENTRAL/SOUTH AMERICA:

**Spanish Phone:** 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)  
**Email:** ONlit-spanish@hibbertco.com

**ASIA/PACIFIC:** LDC for ON Semiconductor – Asia Support

**Phone:** 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)  
**Toll Free** from Hong Kong & Singapore:  
**001-800-4422-3781**  
**Email:** ONlit-asia@hibbertco.com

**JAPAN:** ON Semiconductor, Japan Customer Focus Center

4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031  
**Phone:** 81-3-5740-2745  
**Email:** r14525@onsemi.com

**ON Semiconductor Website:** <http://onsemi.com>

For additional information, please contact your local Sales Representative.