MOSFET – Power, Single, N-Channel
40 V, 0.67 mΩ, 370 A

NTMFS5C404NL

V$_{(BR)DSS}$	R$_{DS(ON)}$ MAX	I$_D$ MAX
40 V	0.67 mΩ @ 10 V	370 A
	1.0 mΩ @ 4.5 V	

Features
- Small Footprint (5x6 mm) for Compact Design
- Low R$_{DS(on)}$ to Minimize Conduction Losses
- Low Q$_G$ and Capacitance to Minimize Driver Losses
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

D (5)
G (4)
S (1,2,3)

N−CHANNEL MOSFET

MAXIMUM RATINGS (T$_J$ = 25°C unless otherwise noted)

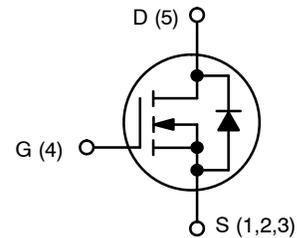| Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V$_{DSS}$	40	V
Gate−to−Source Voltage			V$_{GS}$	±20	V
Continuous Drain Current R$_{\theta JC}$ (Notes 1, 3)	Steady State	T$_C$ = 25°C	I$_D$	370	A
		T$_C$ = 100°C		260	
Power Dissipation R$_{\theta JC}$ (Note 1)		T$_C$ = 25°C	P$_D$	167	W
		T$_C$ = 100°C		67	
Continuous Drain Current R$_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T$_A$ = 25°C	I$_D$	52	A
		T$_A$ = 100°C		37	
Power Dissipation R$_{\theta JA}$ (Notes 1 & 2)		T$_A$ = 25°C	P$_D$	3.2	W
		T$_A$ = 100°C		1.3	
Pulsed Drain Current	T$_A$ = 25°C, t$_p$ = 10 μs		I$_{DM}$	900	A
Operating Junction and Storage Temperature			T$_J$, T$_{stg}$	−55 to + 175	°C
Source Current (Body Diode)			I$_S$	184	A
Single Pulse Drain−to−Source Avalanche Energy (I$_{L(pk)}$ = 38 A)			E$_{AS}$	907	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T$_L$	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
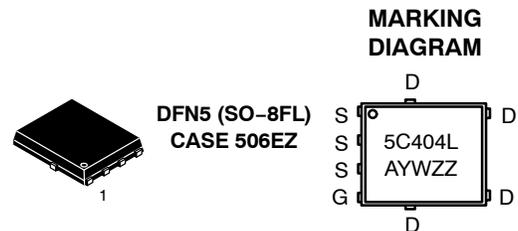
THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case – Steady State	R$_{\theta JC}$	0.75	°C/W
Junction−to−Ambient – Steady State (Note 2)	R$_{\theta JA}$	39	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAM

DFN5 (SO−8FL) CASE 506EZ

S D
S 5C404L
S AYWZZ
G D

5C404L = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION
See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NTMFS5C404NL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				21.6		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25 °C			10	μA
			T_J = 125°C			250	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−6.2		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 50 A		0.52	0.67	mΩ
		V_{GS} = 4.5 V	I_D = 50 A		0.75	1.0	
Forward Transconductance	g_{FS}	V_{DS} =15 V, I_D = 50 A			270		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 25 V			12168		pF
Output Capacitance	C_{OSS}				4538		
Reverse Transfer Capacitance	C_{RSS}				79.8		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 20 V; I_D = 50 A			81		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 20 V; I_D = 50 A			181		
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 4.5 V, V_{DS} = 20 V; I_D = 50 A			8.5		
Gate−to−Source Charge	Q_{GS}				27.8		
Gate−to−Drain Charge	Q_{GD}				23.8		
Plateau Voltage	V_{GP}				2.7		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 20 V, I_D = 50 A, R_G = 1.0 Ω			24		ns
Rise Time	t_r				135		
Turn−Off Delay Time	$t_{d(OFF)}$				87		
Fall Time	t_f				157		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 50 A	T_J = 25°C		0.7	1.2	V
			T_J = 125°C		0.61		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 50 A			97.4		ns
Charge Time	t_a				46.5		
Discharge Time	t_b				50.9		
Reverse Recovery Charge	Q_{RR}				190		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.
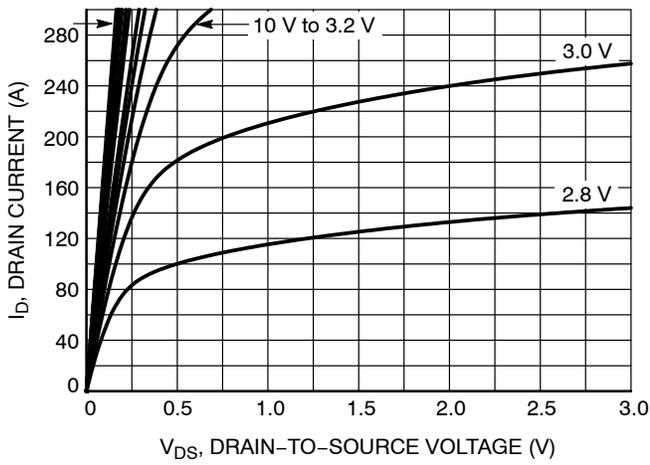
TYPICAL CHARACTERISTICS
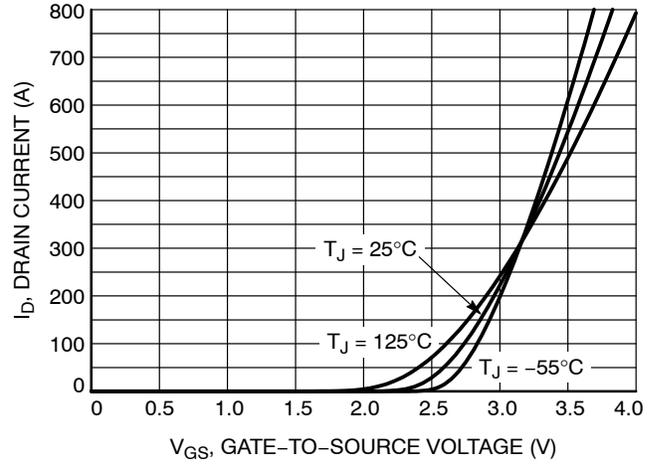

Figure 1. On−Region Characteristics

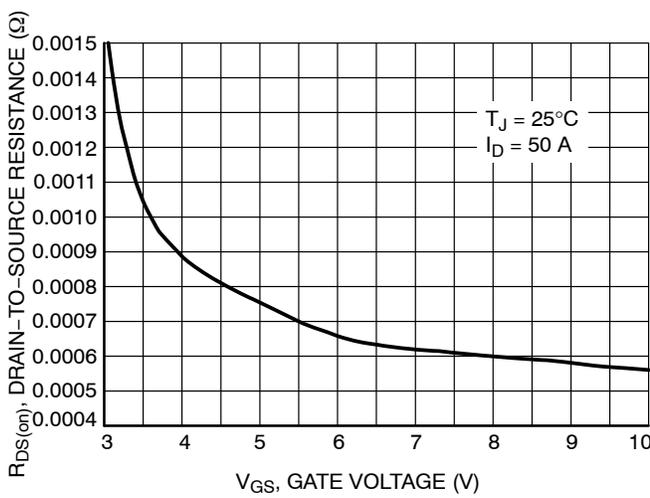Figure 2. Transfer Characteristics

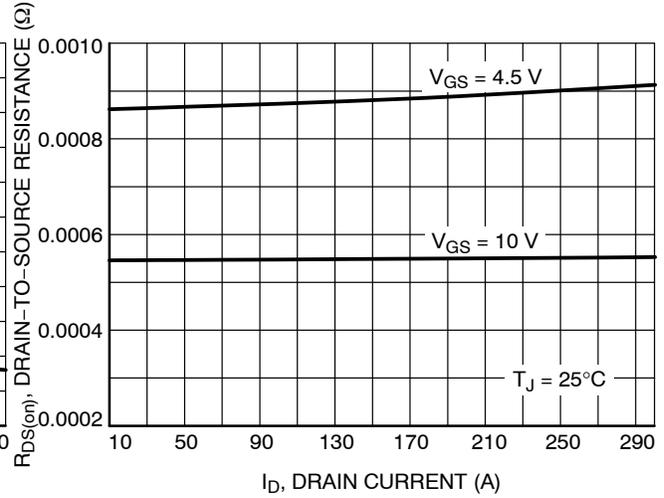Figure 3. On−Resistance vs. Gate−to−Source Voltage

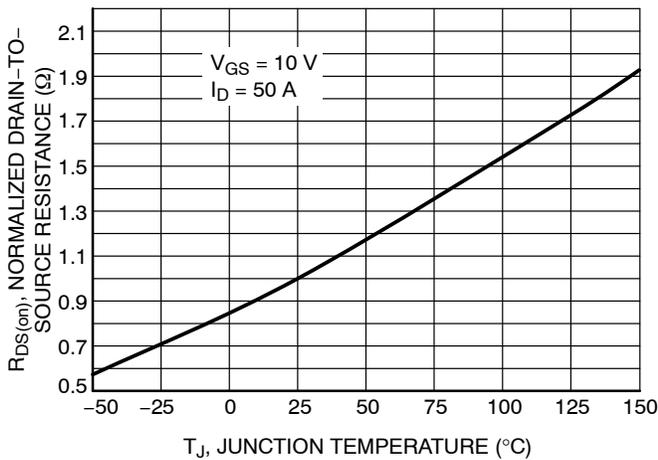
Figure 4. On−Resistance vs. Drain Current and Gate Voltage

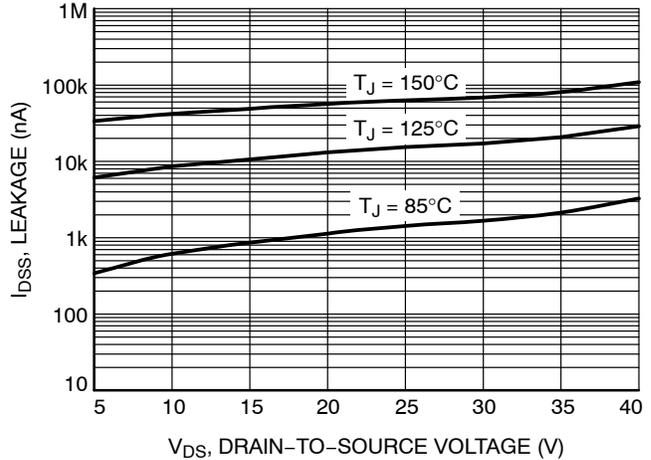Figure 5. On−Resistance Variation with Temperature

Figure 6. Drain−to−Source Leakage Current vs. Voltage
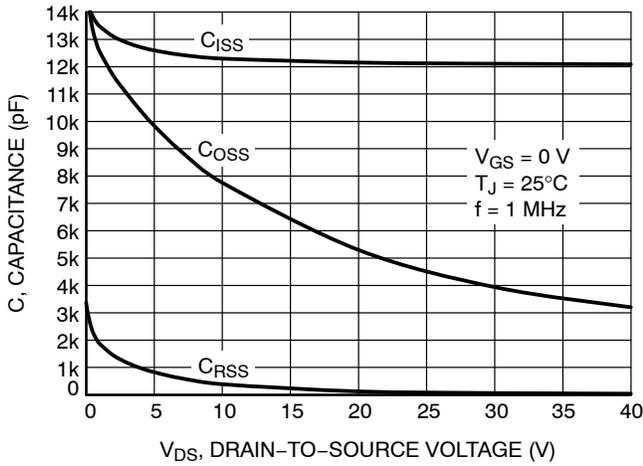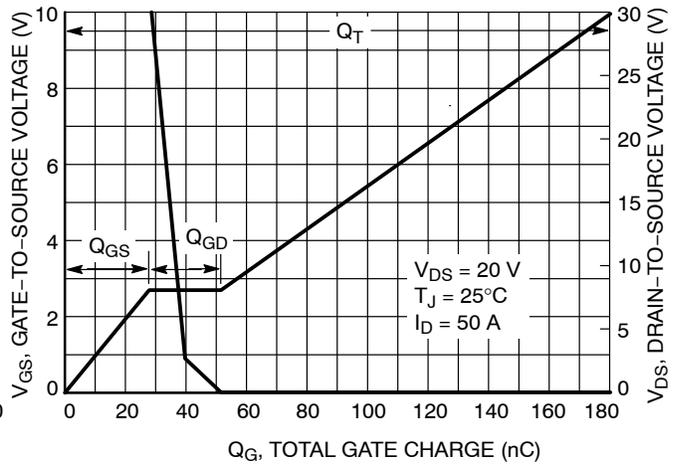
NTMFS5C404NL

Figure 7. Capacitance Variation

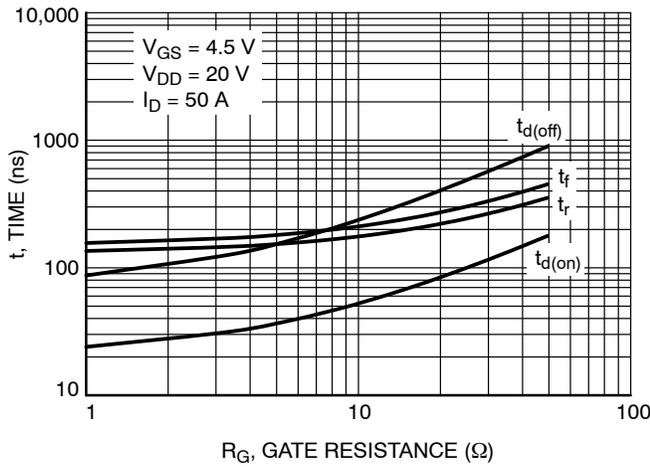Figure 8. Gate−to−Source and
Drain−to−Source Voltage vs. Total Charge

Figure 9. Resistive Switching Time Variation
vs. Gate Resistance
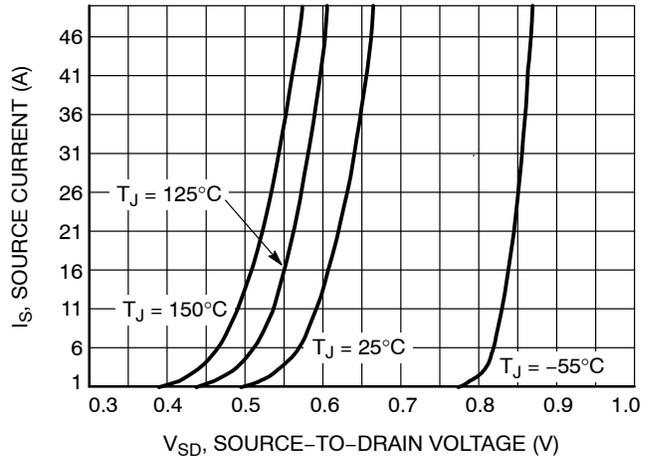
Figure 10. Diode Forward Voltage vs. Current
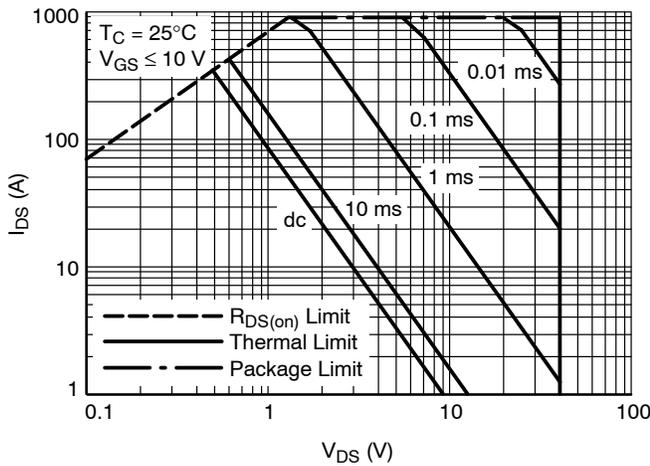
Figure 11. Safe Operating Area
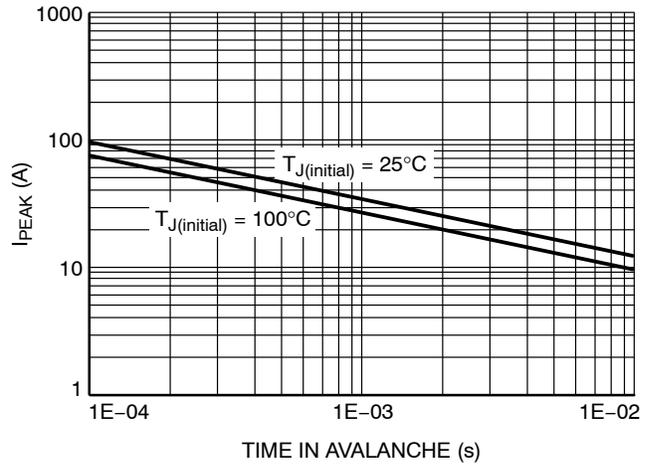
Figure 12. I_{PEAK} vs. Time in Avalanche

NTMFS5C404NL
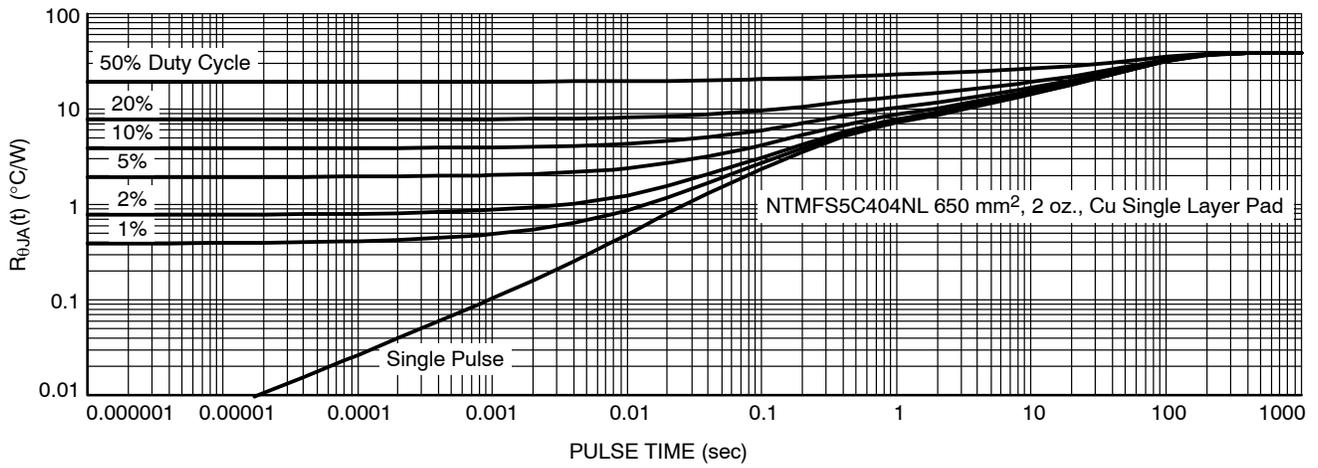
Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping[†]
NTMFS5C404NLT1G	5C404L	DFN5 (Pb–Free)	1500 / Tape & Reel
NTMFS5C404NLT3G	5C404L	DFN5 (Pb–Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DFN5 5x6, 1.27P (SO−8FL)
CASE 506EZ
ISSUE A

SCALE 2:1

DATE 25 AUG 2021

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

PIN 1
IDENTIFIER
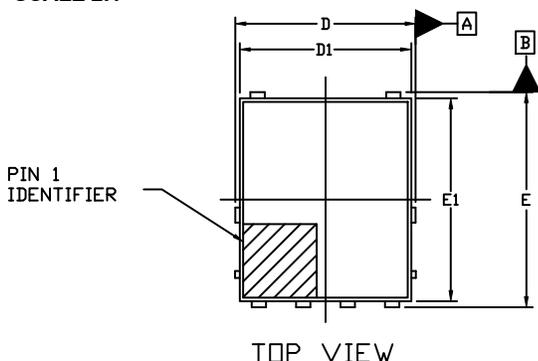
TOP VIEW
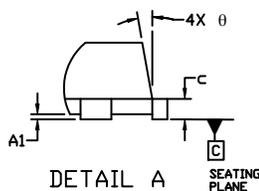
DETAIL A

SIDE VIEW

BOTTOM VIEW

PIN 5
(EXPOSED PAD)

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.80	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
k	1.10	1.20	1.40
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

**GENERIC
MARKING DIAGRAM***

XXXXXX
AYWZZ

XXXXXX = Specific Device Code
A   = Assembly Location
Y   = Year
W   = Work Week
ZZ   = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪ ", may or may not be present. Some products may not follow the Generic Marking.
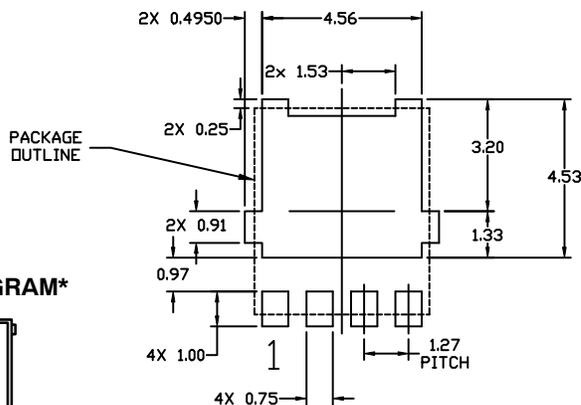
RECOMMENDED
MOUNTING FOOTPRINT

PACKAGE
OUTLINE

2X 0.4950
4.56
2x 1.53
2X 0.25
3.20
4.53
2X 0.91
1.33
0.97
4X 1.00
1.27 PITCH
4X 0.75

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON24855H	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	DFN5 5x6, 1.27P (SO−8FL)		PAGE 1 OF 1

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical–documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

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