# 24-Bit, 96-/192-kHz, Asynchronous, 4-Channel/4-Channel Audio Codec with 2-$V_{RMS}$ Driver, Headphone Driver, and 6 Audio Interface Ports

**Check for Samples: PCM5310**

## FEATURES

- **2- or 2.4-$V_{RMS}$ Output (Typ), 2-$V_{RMS}$ Input (Typ)**
- **Asynchronous Operation for 2 Stereo DACs and 2 Stereo ADCs**
- **6 Audio Interface Ports with Mux and Bypass**
- **Performance:**
  - **THD+N ($f_S$ = 48 kHz): 0.01% (ADC), 0.01% (DAC)**
  - **SNR/DR ($f_S$ = 48 kHz): 95 dB (ADC), 100 dB (DAC)**
  - **Line Input (Stereo x6): Available for 2-$V_{RMS}$ Input**
  - **Line Output (Stereo x2): Available for 2-$V_{RMS}$ or 2.4-$V_{RMS}$ Output**
  - **Headphone Output: > 20 mW into 32 Ω, > 30 mW into 16 Ω**
  - **Sampling Rate: 96 kHz (ADC), 192 kHz (DAC)**
  - **System Clock: 128 $f_S$, 192 $f_S$, 256 $f_S$, 384 $f_S$, 512 $f_S$, 768 $f_S$**
  - **Digital Filter Passband Ripple: ±0.05 dB (ADC), ±0.04 dB (DAC)**
  - **Digital Filter Stop Band Attenuation: –65 dB (ADC), –50 dB (DAC)**
- **$I^2C$™ Interface**
- **Multifunctions:**
  - **Audio Interface: $I^2S$™, Left-Justified, and Right-Justified**
  - **Digital Attenuation: 0 dB to –100 dB in 0.5-dB Steps (DAC), 20 dB to –100 dB in 0.5-dB Steps (ADC)**
  - **Digital Soft Mute: 1.0-dB Steps to Mute**
  - **Digital De-Emphasis Filter: 32, 44.1, 48 kHz**
  - **Digital Audio Interface Mux and Bypass**
  - **Line Input Level Control: 9, 6, 3, 0 dB**
  - **Line Output Level Control: 0, –0.5, –1.0 dB**
  - **Headphone Output Volume Control: 12 dB to –70 dB in 1-dB Steps**
  - **Oversampling Rate Control for DAC**
- **Power-Supply Voltage:**
  - **9 V for 2-$V_{RMS}$ Driver**
  - **3.3 V for Digital and Analog**
- **Power Consumption:**
  - **360 mW at $f_S$ = 48-kHz Operation**
  - **25.5 µW in Power-Down Mode**
- **Pop Noise Reduction at Clock Halt**
- **Short-Circuit Protection for Headphone Output**
- **Flexible GPIO Port:**
  - **Internal Mute Flag**
  - **Internal Zero Flag**
  - **Headphone Insertion Detection Status**
  - **Headphone Short-Circuit Protection Status**
  - **Logic Functions (AND, NAND, OR, NOR, BUF, INV)**
- **Package: 64-Pin HTQFP PowerPAD™**
- **Operating Temperature Range:–25°C to +85°C**

## APPLICATIONS

- **Digital TV**
- **DVD Recorder**
- **IP-STB (Set Top Box)**

## DESCRIPTION

The PCM5310 is a four-channel/four-channel audio codec with a 2-$V_{RMS}$ driver, headphone amplifier, analog multiplexer (mux), and six audio interface ports for digital TV applications.

The PCM5310 accepts left-justified, right-justified, and $I^2S$ audio data formats with 16 or 24 bits. The PCM5310 also incorporates many functions through the $I^2C$ interface, such as an analog bypass mode, analog volume control, analog level control, analog multiplexer, GPIO, zero flag, short protection, de-emphasis filter, high-pass filter, and digital attenuator. The six audio interface ports each have a built-in digital mux and bypass functions to reduce the need for additional DSP ports or other devices.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGING/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

| | | PCM5310 | UNIT |
|---|---|---|---|
| Supply voltage | $V_{CCDA}$, $V_{CCAD}$, $V_{CCP}$, $V_{DD}$ | –0.3 to 4.0 | V |
| | $V_{CCH}$ | –0.3 to 10 | V |
| Ground voltage differences: AGNDAD, AGNDDA, PGND, HGND, DGND | | ±0.1 | V |
| Input voltage | | –0.3 to 4.0 | V |
| Input current (all pins except supplies) | | ±10 | mA |
| Ambient temperature under bias | | –40 to +125 | °C |
| Storage temperature | | –55 to +150 | °C |
| Junction temperature | | +150 | °C |
| Lead temperature (soldering, 5s) | | +260 | °C |
| Package temperature (IR reflow, peak) | | +260 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Analog supply voltage, $V_{CCAD}$, $V_{CCDA}$, $V_{CCP}$ | | 3.0 | 3.3 | 3.6 | V |
| Analog supply voltage, $V_{CCH}$ | | 8.55 | 9 | 9.45 | V |
| Digital supply voltage, $V_{DD}$ | | 3.0 | 3.3 | 3.6 | V |
| Analog input voltage, full-scale (–0 dB) | | | 2 | | $V_{RMS}$ |
| Analog output voltage, full-scale (–0 dB) | | | 2 | 2.4 | $V_{RMS}$ |
| Digital input logic family | | | CMOS | | |
| Digital input clock frequency | ADC system clock | 4.096 | | 36.864 | MHz |
| | ADC sampling clock | 32 | | 96 | kHz |
| | DAC system clock | 4.096 | | 36.864 | MHz |
| | DAC sampling clock | 32 | | 192 | kHz |
| Analog output load resistance | | 10 | | | kΩ |
| Analog output load capacitance | | | 30 | | pF |
| Digital output load capacitance | | | 10 | | pF |
| Operating free-air temperature, $T_A$ | | –25 | | +85 | °C |

## ELECTRICAL CHARACTERISTICS

All specifications at $T_A$ = +25°C, $V_{DD}$ = $V_{CCAD}$ = $V_{CCDA}$ = $V_{CCP}$ = 3.3 V, $V_{CCH}$ = 9 V, $f_S$ (1) = 48 kHz, system clock = 256 $f_S$, and 24-bit data, unless otherwise noted.

| PARAMETER | | | TEST CONDITIONS | PCM5310 MIN | PCM5310 TYP | PCM5310 MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **AUDIO DATA** | | | | | | | |
| **Data Format** | | | | | | | |
| | Audio data bit length | | | | 16, 24 | | Bits |
| | Audio data interface format | | | | $I^2S$, left-justified, right-justified | | |
| | Audio data format | | | | MSB, twos complement | | |
| | Sampling frequency | ADC | | | | 108 | kHz |
| | | DAC | | | | 216 | kHz |
| | System clock | ADC | | | 256 $f_S$, 384 $f_S$, 512 $f_S$, 768 $f_S$ | | MHz |
| | | DAC | | | 128 $f_S$, 192 $f_S$, 256 $f_S$, 384 $f_S$, 512 $f_S$, 768 $f_S$ | | MHz |
| | Bit clock | ADC | | | 48 $f_S$, 64 $f_S$ | | MHz |
| | | DAC | | | 32 $f_S$, 48 $f_S$, 64 $f_S$ | | MHz |
| **DIGITAL INPUT/OUTPUT** | | | | | | | |
| | Logic family | | | | CMOS-compatible | | |
| $V_{IH}$ | Input logic high level | | | 0.7 $V_{DD}$ | | | V |
| $V_{IL}$ | Input logic low level | | | | | 0.3 $V_{DD}$ | V |
| $I_{IH}$ | Input logic high current | | | | | 10 | µA |
| $I_{IL}$ | Input logic low current | | | | | –10 | µA |
| $V_{OH}$ | Output logic high level | | $I_{OH}$ = 2 mA | 0.75 $V_{DD}$ | | | V |
| $V_{OL}$ | Output logic low level | | $I_{OH}$ = –2 mA | | | 0.25 $V_{DD}$ | V |
| **DAC LINE OUTPUT** | | | | | | | |
| **Dynamic Performance** | | | | | | | |
| | Full-scale output voltage | | Digital input = 0 dB, G242, G241 = low | | 2 | | $V_{RMS}$ |
| | | | Digital input = 0 dB, G242, G241 = high | | 2.4 | | $V_{RMS}$ |
| | Dynamic range | | EIAJ, A-weighted | 90 | 100 | | dB |
| SNR | Signal-to-noise ratio | | EIAJ, A-weighted | 90 | 100 | | dB |
| | Channel separation | | | 88 | 97 | | dB |
| THD+N | Total harmonic distortion + noise | | Digital input = 0 dB, G242, G241 = low | | 0.01 | 0.02 | % |
| | Load resistance | | AC load | 10 | | | kΩ |
| **DC Accuracy** | | | | | | | |
| | Gain error | | Digital input = 0 dB, G242, G241 = low | | ±3 | ±13 | % of FSR |
| | Gain mismatch, channel-to-channel | | | | ±3 | ±13 | % of FSR |
| | Bipolar zero error | | Zero data input | | ±40 | ±120 | mV |
| | Center voltage | | Zero data input | | 0.5 $V_{CCDA}$ | | V |
| **Analog Gain Control** | | | | | | | |
| | Gain range | | | | 0, –0.5, –1.0 | | dB |
| | Gain error | | | | ±0.5 | | dB |

(1) $f_S$ = sampling rate.

## ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A$ = +25°C, $V_{DD}$ = $V_{CCAD}$ = $V_{CCDA}$ = $V_{CCP}$ = 3.3 V, $V_{CCH}$ = 9 V, $f_S$ (1) = 48 kHz, system clock = 256 $f_S$, and 24-bit data, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | PCM5310 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **DAC HEADPHONE OUTPUT** | | | | | | |
| **Dynamic Performance** | | | | | | |
| | Full-scale output voltage | Digital input = 0 dB, VOL = 0dB | | 1 | | $V_{RMS}$ |
| | Dynamic range | EIAJ, A-weighted | 85 | 96 | | dB |
| SNR | Signal-to-noise ratio | EIAJ, A-weighted | 85 | 96 | | dB |
| | Channel separation | $R_L$ = 32 Ω | | 88 | | dB |
| THD+N | Total harmonic distortion + noise | $R_L$ = 32 Ω, VOL = 0 dB | | 0.1 | 0.18 | % |
| | | $R_L$ = 16 Ω, VOL = 0 dB | | 1 | 3 | % |
| | Load resistance | | 16 | | | Ω |
| **DC Accuracy** | | | | | | |
| | Gain error | Digital input = 0 dB, VOL = 0dB | | ±3 | ±13 | % of FSR |
| | Gain mismatch, channel-to-channel | | | ±3 | ±13 | % of FSR |
| | Bipolar zero error | Zero data input | | ±27 | ±80 | mV |
| | Center voltage | Zero data input | | 0.5 $V_{CCDA}$ | | V |
| **Analog Volume** | | | | | | |
| | Gain range | | –70 | | 12 | dB |
| | Gain error | | | 0.5 | | dB |
| | Gain step | | | 1.0 | | dB |
| **ADC LINE INPUT** | | | | | | |
| **Dynamic Performance** | | | | | | |
| | Full-scale input voltage | Digital input = 0 dB, VOL = 0dB | | 2 | | $V_{RMS}$ |
| | Dynamic range | EIAJ, A-weighted | 85 | 95 | | dB |
| SNR | Signal-to-noise ratio | EIAJ, A-weighted | 85 | 95 | | dB |
| | Channel separation | | | 93 | | dB |
| THD+N | Total harmonic distortion + noise | Analog input = –1 dB, VOL = 0dB | | 0.01 | 0.018 | % |
| **DC Accuracy** | | | | | | |
| | Gain error | Analog input = 0 dB, VOL = 0dB | | ±3 | ±13 | % of FSR |
| | Gain mismatch, channel-to-channel | | | ±3 | ±13 | % of FSR |
| | Bipolar zero error | Zero data input | | ±17 | ±50 | mV |
| | Center voltage | Zero data input | | 0.5 $V_{CCAD}$ | | V |
| **Analog Input** | | | | | | |
| | Input impedance | | 37.6 | 47 | 56.4 | kΩ |
| **Analog Gain Control** | | | | | | |
| | Gain range | | | 9, 6, 3, 0 | | dB |
| | Gain error | | | ±0.5 | | dB |

## ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A$ = +25°C, $V_{DD}$ = $V_{CCAD}$ = $V_{CCDA}$ = $V_{CCP}$ = 3.3 V, $V_{CCH}$ = 9 V, $f_S$ (1) = 48 kHz, system clock = 256 $f_S$, and 24-bit data, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | PCM5310 MIN | PCM5310 TYP | PCM5310 MAX | UNIT |
|---|---|---|---|---|---|---|
| **ANALOG INPUT TO ANALOG OUTPUT PATH (BYPASS)** | | | | | | |
| **Dynamic Performance** | | | | | | |
| | Full-scale input voltage | Analog input = 0 dB, VOL = 0dB | | 2 | | $V_{RMS}$ |
| | Full-scale output voltage | Analog input = 0 dB, G242, G241 = low | | 2 | | $V_{RMS}$ |
| | Dynamic range | EIAJ, A-weighted | 90 | 100 | | dB |
| SNR | Signal-to-noise ratio | EIAJ, A-weighted | 90 | 100 | | dB |
| | Channel separation | | 88 | 97 | | dB |
| THD+N | Total harmonic distortion + noise | Analog input = 0 dB, G242, G241 = low | | 0.003 | 0.006 | % |
| **DC Accuracy** | | | | | | |
| | Gain error | Analog input = 0 dB, G242, G241 = low | | ±3 | ±13 | % of FSR |
| | Gain mismatch, channel-to-channel | | | 3 | ±13 | % of FSR |
| | Bipolar zero error | Zero data input | | ±20 | ±60 | mV |
| | Center voltage, analog input | Zero data input | | 0.5 $V_{CCAD}$ | | V |
| | Center voltage, analog output | Zero data input | | 0.5 $V_{CCDA}$ | | V |
| **Analog Input** | | | | | | |
| | Input impedance | | 37.6 | 47 | 56.4 | kΩ |
| **FILTERS** | | | | | | |
| **Interpolation Filters for DAC** | | | | | | |
| | Passband | | | | 0.454 $f_S$ | kHz |
| | Stop band | | 0.546 $f_S$ | | | kHz |
| | Passband ripple | | | | ±0.04 | dB |
| | Stop-band attenuation | | –50 | | | dB |
| | Group delay | | | 20/$f_S$ | | s |
| | De-emphasis error | | | ±0.1 | | dB |
| **Analog Filter for DAC** | | | | | | |
| | Frequency response | $f_C$ = 20 kHz | | ±0.1 | | dB |
| | Cutoff frequency | Gain = –3 dB | | 190 | | kHz |
| **Decimation Filter for ADC** | | | | | | |
| | Passband | | | | 0.454 $f_S$ | kHz |
| | Stop band | | 0.583 $f_S$ | | | kHz |
| | Passband ripple | | | | ±0.05 | dB |
| | Stop-band attenuation | | –65 | | | dB |
| | Group delay | | | 17.4/$f_S$ | | s |
| **Analog Filter for ADC** | | | | | | |
| | Frequency response | $f_C$ = 20 kHz | | ±0.01 | | dB |
| | Cutoff frequency | Gain = –3 dB | | 500 | | kHz |
| **High-Pass Filter for ADC** | | | | | | |
| | Frequency response | Gain = –3 dB | | 0.91 | | Hz |

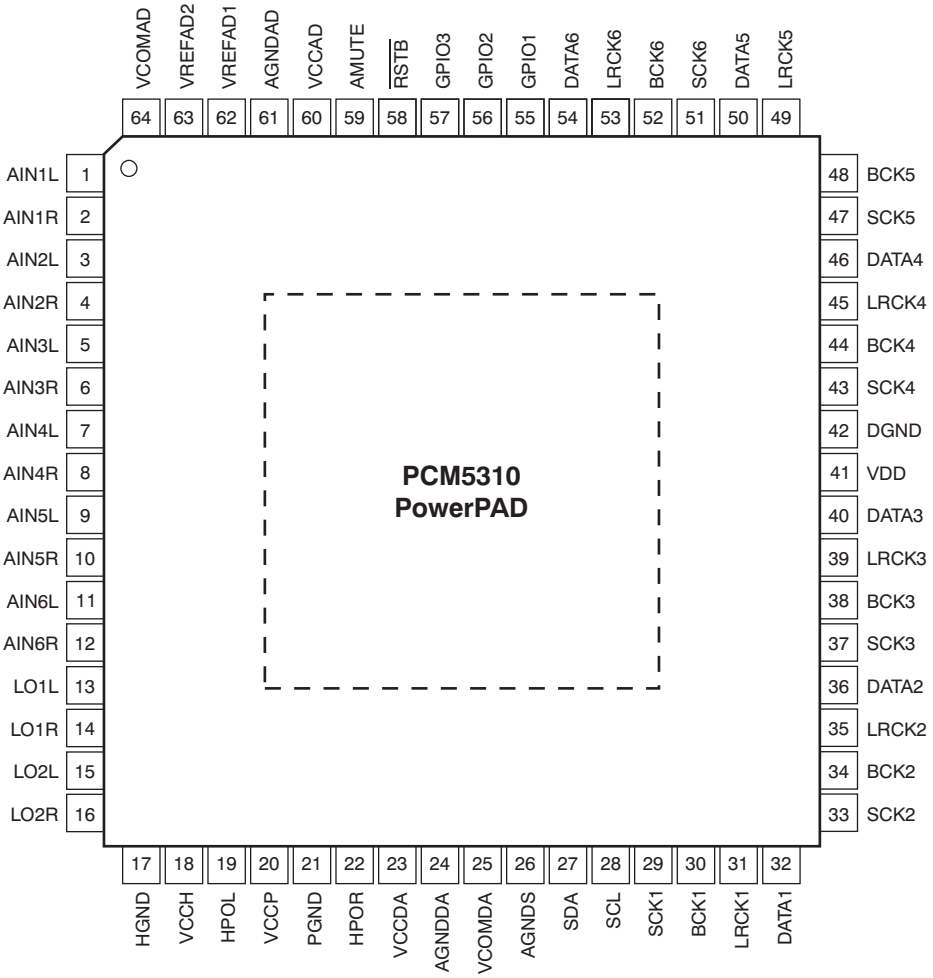
## ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A$ = +25°C, $V_{DD}$ = $V_{CCAD}$ = $V_{CCDA}$ = $V_{CCP}$ = 3.3 V, $V_{CCH}$ = 9 V, $f_S$ (1) = 48 kHz, system clock = 256 $f_S$, and 24-bit data, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | PCM5310 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **POWER-SUPPLY REQUIREMENTS** | | | | | | |
| $V_{DD}$ | Digital voltage range | | 3 | 3.3 | 3.6 | V |
| $V_{CCAD}$ | DAC voltage range | | 3 | 3.3 | 3.6 | V |
| $V_{CCDA}$ | ADC voltage range | | 3 | 3.3 | 3.6 | V |
| $V_{CCP}$ | Headphone driver voltage range | | 3 | 3.3 | 3.6 | V |
| $V_{CCH}$ | 2-$V_{RMS}$ driver voltage range | | 8.55 | 9 | 9.45 | V |
| | Supply current | Zero data input, all active | | 98 | 120 | mA |
| | | All power-down | | 6 | 100 | µA |
| | Power dissipation | Zaro data input, all active | | 360 | 450 | mW |
| | | All power-down | | 25.5 | 350 | µW |
| **TEMPERATURE RANGE** | | | | | | |
| | Operating temperature range | | –25 | | +85 | °C |
| $\theta_{JA}$ | Thermal resistance | HTQFP-64 | | 21 | | °C/W |

## PIN ASSIGNMENTS

**PAP PACKAGE**
**HTQFP-64**
**(TOP VIEW)**



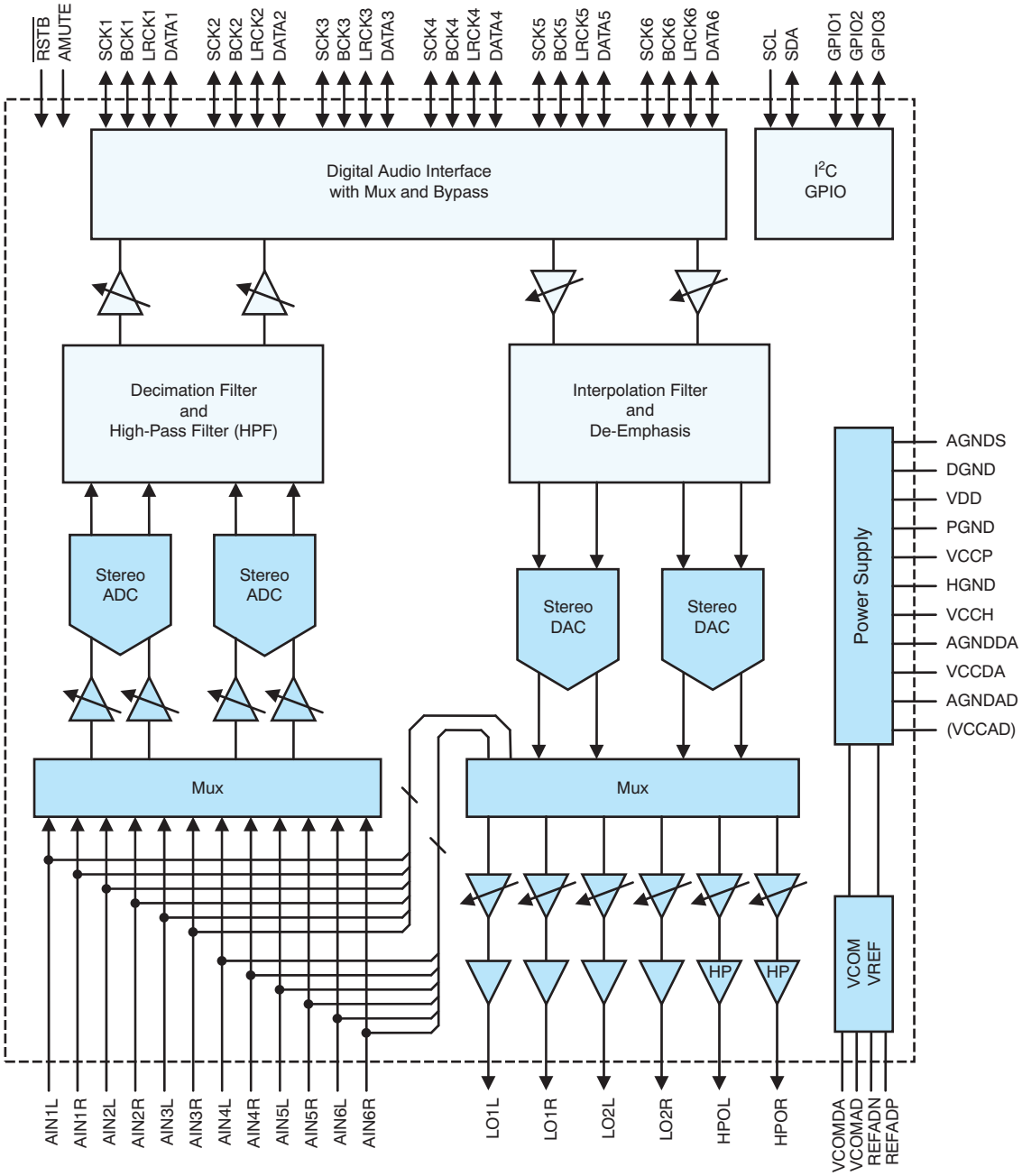

## PIN DESCRIPTIONS

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| AIN1L | 1 | I | Line input 1 L-channel |
| AIN1R | 2 | I | Line input 1 R-channel |
| AIN2L | 3 | I | Line input 2 L-channel |
| AIN2R | 4 | I | Line input 2 R-channel |
| AIN3L | 5 | I | Line input 3 L-channel |
| AIN3R | 6 | I | Line input 3 R-channel |
| AIN4L | 7 | I | Line input 4 L-channel |
| AIN4R | 8 | I | Line input 4 R-channel |
| AIN5L | 9 | I | Line input 5 L-channel |
| AIN5R | 10 | I | Line input 5 R-channel |
| AIN6L | 11 | I | Line input 6 L-channel |
| AIN6R | 12 | I | Line input 6 R-channel |
| LO1L | 13 | O | Line output 1 L-channel |
| LO1R | 14 | O | Line output 1 R-channel |

## PIN DESCRIPTIONS (continued)

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| LO2L | 15 | O | Line output 2 L-channel |
| LO2R | 16 | O | Line output 2 R-channel |
| HPOL | 19 | O | Headphone output L-channel |
| HPOR | 22 | O | Headphone output R-channel |
| VCOMDA | 25 | — | Common voltage for DAC |
| VCOMAD | 64 | — | Common voltage for ADC |
| VREFAD1 | 62 | — | Reference voltage 1 for ADC |
| VREFAD2 | 63 | — | Reference voltage 2 for ADC |
| VCCAD | 60 | — | Power supply for ADC (3.3-V typical) |
| AGNDAD | 61 | — | Ground for ADC |
| VCCDA | 23 | — | Power supply for DAC (3.3-V typical) |
| AGNDDA | 24 | — | Ground for DAC |
| VCCP | 20 | — | Power supply for headphone (3.3-V typical) |
| PGND | 21 | — | Ground for headphone |
| VDD | 41 | — | Power supply for digital (3.3-V typical) |
| DGND | 42 | — | Digital ground |
| VCCH | 18 | — | Power supply for 2-$V_{RMS}$ driver (9.0-V typical) |
| HGND | 17 | — | Ground for 2-$V_{RMS}$ driver |
| AGNDS | 26 | — | Analog ground |
| SCK1 | 29 | I/O | PORT-1 system clock |
| BCK1 | 30 | I/O | PORT-1 serial bit clock |
| LRCK1 | 31 | I/O | PORT-1 left and right channel clock |
| DATA1 | 32 | I/O | PORT-1 serial audio data |
| SCK2 | 33 | I/O | PORT-2 system clock |
| BCK2 | 34 | I/O | PORT-2 serial bit clock |
| LRCK2 | 35 | I/O | PORT-2 left and right channel clock |
| DATA2 | 36 | I/O | PORT-2 serial audio data |
| SCK3 | 37 | I/O | PORT-3 system clock |
| BCK3 | 38 | I/O | PORT-3 serial bit clock |
| LRCK3 | 39 | I/O | PORT-3 left and right channel clock |
| DATA3 | 40 | I/O | PORT-3 serial audio data |
| SCK4 | 43 | I/O | PORT-4 system clock |
| BCK4 | 44 | I/O | PORT-4 serial bit clock |
| LRCK4 | 45 | I/O | PORT-4 left and right channel clock |
| DATA4 | 46 | I/O | PORT-4 serial audio data |
| SCK5 | 47 | I/O | PORT-5 system clock |
| BCK5 | 48 | I/O | PORT-5 serial bit clock |
| LRCK5 | 49 | I/O | PORT-5 left and right channel clock |
| DATA5 | 50 | I/O | PORT-5 serial audio data |
| SCK6 | 51 | I/O | PORT-6 system clock |
| BCK6 | 52 | I/O | PORT-6 serial bit clock |
| LRCK6 | 53 | I/O | PORT-6 left and right channel clock |
| DATA6 | 54 | I/O | PORT-6 serial audio data |
| SCL | 28 | I | Clock for $I^2C$ interface |
| SDA | 27 | I/O | Data for $I^2C$ interface |
| GPIO1 | 55 | I/O | General-purpose input and output 1 |
| GPIO2 | 56 | I/O | General-purpose input and output 2 |
| GPIO3 | 57 | I/O | General-purpose input and output 3 |
| $\overline{\text{RSTB}}$ | 58 | I | Reset (active low) |
| AMUTE | 59 | I | Analog mute control for all analog outputs (active high) |

## FUNCTIONAL BLOCK DIAGRAM



## TYPICAL CHARACTERISTICS: Digital Filter (DAC) Sharp, Slow

All specifications at $T_A$ = +25°C, $V_{DD}$ = $V_{CCAD}$ = $V_{CCDA}$ = $V_{CCP}$ = 3.3 V, $V_{CCH}$ = 9 V, $f_S$ = 48 kHz, system clock = 256 $f_S$, and 24-bit data, unless otherwise noted.

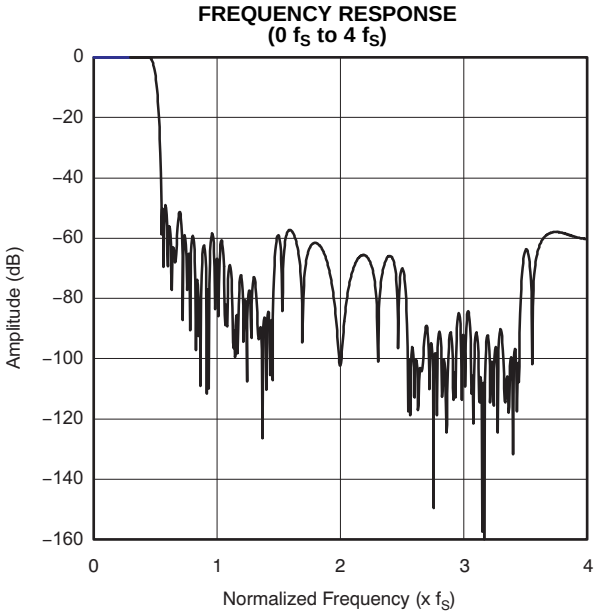



**Figure 1.**

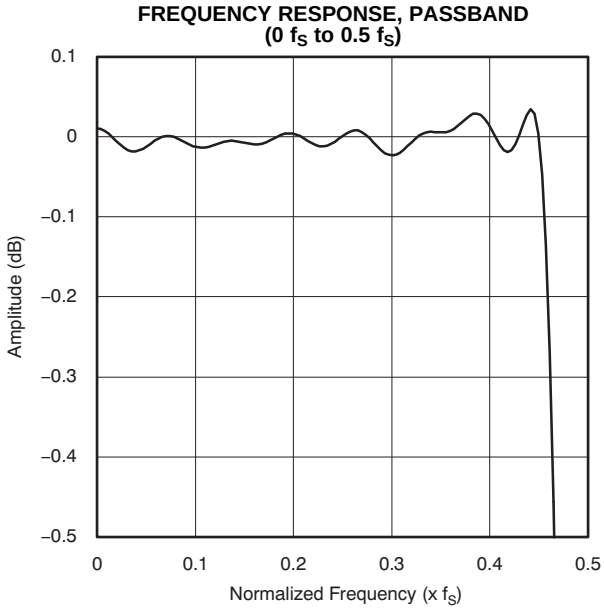



**Figure 2.**

## TYPICAL CHARACTERISTICS: Analog Filter (DAC)

All specifications at $T_A$ = +25°C, $V_{DD}$ = $V_{CCAD}$ = $V_{CCDA}$ = $V_{CCP}$ = 3.3 V, $V_{CCH}$ = 9 V, $f_S$ = 48 kHz, system clock = 256 $f_S$, and 24-bit data, unless otherwise noted.

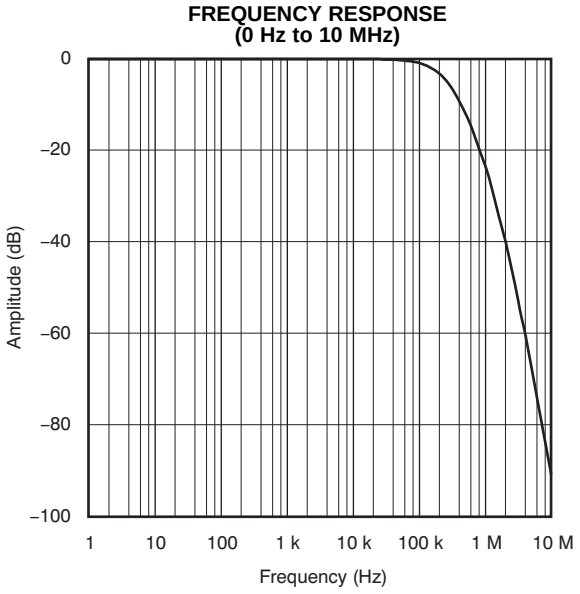



**Figure 3.**

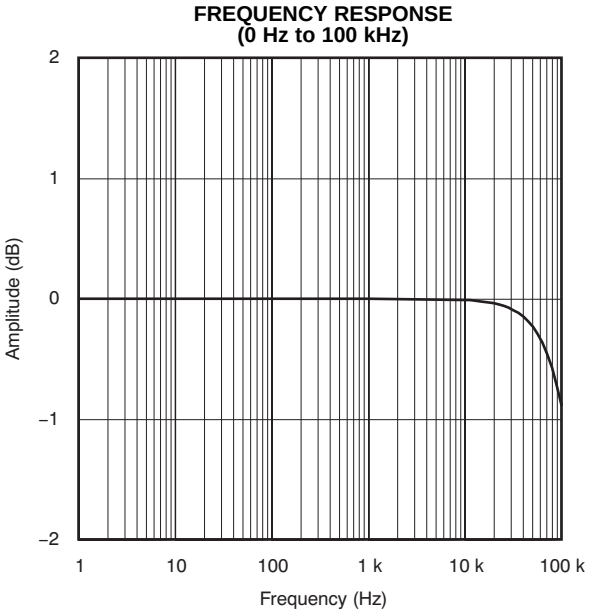



**Figure 4.**

## TYPICAL CHARACTERISTICS: Digital Filter (ADC)

All specifications at $T_A$ = +25°C, $V_{DD}$ = $V_{CCAD}$ = $V_{CCDA}$ = $V_{CCP}$ = 3.3 V, $V_{CCH}$ = 9 V, $f_S$ = 48 kHz, system clock = 256 $f_S$, and 24-bit data, unless otherwise noted.

**FREQUENCY RESPONSE**
**(0 $f_S$ to 32 $f_S$)**

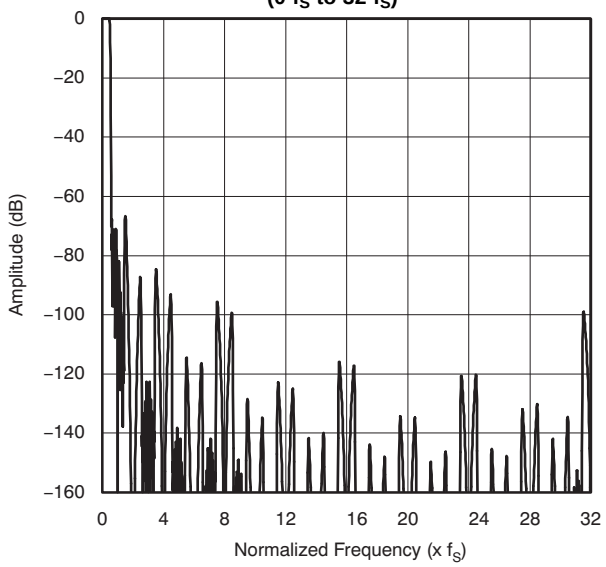



**Figure 5.**

**FREQUENCY RESPONSE, PASSBAND**
**(0 $f_S$ to 0.5 $f_S$)**

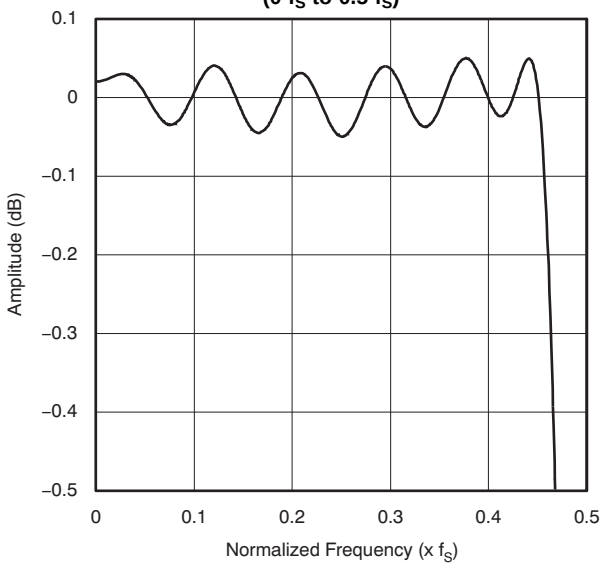



**Figure 6.**

**HIGH-PASS FILTER RESPONSE**
**(0 $f_S$ to 0.4 $f_S$)**

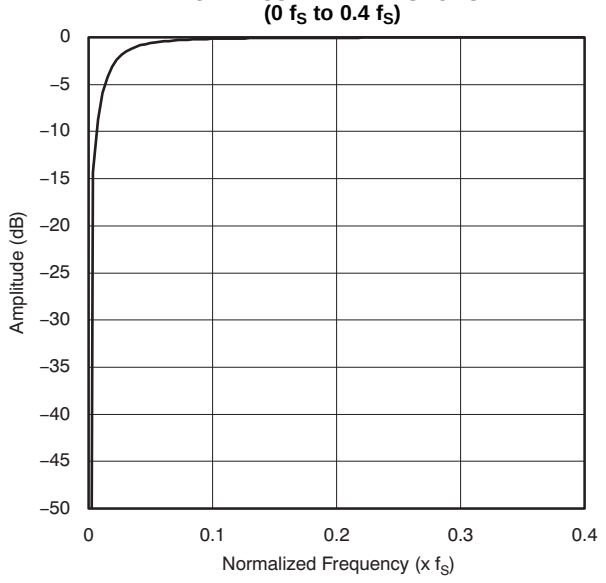



**Figure 7.**

**HIGH-PASS FILTER RESPONSE**
**(0 $f_S$ to 0.1 $f_S$)**

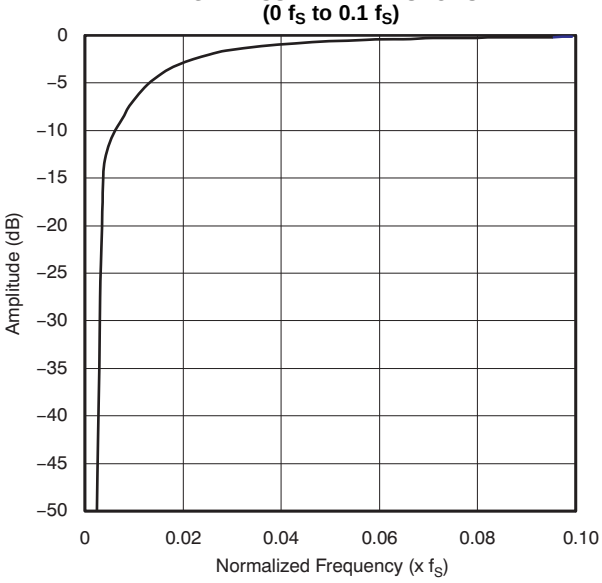



**Figure 8.**

## TYPICAL CHARACTERISTICS: Analog Performance (DAC)

All specifications at $T_A$ = +25°C, $V_{DD}$ = $V_{CCAD}$ = $V_{CCDA}$ = $V_{CCP}$ = 3.3 V, $V_{CCH}$ = 9 V, $f_S$ = 48 kHz, system clock = 256 $f_S$, and 24-bit data, unless otherwise noted.

**TOTAL HARMONIC DISTORTION + NOISE vs $V_{CC}$ SUPPLY VOLTAGE**

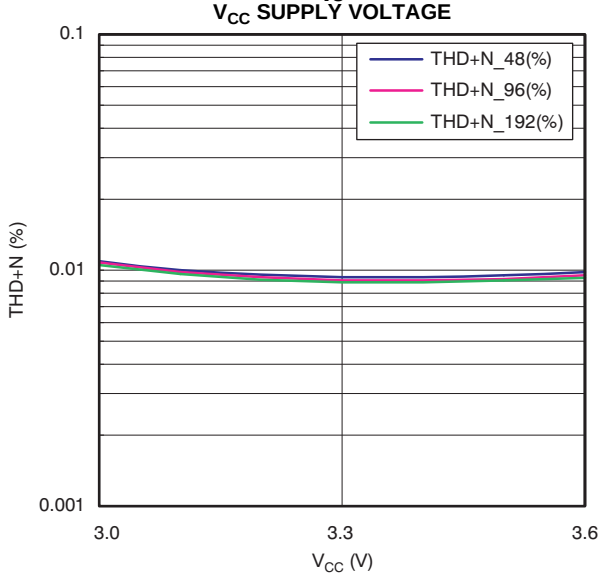



**Figure 9.**

**SIGNAL-TO-NOISE RATIO AND DATA RATE vs $V_{CC}$ SUPPLY VOLTAGE**

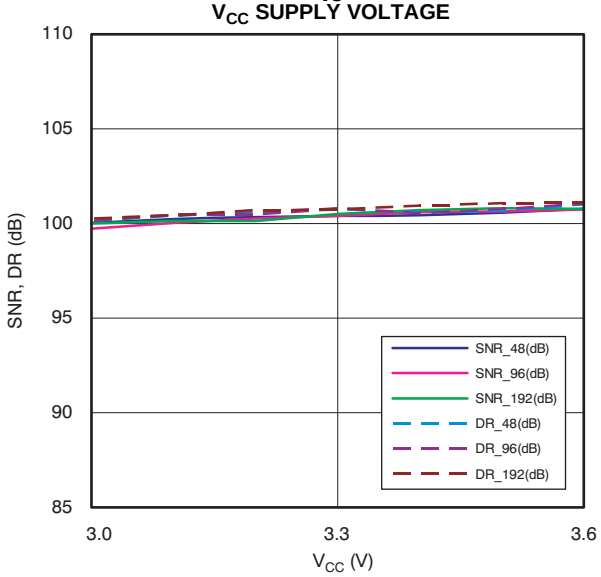



**Figure 10.**

**TOTAL HARMONIC DISTORTION + NOISE vs TEMPERATURE**

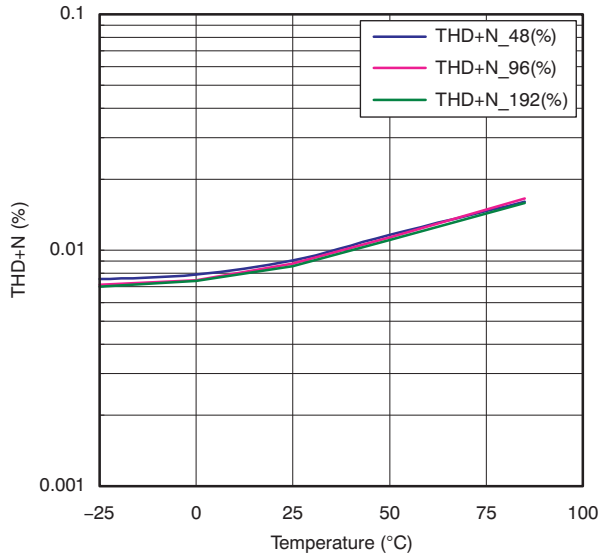



**Figure 11.**

**SIGNAL-TO-NOISE RATIO AND DATA RATE vs TEMPERATURE**

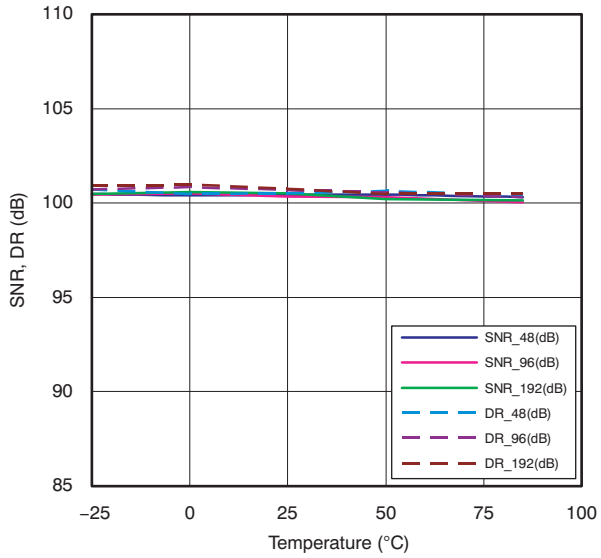



**Figure 12.**

## TYPICAL CHARACTERISTICS: Analog Performance (ADC)

All specifications at $T_A$ = +25°C, $V_{DD}$ = $V_{CCAD}$ = $V_{CCDA}$ = $V_{CCP}$ = 3.3 V, $V_{CCH}$ = 9 V, $f_S$ = 48 kHz, system clock = 256 $f_S$, and 24-bit data, unless otherwise noted.

**TOTAL HARMONIC DISTORTION + NOISE vs $V_{CC}$ SUPPLY VOLTAGE**

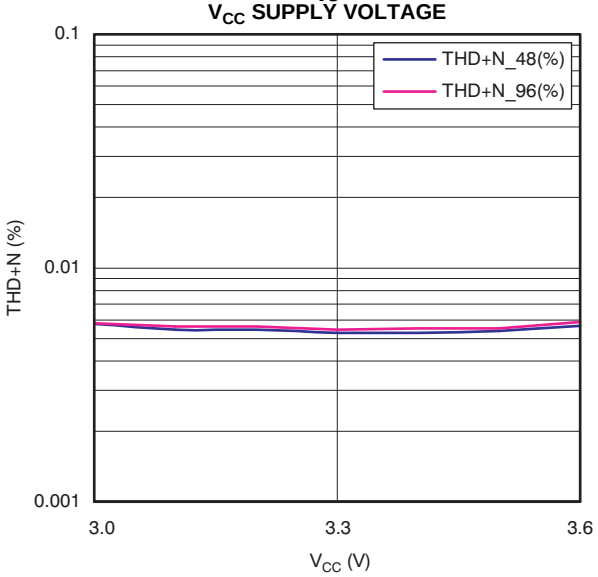



**Figure 13.**

**SIGNAL-TO-NOISE RATIO AND DATA RATE vs $V_{CC}$ SUPPLY VOLTAGE**

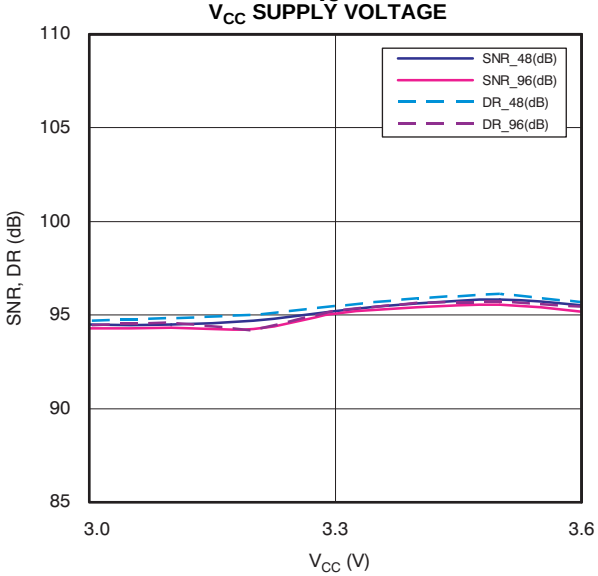



**Figure 14.**

**TOTAL HARMONIC DISTORTION + NOISE vs TEMPERATURE**

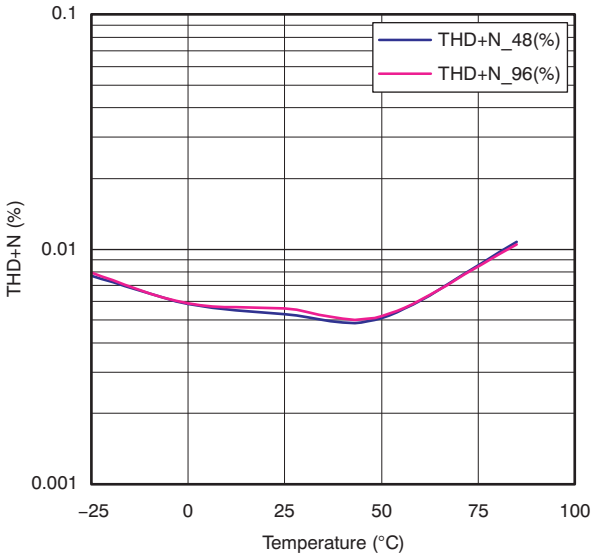



**Figure 15.**

**SIGNAL-TO-NOISE RATIO AND DATA RATE vs TEMPERATURE**

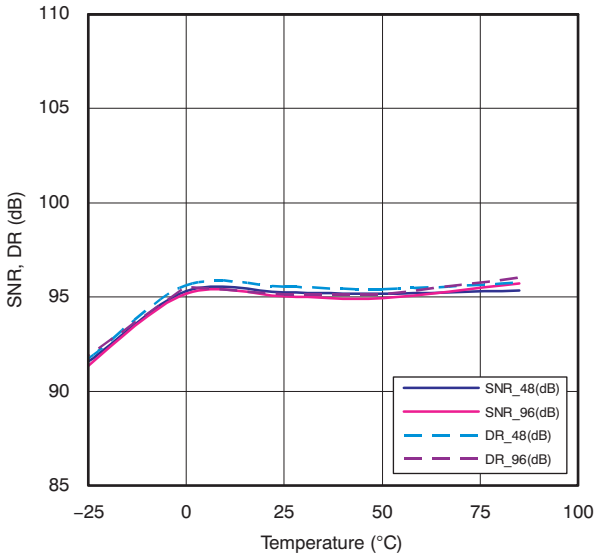



**Figure 16.**

## TYPICAL CHARACTERISTICS: Analog Performance (Headphone)

All specifications at $T_A$ = +25°C, $V_{DD}$ = $V_{CCAD}$ = $V_{CCDA}$ = $V_{CCP}$ = 3.3 V, $V_{CCH}$ = 9 V, $f_S$ = 48 kHz, system clock = 256 $f_S$, and 24-bit data, unless otherwise noted.

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (48 kHz, 16 Ω)**

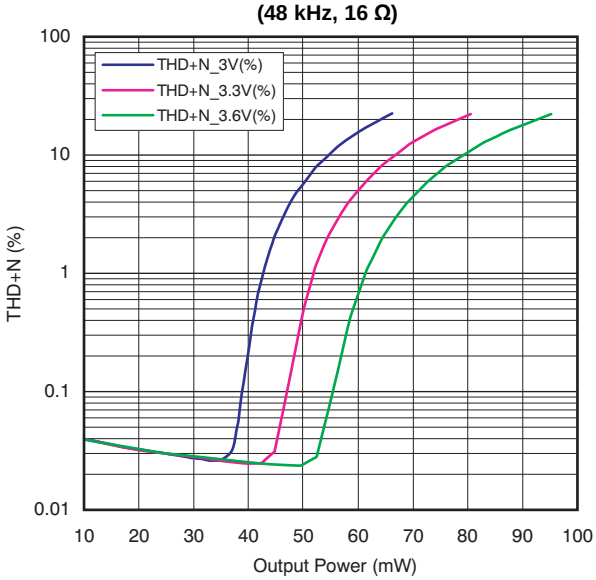



**Figure 17.**

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (48 kHz, 32 Ω)**

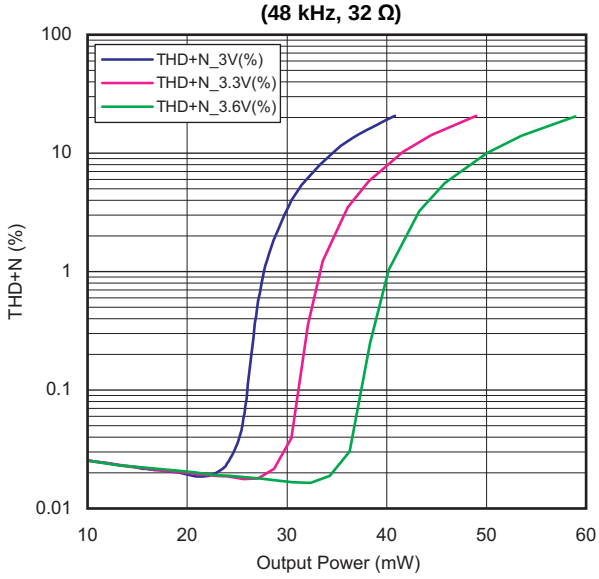



**Figure 18.**

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (48 kHz, 0 dB, 6 dB, 12 dB, 16 Ω)**

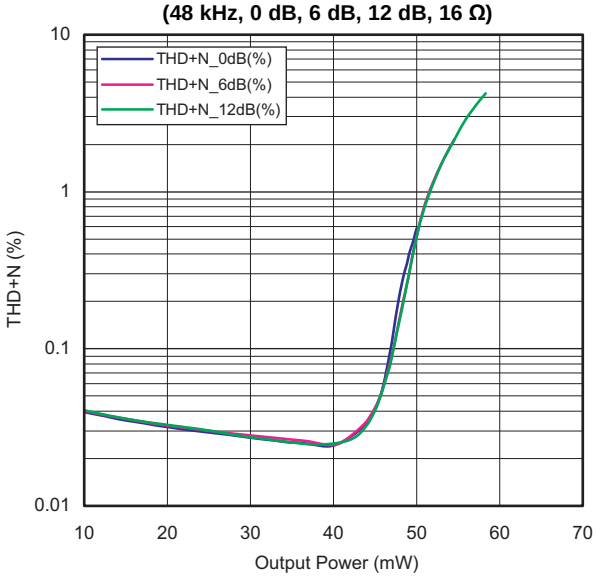



**Figure 19.**

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER (48 kHz, 0 dB, 6 dB, 12 dB, 32 Ω)**

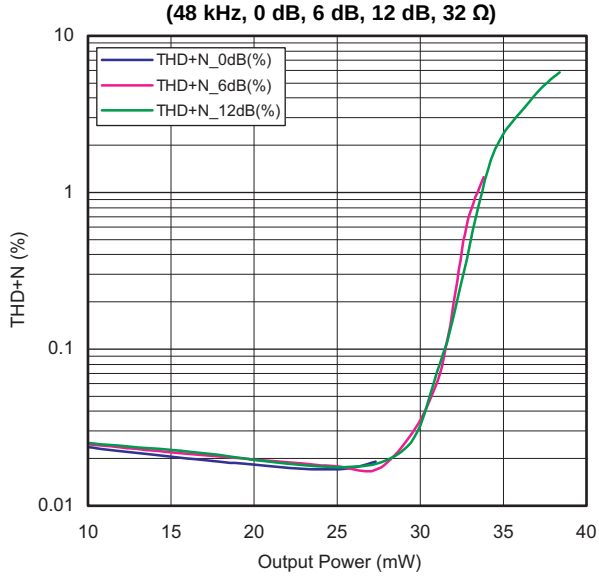



**Figure 20.**

## TYPICAL CHARACTERISTICS: Output Spectrum (DAC)

All specifications at $T_A$ = +25°C, $V_{DD}$ = $V_{CCAD}$ = $V_{CCDA}$ = $V_{CCP}$ = 3.3 V, $V_{CCH}$ = 9 V, $f_S$ = 48 kHz, system clock = 256 $f_S$, and 24-bit data, unless otherwise noted.

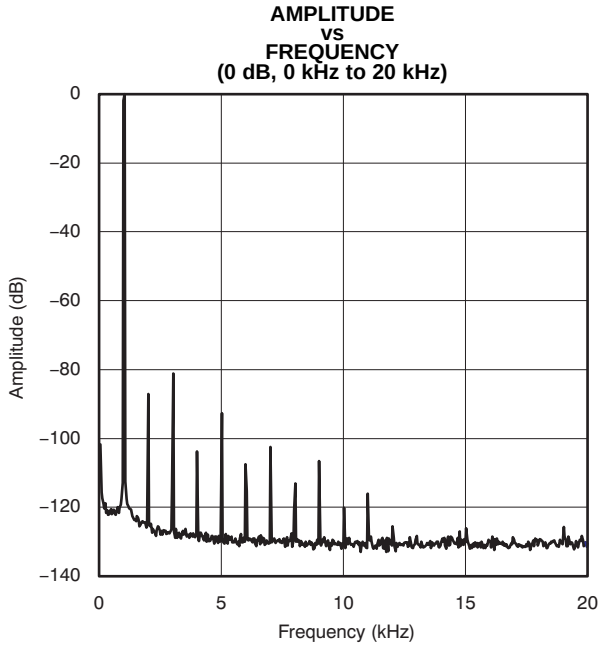



**Figure 21.**

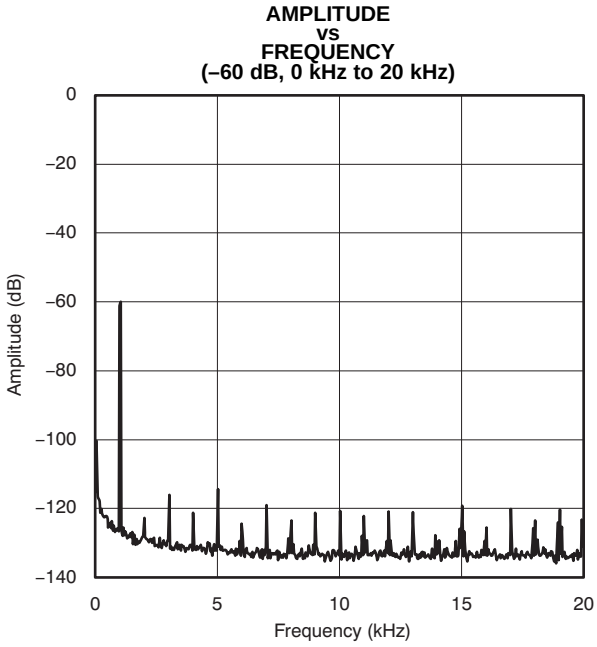



**Figure 22.**

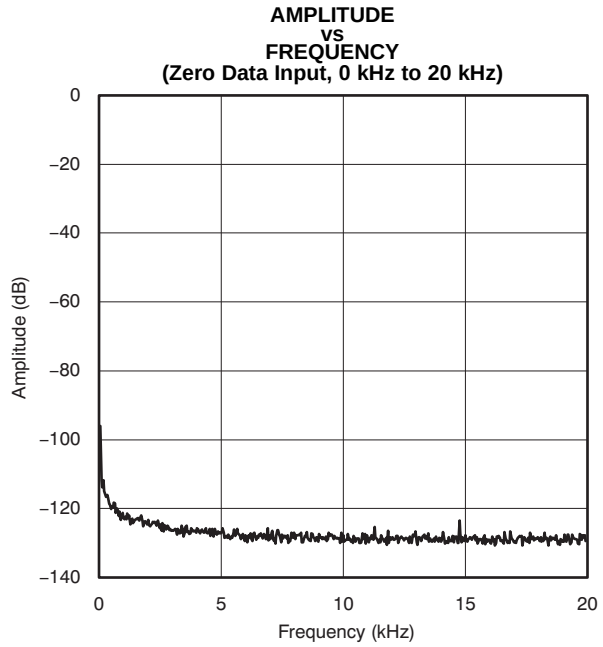



**Figure 23.**

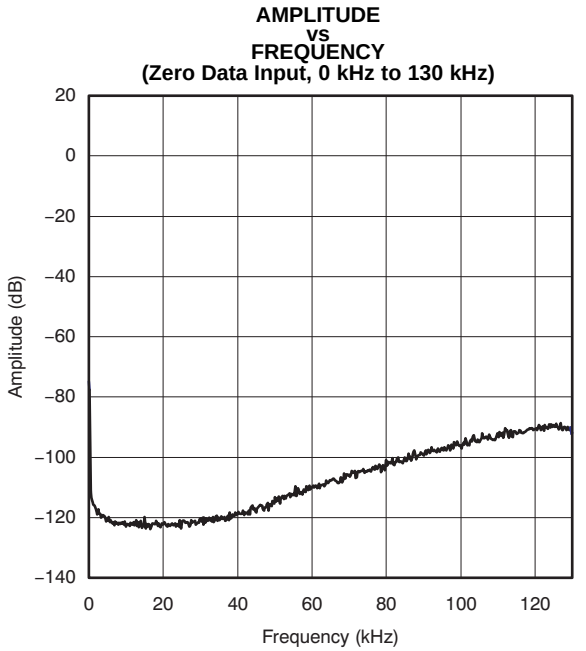



**Figure 24.**

## TYPICAL CHARACTERISTICS: Output Spectrum (ADC)

All specifications at $T_A$ = +25°C, $V_{DD}$ = $V_{CCAD}$ = $V_{CCDA}$ = $V_{CCP}$ = 3.3 V, $V_{CCH}$ = 9 V, $f_S$ = 48 kHz, system clock = 256 $f_S$, and 24-bit data, unless otherwise noted.

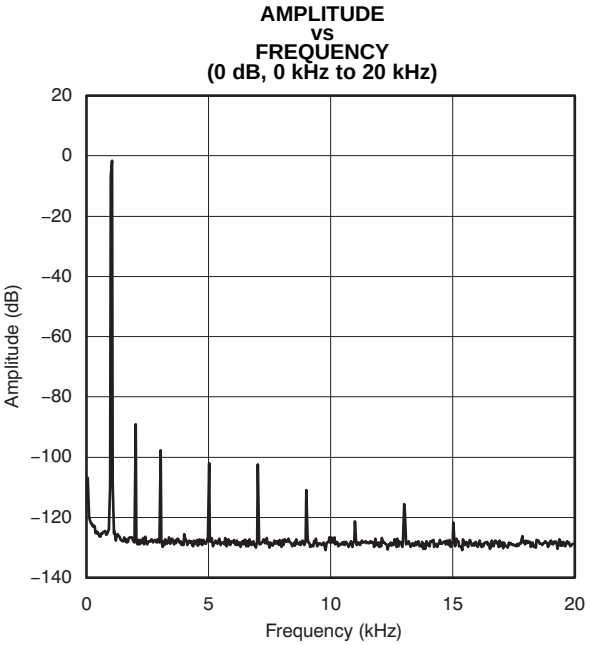



**Figure 25.**

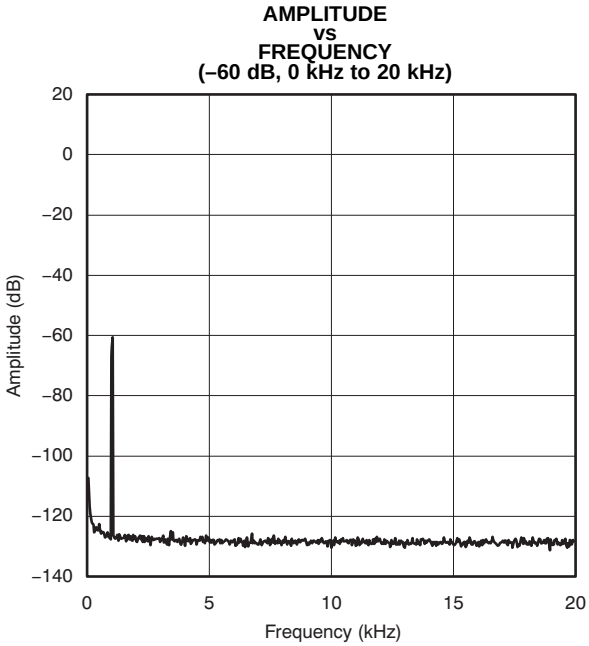



**Figure 26.**

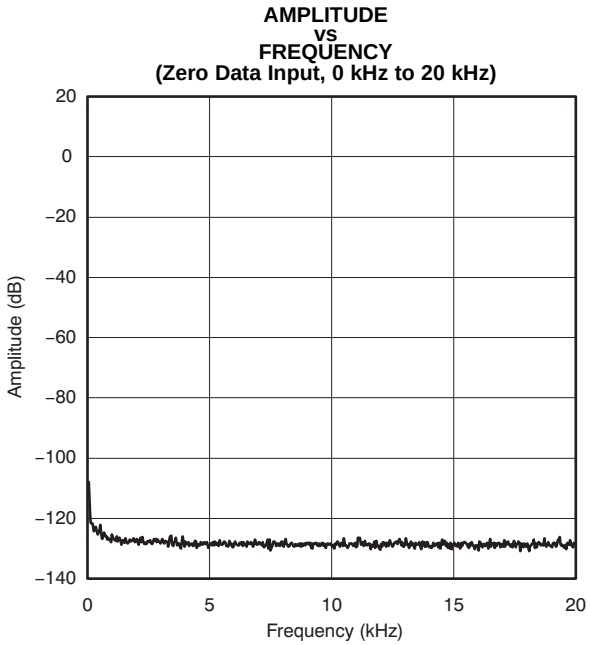



**Figure 27.**

# DETAILED DESCRIPTION

## ANALOG INPUTS

The PCM5310 includes a four-channel analog-to-digital converter (ADC) with a programmable gain amplifier (PGA) and six stereo analog inputs with a 2-$V_{RMS}$ input. Pins AIN1L/1R to AIN6L/6R are connected to the ADC left (L) or right ®) channel through the analog multiplexer (mux) and PGA, as shown in Figure 28. If the analog input voltage level is less than 2 $V_{RMS}$, it can be amplified by using the PGA. The gain level can be set to 9 dB, 6 dB, or 3 dB. The descriptions for the analog input registers are shown in Table 1.

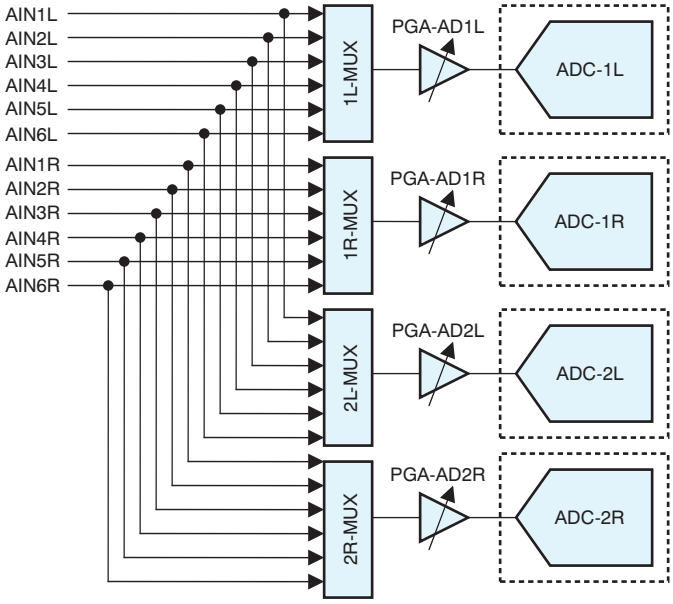



**Figure 28. Analog Inputs**

**Table 1. Analog Input Registers**

| REGISTER DESCRIPTION | REGISTER NUMBER | REGISTER BITS |
|---|---|---|
| Analog input mux selection for ADC1L/1R | 20 | AX1R[2:0], AX1L[2:0] |
| Analog input mux selection for ADC2L/2R | 21 | AX2R[2:0], AX2L[2:0] |
| Analog input gain control for ADC1L/1RW | 22 | AG1R[1:0], AG1L[1:0] |
| Analog input gain control for ADC2L/2R | 23 | AG2R[1:0], AG2L[1:0] |

## ANALOG OUTPUTS

The PCM5310 includes a four-channel digital-to-analog converter (DAC), two stereo line outputs with analog level control, a headphone output with analog volume control, and an analog multiplexer (mux) with analog direct input path. Line outputs (LO1L, LO1R, LO2L, LO2R) have a 2-$V_{RMS}$ capability without external amplifiers. If an audio application requires a higher output voltage level, the PCM5310 can achieve a 2.4-$V_{RMS}$ output.

The headphone output (HPOL, HPOR) has a driving capability of more than 30 mW of output power into a 16-Ω load at 0.1% THD, and an analog volume with zero crossing that can be controlled from –70 dB to 12 dB. For audio applications that require it, the analog volume for the L- and R-channels can be set simultaneously using the headphone output update control.

The line outputs and headphone output can select analog input sources from all the analog inputs and each DAC channel, as shown in Figure 29. The descriptions for the analog output registers are shown in Table 2.

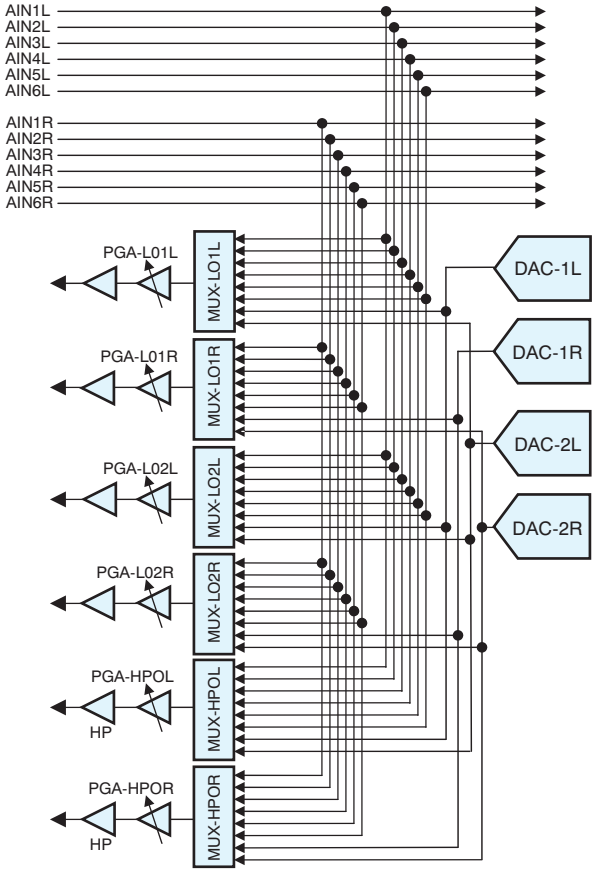



**Figure 29. Analog Outputs**

**Table 2. Analog Output Registers**

| REGISTER DESCRIPTION | REGISTER NUMBER | REGISTER BITS |
|---|---|---|
| Gain level control for line outputs | 27 | GL2R[1:0], GL2L[1:0], GL1R[1:0], GL1L[1:0] |
| 2.0 $V_{RMS}$ or 2.4 $V_{RMS}$ selection for line outputs | 28 | G242, G241 |
| Headphone volume zero crossing update control | 30 | HUPE, HSUR, HSUL, HZRS |
| Headphone output volume level setting | 31, 32 | HMUL, HMUR, HVOL[6:0], HVOR[6:0] |
| Analog output mux selection for line output 1 | 24 | AL1R[3:0], AL1L[3:0] |
| Analog output mux selection for line output 2 | 25 | AL2R[3:0], AL2L[3:0] |
| Analog output mux selection for headphone output | 26 | AHPR[3:0], AHPL[3:0] |

## SYSTEM CLOCK INPUT, OUTPUT, AND $f_S$ AUTOMATIC DETECTION

The PCM5310 has six system clock input ports: SCK1, SCK2, SCK3, SCK4, SCK5, and SCK6. Each input port can receive an independent clock at various frequencies. These ports are used for the internal clock of the digital filters and delta-sigma modulators, which are combined into a single common audio clock. The PCM5310 automatically detects the input clock rate at 128 $f_S$, 192 $f_S$, 256 $f_S$, 384 $f_S$, 512 $f_S$ or 768 $f_S$ (where $f_S$ is the audio sampling rate); if necessary, automatic clock rate detection can be disabled. The descriptions for the system clock input, output, and $f_S$ automatic detection registers are shown in Table 3. Table 4 shows the frequency of the common audio clock. Figure 30 and Table 5 shows the timing requirements for the system clock input.

**Table 3. System Clock Input, Output, and $f_S$ Automatic Detection Registers**

| REGISTER DESCRIPTION | REGISTER NUMBER | REGISTER BITS |
|---|---|---|
| Master or slave with $f_S$ detection for DAC12 | 44 | DMS12[3:0] |
| Audio interface format for DAC12 | 44 | DFM12[1:0] |
| Master or slave with $f_S$ detection for DAC34 | 54 | DMS34[3:0] |
| Audio interface format for DAC34 | 54 | DFM34[1:0] |
| Master or slave with $f_S$ detection for ADC12 | 84 | AMS12[3:0] |
| Audio interface format for ADC12 | 84 | AFM12[1:0] |
| Master or slave with $f_S$ detection for ADC34 | 94 | AMS34[3:0] |
| Audio interface format for ADC34 | 94 | AFM34[1:0] |
| SCK6 clock output selection | 07 | PSC6[2:0] |

**Table 4. System Clock Frequencies for the Common Audio Clock**

| SAMPLING FREQUENCY (kHz) | SYSTEM CLOCK FREQUENCY (MHz) | | | | | |
|---|---|---|---|---|---|---|
| | 128 $f_S$ (1) | 192 $f_S$ (1) | 256 $f_S$ | 384 $f_S$ | 512 $f_S$ | 768 $f_S$ |
| 32 | 4.0960 | 6.1440 | 8.1920 | 12.2880 | 16.3840 | 24.5760 |
| 44.1 | 5.6488 | 8.4672 | 11.2896 | 16.9344 | 22.5792 | 33.8688 |
| 48 | 6.1440 | 9.2160 | 12.2880 | 18.4320 | 24.5760 | 36.8640 |
| 88.2 | 11.2896 | 16.9344 | 22.5792 | 33.8688 | Not supported | Not supported |
| 96 | 12.2880 | 18.4320 | 24.5760 | 36.8640 | Not supported | Not supported |
| 176.4 (1) | 22.5792 | 33.8688 | Not supported | Not supported | Not supported | Not supported |
| 192 (1) | 24.5760 | 36.8640 | Not supported | Not supported | Not supported | Not supported |

(1) This sampling frequency and system clock frequency are supported only for the DAC.

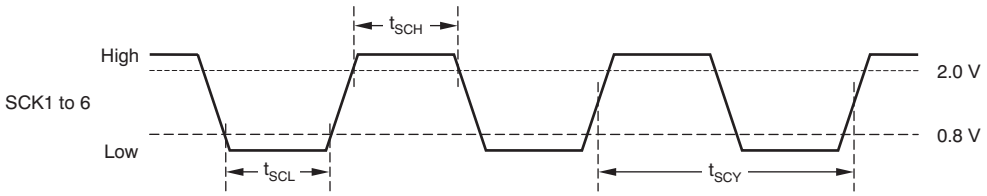


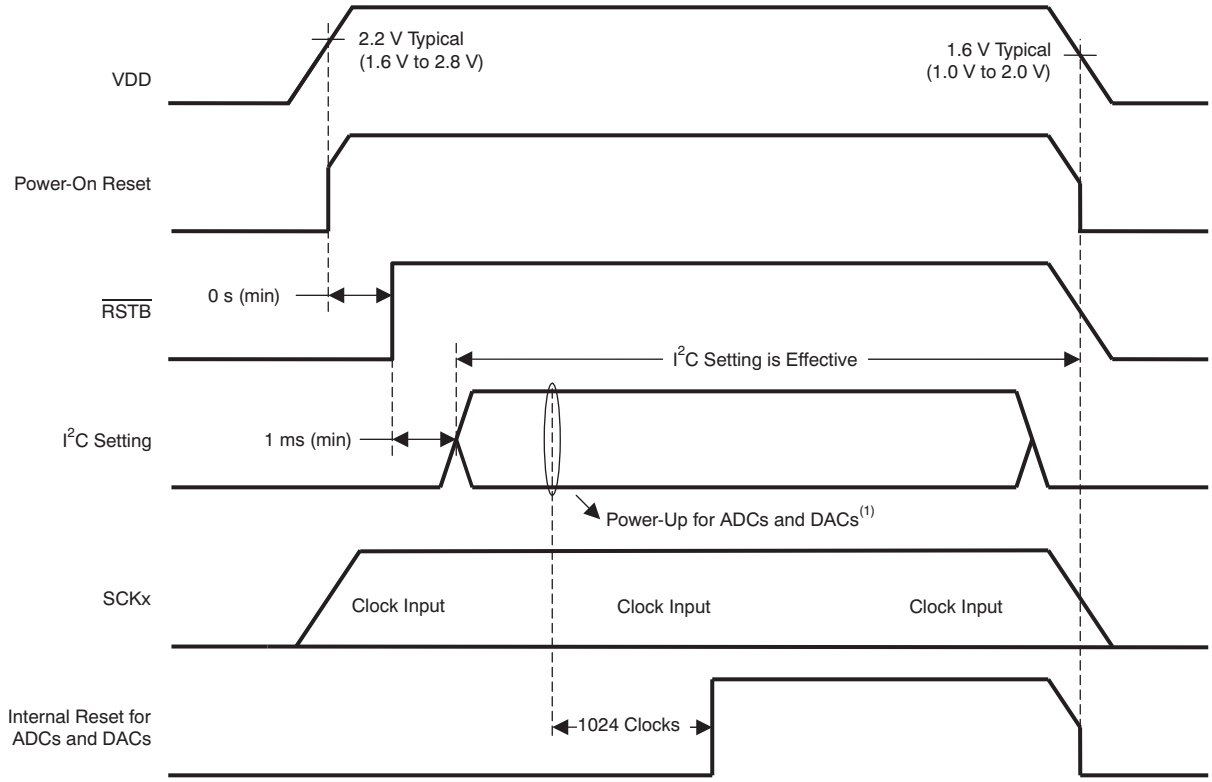

**Figure 30. System Clock Input Timing**

**Table 5. Timing Characteristics for Figure 30**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{SCY}$ | System clock cycle time | 25 | | ns |
| $t_{SCH}$ | System clock high time | 0.4 $t_{SCY}$ | | ns |
| $t_{SCL}$ | System clock low time | 0.4 $t_{SCY}$ | | ns |
| | System clock duty cycle | 40 | 60 | % |

## POWER ON/OFF RESET

The power-on reset (POR) circuit generates a reset signal at typically 2.2 V; this circuit does not depend on the other power supplies: $V_{CCDA}$, $V_{CCAD}$, $V_{CCH}$, and $V_{CCP}$. The internal circuit is cleared to default status, then all analog and digital outputs have no signal. It is recommended to turn the device on and off as shown in Figure 31, in order to avoid loud, audible *pop* noises when powering the device on or off.




(1) $\overline{\text{RSTB}}$ is active low. 100 ns (minimum) is needed for an effective reset to the internal circuit.

**Figure 31. Power On/Off Reset**

## REGISTER RESET AND SYSTEM RESET (Register 01)

Register reset (MRST) clears all register data to the default setting. The MRST register is automatically set to '1' after the reset.

System reset (SRST) clears all internal circuits, including all register data, to default status simultaneously. The SRST register is automatically set to '1' after the reset.

Note that the PCM5310 may have audible pop noises on the analog and digital outputs when enabling MRST and SRST.

The descriptions for the register reset and system reset registers are shown in Table 6.

**Table 6. Reset Registers**

| REGISTER DESCRIPTION | REGISTER NUMBER | REGISTER BITS |
|---|---|---|
| Reset register data only | 01 | MRST |
| Reset for all circuits including register data | 01 | SRST |

## $\overline{\text{RSTB}}$ Control

Taking $\overline{\text{RSTB}}$ (pin 58) from high to low clears all internal circuits to default status. If an application does not require reset control, $\overline{\text{RSTB}}$ should be connected with an RC passive delay circuit to the digital power supply ($V_{DD}$).

Note that the PCM5310 may have audible pop noises on the analog and digital outputs when enabling $\overline{\text{RSTB}}$.

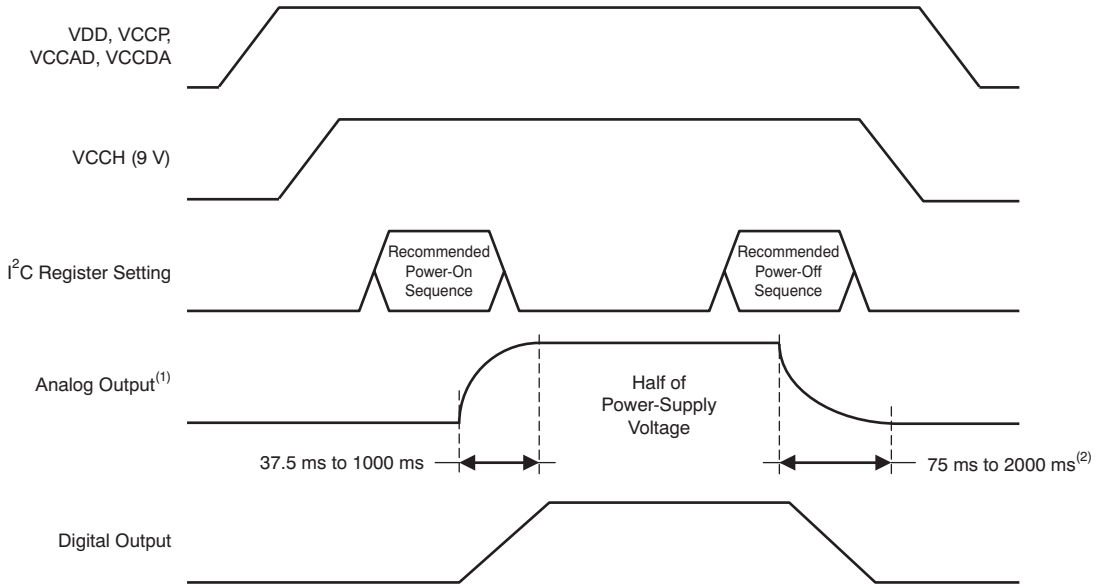
The $\overline{\text{RSTB}}$ control status descriptions are shown in Table 6.

**Table 7. $\overline{\text{RSTB}}$ Control**

| $\overline{\text{RSTB}}$ (PIN 58) STATUS | DESCRIPTION |
|---|---|
| Low | Reset all circuits including register data |
| High | Reset release |

## POWER-SUPPLY SEQUENCE AND POWER ON/OFF SEQUENCE

In order to reduce audible pop noise, a register setting sequence is required after turning on all power supplies and before turning off all power supplies. Any modules that are not used in the application or system should be powered down after the recommended power-on sequence. Before the power-off sequence, all modules should be in a power-on state. The recommended power-supply sequence is shown in Figure 32. The recommended register settings are shown in Table 8 and Table 9.




(1) Ramp up/down time for the analog output can be changed through the register setting (see Register 18, PDTM[2:0]).

(2) A 1.0-µF capacitor should be connected to the VCOMAD and VCOMDA pins.

**Figure 32. Recommended Power On/Off Sequence**

**Table 8. Recommended Register Settings When Powered On**

| STEP | REGISTER SETTING | | DESCRIPTION |
|---|---|---|---|
| | ADDRESS | DATA | |
| 1 | — | — | Turn on all power supplies |
| 2 | 11 | 00 | Analog bias power up |
| 3 | 1F | 49 | Headphone output L-channel mute disable and level (–42 dB) setting(1) |
| 4 | 20 | 49 | Headphone output R-channel mute disable and level (–42 dB) setting(1) |
| 5 | 1E | B0 | Headphone volume update control |
| 6 | 1B | 00 | Line output gain (0 dB) control from DAC(1) |
| 7 | 1C | 00 | Line output 2 $V_{RMS}$ and 2.4 $V_{RMS}$ mode select |
| 8 | 2A | FF | DAC12 L-channel digital attenuation level (0 dB) setting(1) |
| 9 | 2B | FF | DAC12 R-channel digital attenuation level (0 dB) setting(1) |
| 10 | 29 | 00 | DAC12 digital mute setting and digital gain boost |
| 11 | 28 | B1 | DAC12 digital attenuation/mute control and zero crossing enable |
| 12 | 34 | FF | DAC34 L-channel digital attenuation level (0 dB) setting(1) |
| 13 | 35 | FF | DAC34 R-channel digital attenuation level (0 dB) setting(1) |
| 14 | 33 | 00 | DAC34 digital mute setting and digital gain (0 dB) boost |
| 15 | 32 | B1 | DAC34 digital attenuation/mute control and zero crossing enable |
| 16 | 52 | D5 | ADC12 L-channel digital attenuation level (0 dB) setting(1) |
| 17 | 53 | D5 | ADC12 R-channel digital attenuation level (0 dB) setting(1) |

(1) Any level is acceptable for volume, gain, and attenuation. The level should be resumed by register data recorded when the system powers off.

**Table 8. Recommended Register Settings When Powered On (continued)**

| STEP | REGISTER SETTING | | DESCRIPTION |
|---|---|---|---|
| | ADDRESS | DATA | |
| 18 | 51 | 00 | ADC12 digital mute disable |
| 19 | 50 | 01 | ADC12 digital attenuation/mute control and zero crossing enable |
| 20 | 5C | D7 | ADC34 L-channel digital attenuation level (0 dB) setting(1) |
| 21 | 5D | D7 | ADC34 R-channel digital attenuation level (0 dB) setting(1) |
| 22 | 5B | 00 | ADC34 digital mute disable |
| 23 | 5A | 01 | ADC34 digital attenuation/mute control and zero crossing enable |
| 24 | 18 | 77 | Line output 1 L-/R-channel mux select |
| 25 | 19 | 00 | Line output 2 L-/R-channel mux select |
| 26 | 1A | 88 | Headphone output L-/R-channel mux select |
| 27 | 14 | 11 | ADC12 analog input mux select (AIN1L/R)(2) |
| 28 | 15 | 22 | ADC34 analog input mux select (AIN2L/R)(2) |
| 29 | 16 | 00 | ADC12 analog input gain level (0 dB) setting(1) |
| 30 | 17 | 00 | ADC34 analog input gain level (0 dB) setting(1) |
| 31 | 65 | 98 | Audio interface (LRCKx/BCKx) PORT-1 and PORT-2 setting (ADC12/34, master)(3) |
| 32 | 66 | 98 | Audio interface (DATAx) PORT-1 and PORT-2 setting (DATA output of ADC12/34)(3) |
| 33 | 67 | 10 | Audio interface (SCKx) PORT-1 and PORT-2 setting (input of SCK1/2)(4) |
| 34 | 68 | 32 | Audio interface (LRCKx/BCKx) PORT-3 and PORT-4 setting (input of LRCK3/4, BCK3/4)(4) |
| 35 | 69 | 32 | Audio interface (DATAx) PORT-3 and PORT-4 setting (input of DATA3/4)(4) |
| 36 | 6A | 32 | Audio interface (SCKx) PORT-3 and PORT-4 setting (input of SCK3/4)(4) |
| 37 | 6B | 54 | Audio interface (LRCKx/BCKx) PORT-5 and PORT-6 setting (input of LRCK3/4, BCK3/4)(4) |
| 38 | 6C | 54 | Audio interface (DATAx) PORT-5 and PORT-6 setting (input of DATA5/6)(4) |
| 39 | 6D | 54 | Audio interface (SCKx) PORT-5 and PORT-6 setting (input of SCK5/6)(4) |
| 40 | 6E | 43 | DAC12 and DAC34 LRCK/BCK select(4) |
| 41 | 6F | 43 | DAC12 and DAC34 DATA select(4) |
| 42 | 70 | 43 | DAC12 and DAC34 SCK select(4) |
| 43 | 74 | 89 | ADC12 and ADC34 LRCK/BCK select (ADC12/34, master)(4) |
| 44 | 75 | 10 | ADC12 and ADC34 SCK select(4) |
| 45 | 76 | 76 | GPIO control or GPIO1 and GPIO2 audio data select |
| 46 | 2C | 80 | DAC12 audio interface and master/slave select(5) |
| 47 | 36 | 80 | DAC34 audio interface and master/slave select(5) |
| 48 | 54 | 40 | ADC12 audio interface and master/slave select (master, 256 $f_S$)(5) |
| 49 | 5E | 40 | ADC34 audio interface and master/slave select (master, 256 $f_S$)(5) |
| 50 | 12 | 11 | Analog back-end and front-end power-up |
| 51 | 2E | 00 | DAC12 power-up |
| 52 | 38 | 00 | DAC34 power-up |
| 53 | 55 | 00 | ADC12 power-up |
| 54 | 5F | 00 | ADC34 power-up |
| 55 | 12 | 01 | Common voltage ($V_{COM}$) power-up and ramp up/down time setting |

(2) Any input terminals are acceptable for input of ADC12 and ADC34.
(3) These settings are not required if application does not use audio interface mux and bypass selection.
(4) These settings are not required if application does not use audio interface mux and bypass selection.
(5) These settings are not required if application uses slave mode for audio interface and SCK automatic $f_S$ detection.

**Table 9. Recommended Register Setting When Powered Off**

| STEP | REGISTER SETTING | | DESCRIPTION |
|---|---|---|---|
| | ADDRESS | DATA | |
| 1 | 18 | 00 | Line output1 L- and R-channel mux select |
| 2 | 19 | 00 | Line output2 L- and R-channel mux select |
| 3 | 1A | 00 | Headphone output L- and R-channel mux select |
| 4 | 14 | 00 | ADC12 analog input mux select |
| 5 | 15 | 00 | ADC34 analog input mux select |
| 6 | 12 | 11 | Common voltage ($V_{COM}$) power-down and ramp up/down time setting |
| 7 | 55 | 80 | ADC12 power-down |
| 8 | 5F | 80 | ADC34 power-down |
| 9 | 2E | 80 | DAC12 power-down |
| 10 | 38 | 80 | DAC34 power-down |
| 11 | 12 | 71 | Analog back-end and front-end power-down |
| 12 | 11 | 80 | Analog bias power-down |
| 13 | — | — | Turn off all power supplies |

## AUDIO SERIAL INTERFACE

The PCM5310 has six audio interface ports: SCKx, BCKx, LRCKx, and DATAx (bidirectional). Each port or signal can be connected to any ADC or DAC. If an audio system application wants to bypass an audio signal, the PCM5310 can bypass from any port to any port. Refer to Figure 33 for a diagram of the of the audio interface port and mux. See Figure 47 to Figure 52 for detailed diagrams of PORT-1 to PORT-6.

The audio interface consists of LRCKs, BCKs, and DATAs. The sampling rate ($f_S$), left channel and right channel data are present on the LRCKs. The DATAs receive the serial audio data from the interpolation filter for the DAC, and the DATAs transmit the serial data to the decimation filter. The BCKs are used to receive and transmit the serial audio data on the DATAs by high-to-low transition. The BCKs and LRCKs should be synchronized with the system clocks, SCKs. The PCM5310 operates with the LRCKs/BCKs synchronized with the SCKs; however, the PCM5310 does not need a specific phase between the BCKs/LRCKs and the SCKs. Each audio interface port can select either the master or slave mode, and generate the LRCKs and BCKs from the SCKs in master mode. The descriptions for the audio serial interface registers are shown in Table 6.

**Table 10. Audio Serial Interface Registers**

| REGISTER DESCRIPTION | REGISTER NUMBER | REGISTER BITS |
|---|---|---|
| Master or slave with $f_S$ detection for DAC12 | 44 | DMS12[3:0] |
| Audio interface format for DAC12 | 44 | DFM12[1:0] |
| Master or slave with $f_S$ detection for DAC34 | 54 | DMS34[3:0] |
| Audio interface format for DAC34 | 54 | DFM34[1:0] |
| Master or slave with $f_S$ detection for ADC12 | 84 | AMS12[3:0] |
| Audio interface format for ADC12 | 84 | AFM12[1:0] |
| Master or slave with $f_S$ detection for ADC34 | 94 | AMS34[3:0] |
| Audio interface format for ADC34 | 94 | AFM34[1:0] |
| LRCK/BCK selection of PORT-1 and PORT-2 | 101 | LBS2[3:0], LBS1[3:0] |
| DATA selection of PORT-1 and PORT-2 | 102 | DTS2[3:0], DTS1[3:0] |
| SCK selection of PORT-1 and PORT-2 | 103 | SCS2[2:0], SCS1[2:0] |
| LRCK/BCK selection of PORT-3 and PORT-4 | 104 | LBS4[3:0], LBS3[3:0] |
| DATA selection of PORT-3 and PORT-4 | 105 | DTS4[3:0], DTS3[3:0] |
| SCK selection of PORT-3 and PORT-4 | 106 | SCS4[2:0], SCS3[2:0] |
| LRCK/BCK selection of PORT-5 and PORT-6 | 107 | LBS6[3:0], LBS5[3:0] |
| DATA selection of PORT-5 and PORT-6 | 108 | DTS6[3:0], DTS5[3:0] |
| SCK selection of PORT-5 and PORT-6 | 109 | SCS6[2:0], SCS5[2:0] |
| LRCK/BCK selection of DAC12 and DAC34 | 110 | D34LB[3:0], D12LB[3:0] |
| DATA selection of DAC12 and DAC34 | 111 | D34DT[3:0], D12DT[3:0] |
| SCK selection of DAC12 and DAC34 | 112 | D34S[2:0], D12S[2:0] |
| LRCK/BCK selection of ADC12 and ADC34 | 116 | A34LB[3:0], A12LB[3:0] |
| SCK selection of ADC12 and ADC34 | 117 | A34SC[2:0], A12SC[2:0] |
| GPIO-1 and GPIO-2 audio data selection | 118 | GP2S[3:0], GP1S[3:0] |

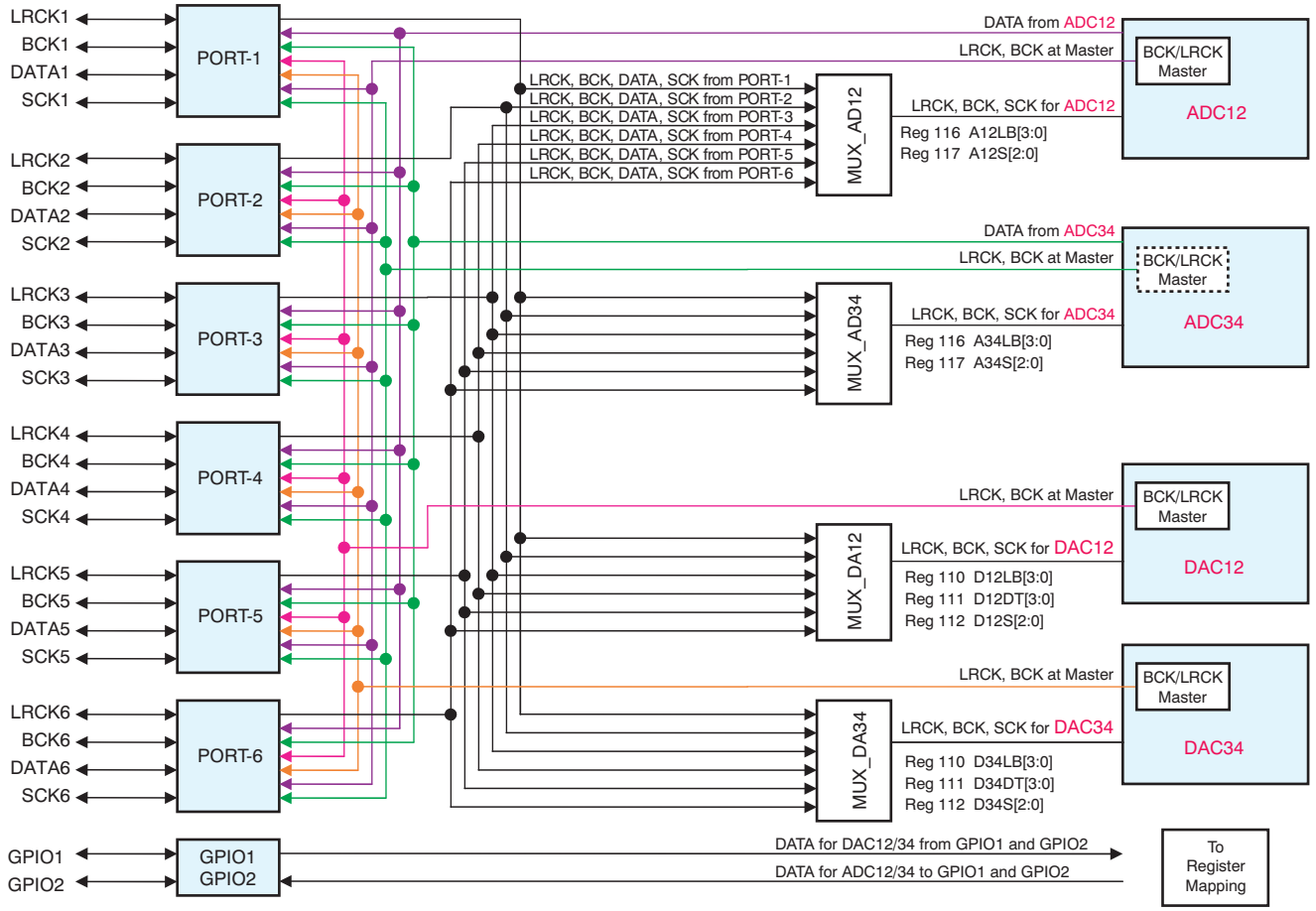



**Figure 33. Audio Interface Port and Mux**

## AUDIO DATA FORMATS AND TIMING

The PCM5310 supports $I^2S$, left-justified, and right-justified data formats with 32 $f_S$, 48 $f_S$, or 64 $f_S$ BCK rates for digital input, and 48 $f_S$ or 64 $f_S$ BCK rates for the ADC. The data formats are shown in Figure 34 and can be selected through the $I^2C$ interface. All formats require binary twos complement, MSB first audio data. The default format is 16- to 24-bits $I^2S$. Figure 35 and Figure 36 show detailed timing diagrams. The descriptions for the audio interface data format registers are shown in Table 11.

**Table 11. Audio Interface Data Format Registers**

| REGISTER DESCRIPTION | REGISTER NUMBER | REGISTER BITS |
|---|---|---|
| Audio interface format for DAC12 | 44 | DFM12[1:0] |
| Audio interface format for DAC34 | 54 | DFM34[1:0] |
| Audio interface format for ADC12 | 84 | AFM12[1:0] |
| Audio interface format for ADC34 | 94 | AFM34[1:0] |

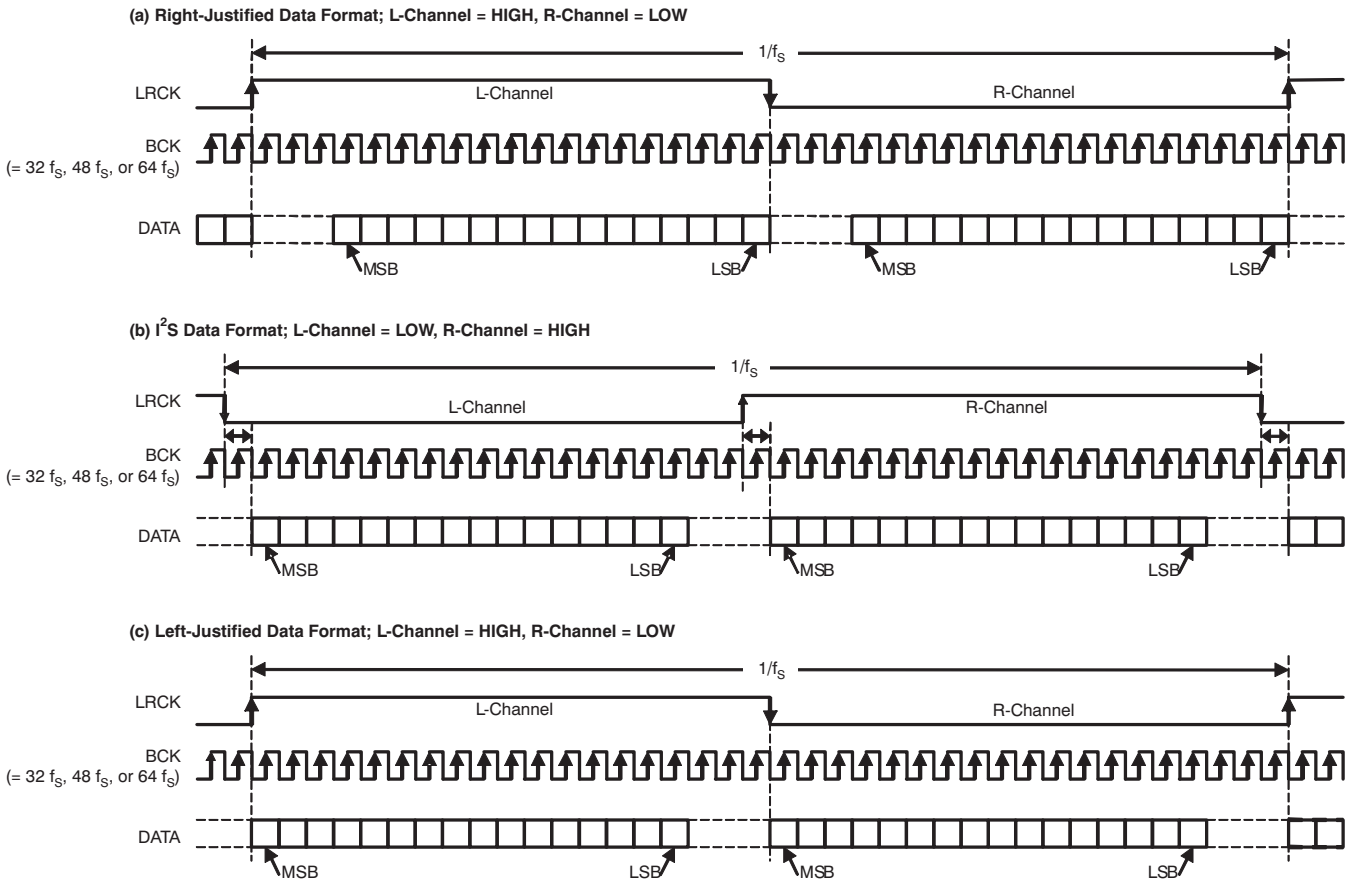
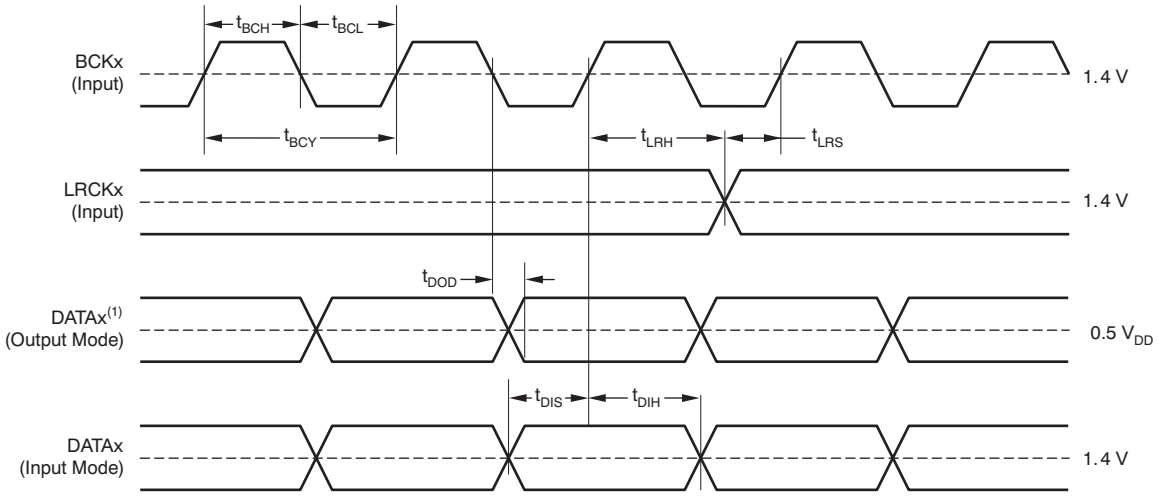



**Figure 34. Audio Data Input and Output Formats**

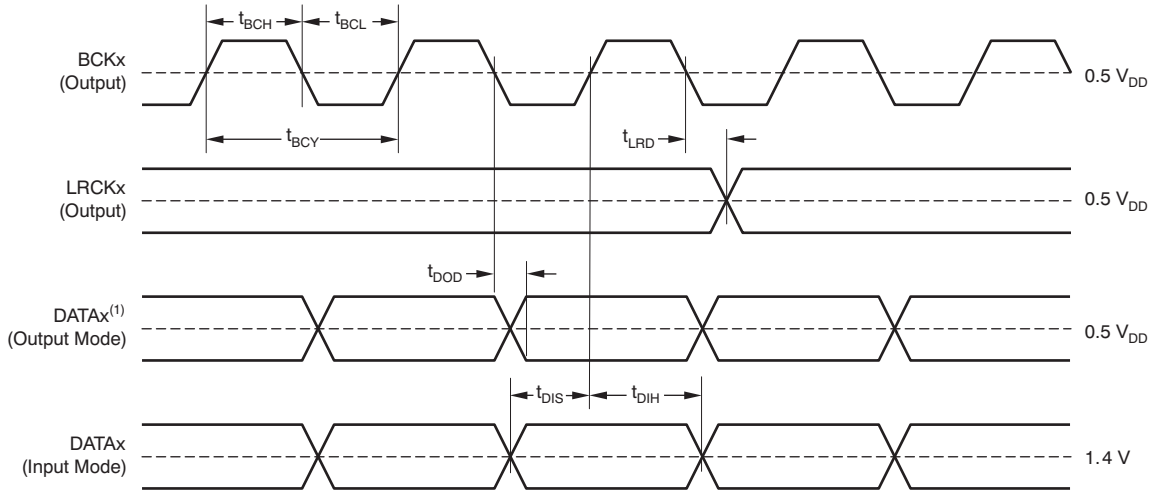



(1) Load capacitance of output is 20 pF.

**Figure 35. Audio Interface Timing (Slave Mode)**

**Table 12. Timing Requirements for Figure 35**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{BCY}$ | BCKx cycle time | 75 | | ns |
| $t_{BCH}$ | BCKx pulse width high | 35 | | ns |
| $t_{BCL}$ | BCKx pulse width low | 35 | | ns |
| $t_{LRS}$ | LRCKx set-up time to BCKx rising edge | 15 | | ns |
| $t_{LRH}$ | LRCKx hold time to BCKx rising edge | 10 | | ns |
| $t_{DIS}$ | DATAx setup time to BCKx rising edge | 10 | | ns |
| $t_{DIH}$ | DATAx hold time to BCKx rising edge | 10 | | ns |
| $t_{DOD}$ | DATAx delay time from BCKx falling edge | 0 | 30 | ns |




(1) Load capacitance of output is 20 pF.

**Figure 36. Audio Interface Timing (Master Mode)**

**Table 13. Timing Requirements for Figure 36**

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{BCY}$ | BCKx cycle time | | 1/(64 $f_S$) | | |
| $t_{BCH}$ | BCKx pulse width high | 0.4 $t_{BCY}$ | 0.5 $t_{BCY}$ | 0.6 $t_{BCY}$ | |
| $t_{BCL}$ | BCKx pulse width low | 0.4 $t_{BCY}$ | 0.5 $t_{BCY}$ | 0.6 $t_{BCY}$ | |
| $t_{LRD}$ | LRCKx delay time from BCKx falling edge | –15 | | 20 | ns |
| $t_{DIS}$ | DATAx setup time to BCKx rising edge | 10 | | | ns |
| $t_{DIH}$ | DATAx hold time to BCKx rising edge | 10 | | | ns |
| $t_{DOD}$ | DATAx delay time from BCKx falling edge | –10 | | 20 | ns |

## ADC AND FILTER

The analog-to-digital converter (ADC) and digital filter include a delta-sigma modulator, decimation filter, high-pass filter (HPF), digital gain control, digital attenuation control, and digital soft mute, as shown in Figure 37. The HPF eliminates dc offset of the ADC analog section with 0.91 Hz as the cutoff frequency at a 48-kHz sampling rate. The digital gain or attenuation control can be adjusted from 20 dB to –100 dB in 0.5-dB steps. The descriptions for the ADC and filter registers are shown in Table 14.

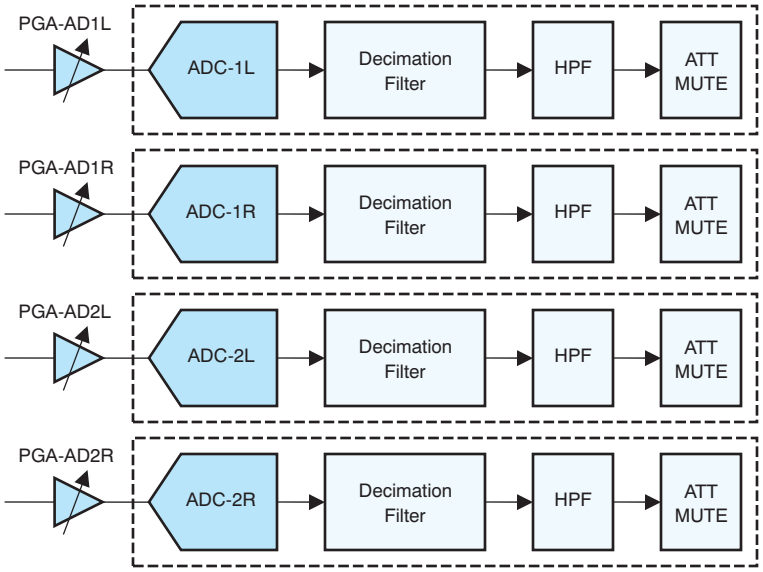



**Figure 37. ADCs and Filters**

**Table 14. ADC and Filter Registers**

| REGISTER DESCRIPTION | REGISTER NUMBER | REGISTER BITS |
|---|---|---|
| Digital attenuation and gain update control for ADC12 | 80 | A12E, AUC2, AUC1, AZ12 |
| Digital soft mute setting for ADC12 | 81 | AMU2, AMU1 |
| Digital attenuation and gain level setting for ADC12 | 82, 83 | AAT2[7:0], AAT1[7:0] |
| High-pass filter disable for ADC12 | 84 | HF12 |
| Digital attenuation and gain update control for ADC34 | 90 | A34E, AUC4, AUC3, AZ34 |
| Digital soft mute setting for ADC34 | 91 | AMU4, AMU3 |
| Digital attenuation and gain level setting for ADC34 | 92, 93 | AAT4[7:0], AAT3[7:0] |
| High-pass filter disable for ADC34 | 94 | HF34 |

## DAC AND FILTER

The digital-to-analog converter (DAC) and digital filter include a delta-sigma modulator, interpolation filter, de-emphasis filter (DEM), digital gain control, digital attenuation control, digital soft mute, and digital gain boost, as shown in Figure 38. The digital gain or attenuation control can be adjusted from 20 dB to –100 dB in 0.5-dB steps. To play back low-volume recorded audio data, the digital gain can be used with a boost of either 6 dB, 12 dB, or 18 dB selected through the $I^2C$ interface. The descriptions for the DAC and filter registers are shown in Table 14.

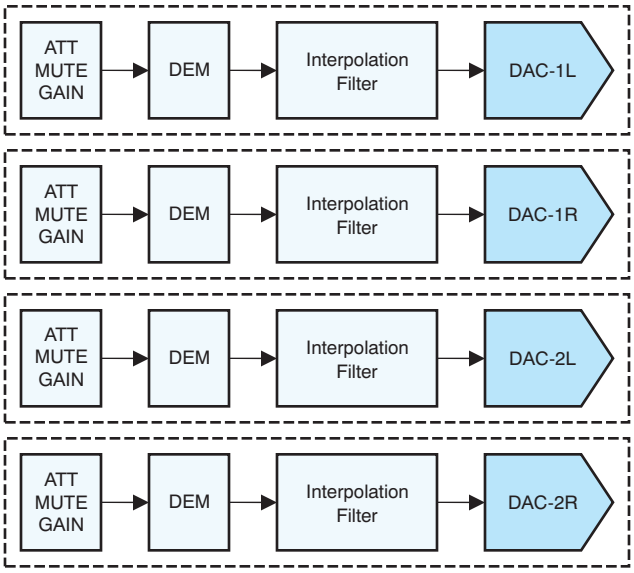



**Figure 38. DACs and Filters**

**Table 15. DAC and Filter Registers**

| REGISTER DESCRIPTION | REGISTER NUMBER | REGISTER BITS |
|---|---|---|
| Digital attenuation and gain update control for DAC12 | 40 | D12E, DUC2, DUC1, DZ12 |
| Digital soft mute and boost setting for DAC12 | 41 | DMU2, DMU1, DB12[1:0] |
| Digital attenuation and gain level setting for DAC12 | 42, 43 | DAT2[7:0], DAT1[7:0] |
| De-emphasis filter setting for DAC12 | 45 | DM12, DF12[1:0] |
| Digital attenuation and gain update control for DAC34 | 50 | D34E, DUC4, DUC3, DZ34 |
| Digital soft mute setting for DAC34 | 51 | DMU4, DMU3 |
| Digital attenuation and gain level setting for DAC34 | 52, 53 | DAT4[7:0], DAT3[7:0] |
| De-emphasis filter setting for DAC34 | 55 | DM34, DF34[1:0] |

## GPIO CONTROL

The PCM5310 has three general-purpose input/output (GPIO) pins (pins 55, 56, and 57) that can be assigned to various functions and internal status reads shown in Table 16, Table 17, Table 18, and Figure 39.

**Table 16. GPIO Control Registers**

| REGISTER DESCRIPTION | REGISTER NUMBER | REGISTER BITS |
|---|---|---|
| GPIO1 select, bypass PORT-4 | 09 | GBP4, GSL1[4:0] |
| GPIO2 select, bypass PORT-5 | 10 | GBP5, GSL2[4:0] |
| GPIO3 select | 11 | GSL3[4:0] |

**Table 17. Register Data Read Through the GPIO Pins**

| REGISTER DESCRIPTION | REGISTER NUMBER | REGISTER BITS |
|---|---|---|
| External device control | 08 | GPO3, GPO2, GPO1 |
| Headphone short-circuit protection status | 16 | SSHR, SSHL |
| Headphone insertion detect status | 35 | RHPI |
| Mute status for headphone | 35 | RHMUR, RHMUL |
| System clock $f_S$ detect for DAC12, DAC34 | 35, 36 | RD12FS[2:0], RD34[2:0] |
| System clock $f_S$ detect for ADC12, ADC34 | 37, 38 | RA12FS[2:0], RA34[2:0] |
| Digital mute status for DAC12 and DAC34 | 36 | RDM4, RDM3, RDM2, RDM1 |
| Digital mute status for ADC12 and ADC34 | 37 | RAM4, RAM3, RAM2, RAM1 |
| Zero crossing timeout for DAC12 and DAC34 | 38 | RDZ4, RDZ3, RDZ2, RDZ1 |
| Zero crossing timeout for ADC12 and ADC34 | 39 | RAZ4, RAZ3, RAZ2, RAZ1 |
| Zero crossing timeout for headphone | 39 | RHZR, RHZL |

**Table 18. Other GPIO Pin Functions**

| GPIO PIN FUNCTION | DESCRIPTION |
|---|---|
| Zero flag for digital input | Read the status for each DAC channel or all DAC channels |
| Logic | OR, AND, NOR, NAND, buffer, inverter |
| Audio data | Bypass audio data to PORT-4 and PORT-5 from GPIO pins |

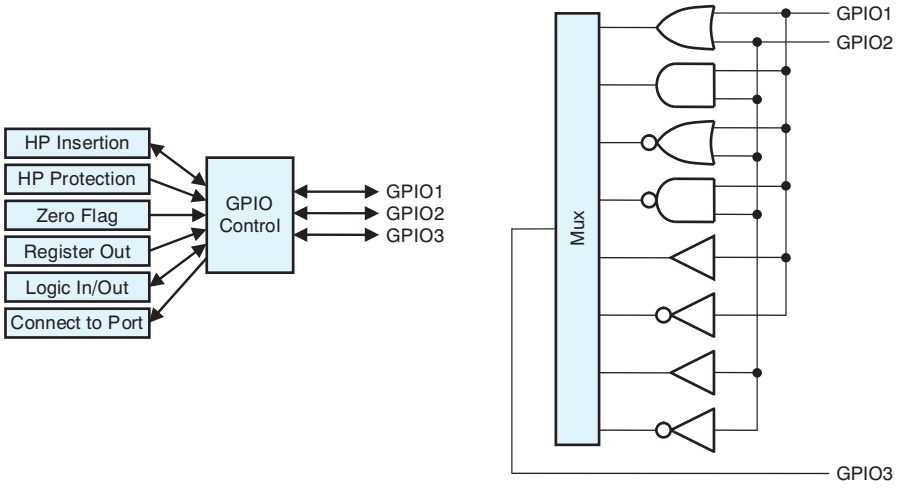



**Figure 39. GPIO Control**

## HEADPHONE SHORT-CIRCUIT PROTECTION

The PCM5310 has short-circuit protection for each headphone output. The short-circuit status can be read from the GPIO pins and the register data can be read through the $I^2C$ interface. The short-circuit detection time can be internally adjusted to avoid the headphone amplifier shutting down when inserting or removing the headphone jack. The descriptions for the headphone and short-circuit protection registers are shown in Table 19. The headphone short-circuit protection sequence is shown in Figure 40.

**Table 19. Headphone Short-Circuit Protection Registers**

| REGISTER DESCRIPTION | REGISTER NUMBER | REGISTER BITS |
|---|---|---|
| Headphone short-circuit protection enable/disable | 13 | SRCR, SHCR, SPDR, SRCL, SHCL, SPDL |
| Headphone short-circuit protection detect time | 14 | SDTR[1:0], SDTL[1:0] |
| Headphone short-circuit protection release time | 15 | SRTR[1:0], SRTL[1:0] |
| Headphone short-circuit protection status read | 16 | SSHR, SSHL |

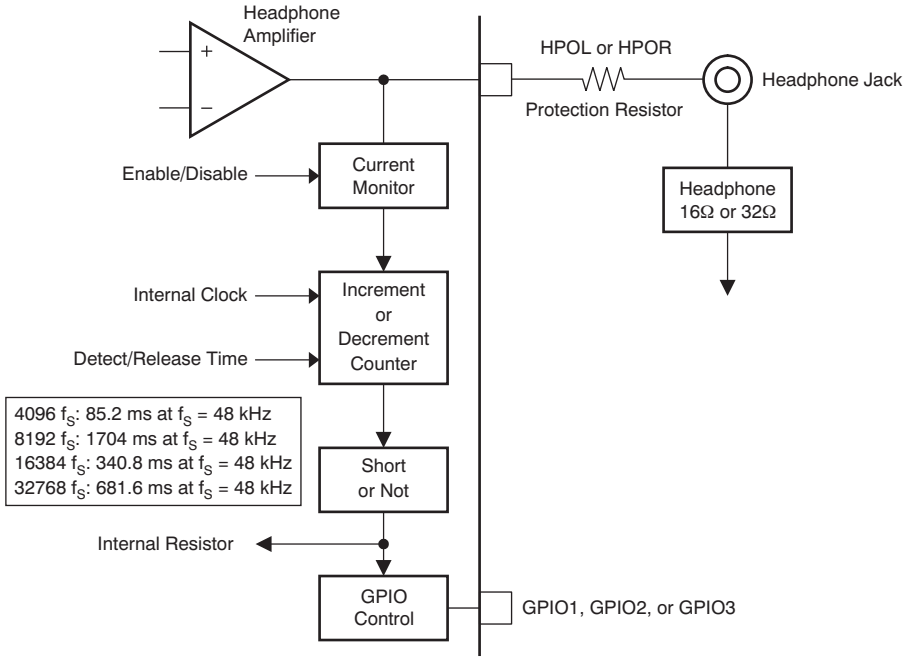



**Figure 40. Headphone Short-Circuit Protection Sequence**

When the short-circuit protection is enabled, it is recommended to insert a small protection resistor to limit over-current flow. Table 20 shows the headphone output power with a small resistor.

**Table 20. Headphone Amplifier Output Power Load**

| $R_L$ = 32 Ω + PROTECTION RESISTOR | 32 Ω + 4 Ω | 32 Ω + 8 Ω | 32 Ω + 16 Ω |
|---|---|---|---|
| 0.1% THD | 28 mW | 22 mW | 16 mW |
| 10% THD | 37 mW | 31 mW | 22 mW |

## HEADPHONE INSERTION DETECTION

The descriptions for the headphone insertion detection registers are shown in Table 21. The PCM5310 detects the insertion status of a headphone plug using the GPIO pins through the register setting and writes the status to the register, which can be read by the $I^2C$ interface. The status can also output to the GPIO pins, as shown in Figure 41.

**Table 21. Headphone Insertion Detection Registers**

| REGISTER DESCRIPTION | REGISTER NUMBER | REGISTER BITS |
|---|---|---|
| GPIO1 selection | 09 | GSL1[4:0] |
| GPIO2 selection | 10 | GSL2[4:0] |
| GPIO3 selection | 11 | GSL3[4:0] |
| Read status for headphone insertion | 35 | RIPI |

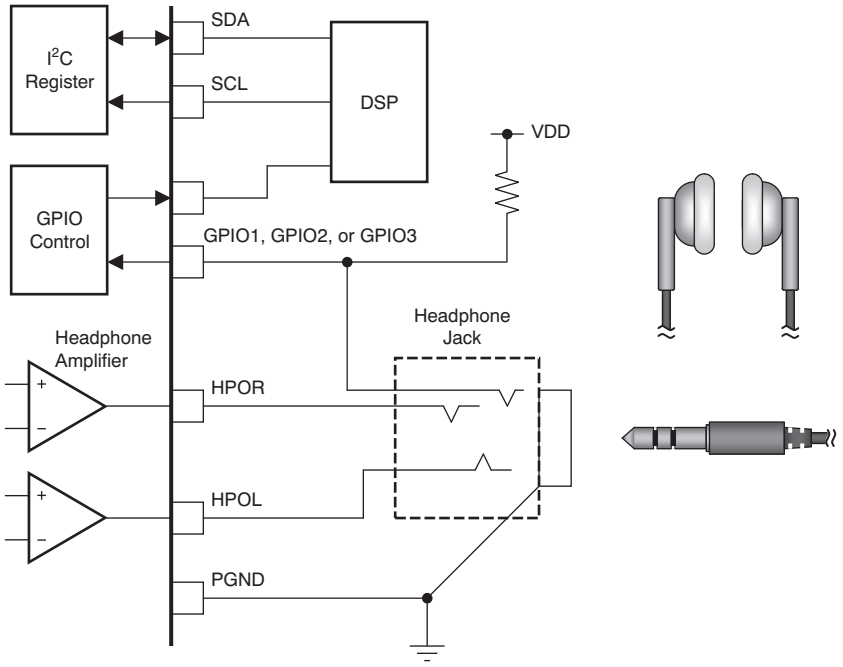



**Figure 41. Headphone Insertion Detection**

## ZERO FLAG DETECTION

The PCM5310 detects continuous zero data input to either DAC12, DAC34, or both DAC12 and DAC34. The GPIO pins can output the status to an external device by the register setting. The flag changes from low to high when the L-and R-channel data are zero after 1024 $f_S$. The descriptions for the zero flag detection registers are shown in Table 22. Figure 42 shows the zero flag detection operation.

**Table 22. Zero Flag Registers**

| REGISTER DESCRIPTION | REGISTER NUMBER | REGISTER BITS |
|---|---|---|
| GPIO1 selection | 09 | GSL1[4:0] |
| GPIO2 selection | 10 | GSL2[4:0] |
| GPIO3 selection | 11 | GSL3[4:0] |

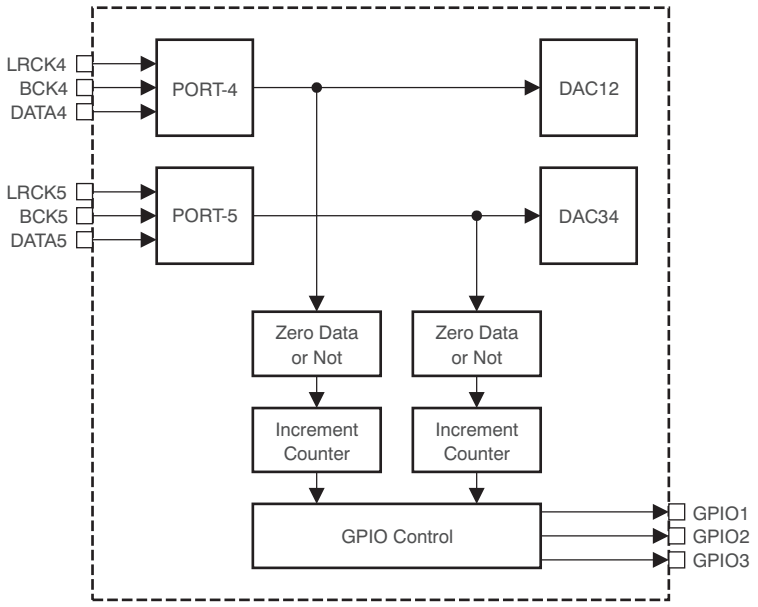



**Figure 42. Zero Flag Detection**

## AMUTE Control

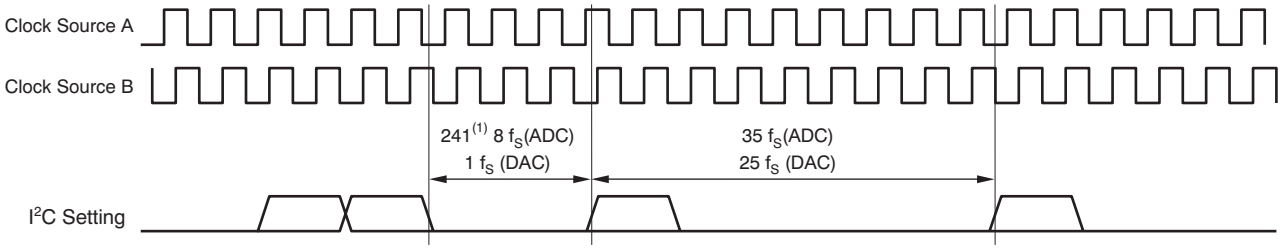
The PCM5310 has an AMUTE pin (pin 59) that controls the digital and analog mute function linked to Register 19 (13h). If these settings are disabled and the AMUTE pin goes from low to high, the PCM5310 holds the digital and analog mute disabled. If these settings are enabled and the AMUTE pin goes from low to high, the PCM5310 enables digital and analog mute. The mute function set by the AMUTE pin is effective, regardless of the setting in Register 19.

## MUTE CONTROL TIMING DURING CLOCK CHANGES

The PCM5310 has six audio interface ports and can change from the current source to another source. However, the analog output or digital output may have an audible pop noise when changing or stopping clocks. It is recommend to use the mute control with zero data input and waiting time to avoid pop noise and clean up the internal circuit via $I^2C$. Figure 43 illustrates the details.

Note that the digital and analog inputs should be zero data initially. After that, use the following steps:

1. Disable zero crossing detection.
2. Enable the analog or digital output mute.
3. Change the clock source.
4. Disable the analog or digital mute.



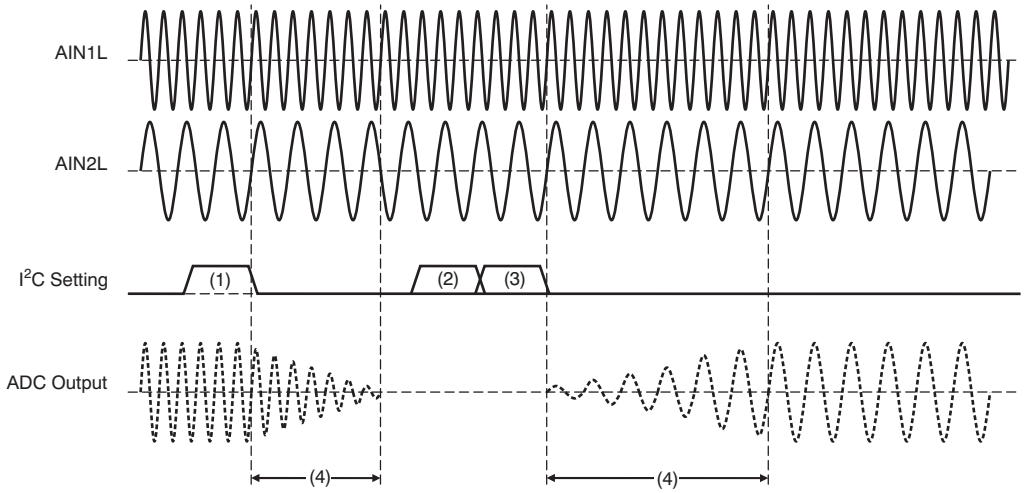

NOTE: The digital and analog inputs should be zero data at first. Then use the following setting procedure:
a) Disable zero crossing detection.
b) Enable analog or digital output mute.
c) Change the clock source.
d) Disable the analog or digital mute.

(1) Value depends on attenuation level setting in Registers 82, 83, 92, and 93.

**Figure 43. Mute Control Timing During Clock Changes**

## ANALOG MUX CHANGING TO REDUCE AUDIBLE NOISE

The PCM5310 has an analog multiplexer (mux) that can select six stereo analog inputs. The ADC output may have audible noise when selecting without mute control via $I^2C$. It is recommend to use digital soft mute before changing the analog input, as shown in Figure 44.




(1) Enable digital soft mute of ADC.

(2) Change analog input source.

(3) Disable digital soft mute of ADC.

(4) Maximum mute time is [241 × 8 $f_S$] seconds; however, this time depends on the wave form if zero crossing is enabled. It is recommended to read the status of this mute from Register 35 to 39 via $I^2C$. Then if the status is high, disable mute.

**Figure 44. Analog Mux Changing to Reduce Audible Noise**

## TWO-WIRE INTERFACE ($I^2C$)

The PCM5310 supports the $I^2C$ serial bus and the data transmission protocol for the $I^2C$ standard as a slave device. This protocol is explained in the $I^2C$ specification 2.0.

In $I^2C$ mode, the control terminals are changed as shown in Table 23.

**Table 23. Control Pins**

| PIN NAME | INPUT/OUTPUT | DESCRIPTION |
|---|---|---|
| SDA | Input/Output | $I^2C$ data |
| SCL | Input | $I^2C$ clock |

### Slave Address

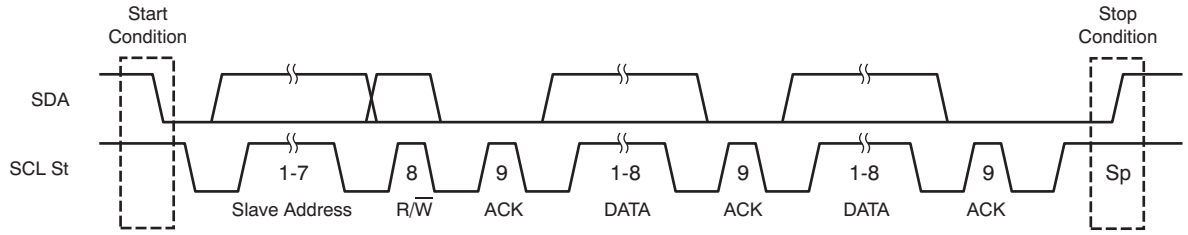
The PCM5310 has its own 7-bit slave address, as shown in Table 24.

**Table 24. Slave Address**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | R/$\overline{W}$ |

### Packet Protocol

The master device must control packet protocol, which consists of a start condition, a slave address with read/write ®/$\overline{W}$) bit, data (if write) or acknowledgement (if read), and a stop condition, as shown in Figure 45. The PCM5310 supports only a slave receiver and slave transmitter. Table 25 shows a basic $I^2C$ write operation. Table 26 shows a basic $I^2C$ read operation.




R/$\overline{W}$: Read operation if '1'; otherwise, write operation.
ACK: Acknowledgement of a byte if '0'.
DATA: 8 bits (1 byte).

**Figure 45. Basic $I^2C$ Framework**

**Table 25. Basic $I^2C$ Write Operation**

| TRANSMITTER | M | M | M | S | M | S | M | S | M |
|---|---|---|---|---|---|---|---|---|---|
| DATA TYPE | St | Slave address | R/$\overline{W}$ | ACK | DATA | ACK | DATA | ACK | Sp |

LEGEND: M = master device, S = slave device, St = START condition, Sp = STOP condition, R/$\overline{W}$ = read/write, ACK = acknowledge.

**Table 26. Basic $I^2C$ Read Operation**

| TRANSMITTER | M | M | M | S | M | S | M | S | M |
|---|---|---|---|---|---|---|---|---|---|
| DATA TYPE | St | Slave address | R/$\overline{W}$ | ACK | DATA | NACK | DATA | NACK | Sp |

LEGEND: M = master device, S = slave device, St = START condition, Sp = STOP condition, R/$\overline{W}$ = read/write, ACK = acknowledge, NACK = not acknowledge.

### Write Operation

The master can write to any PCM5310 register in a single access. The master sends a PCM5310 slave address with a write bit, a register address, and data. When undefined registers are accessed, the PCM5310 does not send any acknowledgement. Table 27 shows the framework for a write operation.

**Table 27. Framework for Write Operation**

| **TRANSMITTER** | M | M | M | S | M | S | M | S | M |
|---|---|---|---|---|---|---|---|---|---|
| **DATA TYPE** | St | Slave address | $\overline{W}$ | ACK | Register address | ACK | Write data | ACK | Sp |

LEGEND: M = master device, S = slave device, St = start condition, Sp = stop condition, $\overline{W}$ = write, ACK = acknowledge.

### Read Operation

The master can read any PCM5310 register. The value of the register address is stored in an indirect index register in advance. The master sends the PCM5310 slave address with a read bit after storing the register address. The PCM5310 then transfers the data to the address specified by the index register. Table 28 shows the framework for a read operation.

**Table 28. Framework for Read Operation**

| **TRANSMITTER** | M | M | M | S | M | S | M | M | M | S | S | M | M |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **DATA TYPE** | St | Slave address | $\overline{W}$ | ACK | Register address | ACK | Sr | Slave address | R | ACK | Read data | NACK | Sp |

LEGEND: M = master device, S = slave device, St = START condition, Sr = repeated START condition, Sp = STOP condition, $\overline{W}$ = write, R = read, ACK = acknowledge, NACK = not acknowledge.

## I²C Timing Diagram

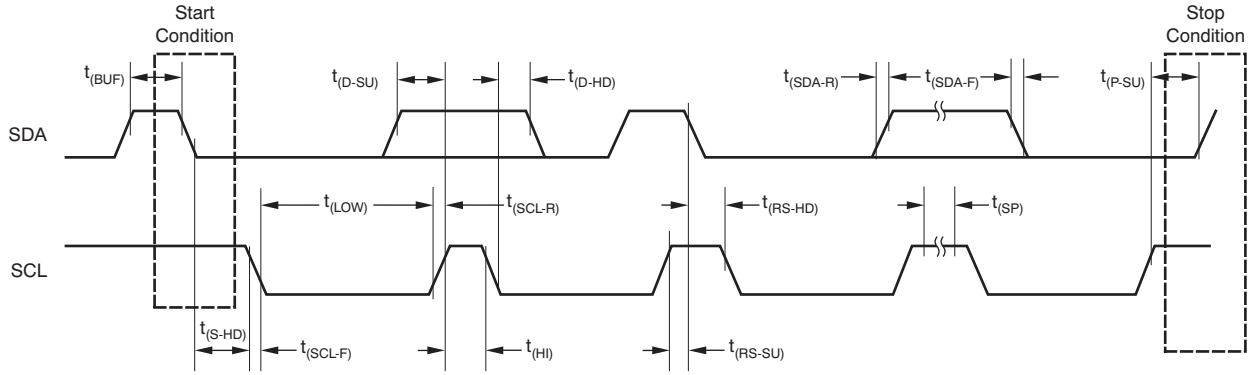



**Figure 46. I²C Timing**

**Table 29. Timing Characteristics for Figure 46**

| PARAMETER | | I²C SPECIFICATION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | Standard | | 100 | kHz |
| $t_{(BUF)}$ | Bus free time between STOP and START condition | Standard | 4.7 | | µs |
| $t_{(LOW)}$ | SCL clock low period | Standard | 4.7 | | µs |
| $t_{(HI)}$ | SCL clock high period | Standard | 4 | | µs |
| $t_{(RS-SU)}$ | START condition setup time | Standard | 4.7 | | µs |
| $t_{(S-HD)}$ | START condition hold time | Standard | 4 | | µs |
| $t_{(D-SU)}$ | Data setup time | Standard | 250 | | ns |
| $t_{(D-HD)}$ | Data hold time | Standard | 0 | 900 | ns |
| $t_{(SCL-R)}$ | SCL signal rise time | Standard | 20 + 0.1 $C_B$ | 1000 | ns |
| $t_{(SCL-R1)}$ | Rise time of SCL signal after a repeated START condition and after an acknowledge bit | Standard | 20 + 0.1 $C_B$ | 1000 | ns |
| $t_{(SCL-F)}$ | SCL signal fall time | Standard | 20 + 0.1 $C_B$ | 1000 | ns |
| $t_{(SDA-R)}$ | SDA signal rise time | Standard | 20 + 0.1 $C_B$ | 1000 | ns |
| $t_{(SDA-F)}$ | SDA signal fall time | Standard | 20 + 0.1 $C_B$ | 1000 | ns |
| $t_{(P-SU)}$ | STOP condition setup time | Standard | 4 | | µs |
| $C_B$ | Capacitive load for SDA and SCL line | | | 400 | pF |
| $t_{(SP)}$ | Suppressed spike pulse duration | | | 25 | ns |

## REGISTER MAP

The mode control register map is shown in Table 30. Each register includes an index (or address) indicated by the IDX[6:0] bits.

**Table 30. Mode Control Register Map**

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 01 | 01h | Reset function | MRST | SRST | RSV(1) | RSV | RSV | RSV | RSV | RSV |
| 08 | 08h | GPIO pin output control | RSV | RSV | RSV | RSV | RSV | GPO3 | GPO2 | GPO1 |
| 09 | 09h | GPIO PORT-1 selection | RSV | RSV | RSV | GSL1[4:0] | | | | |
| 10 | 0Ah | GPIO PORT-2 selection | RSV | RSV | RSV | GSL2[4:0] | | | | |
| 11 | 0Bh | GPIO PORT-3 selection | RSV | RSV | RSV | GSL3[4:0] | | | | |
| 12 | 0Ch | Not assigned | RSV | RSV | RSV | RSV | RSV | RSV | RSV | RSV |
| 13 | 0Dh | Headphone short-circuit protection enable/disable | RSV | SRCR | SHCR | SPDR | RSV | SRCL | SHCL | SPDL |
| 14 | 0Eh | Headphone short-circuit protection detect time | RSV | RSV | SDTR[1:0] | | RSV | RSV | SDTL[1:0] | |
| 15 | 0Fh | Headphone short-circuit protection release time, auto control | RSV | SADR | SRTR[1:0] | | RSV | SADL | SRTL[1:0] | |
| 16 | 10h | Headphone short-circuit protection status read | RSV | RSV | RSV | SSHR | RSV | RSV | RSV | SSHL |
| 17 | 11h | Power up/down (bias) | PBIS | RSV | RSV | RSV | RSV | PDCF[1:0] | | PDCS |
| 18 | 12h | Power up/down (analog), power up/down time | RSV | PABE | PAFE | PCOM | RSV | PDTM[2:0] | | |
| 19 | 13h | Mute control linked to AMUTE pin | MD12 | MD34 | MHPR | MHPL | ML2R | ML2L | ML1R | ML1L |
| 20 | 14h | Analog input mux selection for ADC12 | RSV | AX1R[2:0] | | | RSV | AX1L[2:0] | | |
| 21 | 15h | Analog input mux selection for ADC34 | RSV | AX2R[2:0] | | | RSV | AX2L[2:0] | | |
| 22 | 16h | Analog input gain control for ADC12 | RSV | RSV | AG1R[1:0] | | RSV | RSV | AG1L[1:0] | |
| 23 | 17h | Analog input gain control for ADC12 | RSV | RSV | AG2R[1:0] | | RSV | RSV | AG2L[1:0] | |
| 24 | 18h | Analog output mux selection for line output 1 | AL1R[3:0] | | | | AL1L[3:0] | | | |
| 25 | 19h | Analog output mux selection for line output 2 | AL2R[3:0] | | | | AL2L[3:0] | | | |
| 26 | 1Ah | Analog output mux selection for headphone output | AHPR[3:0] | | | | AHPL[3:0] | | | |
| 27 | 1Bh | Gain control for line output | GL2R[1:0] | | GL2L[1:0] | | GL1R[1:0] | | GL1L[1:0] | |
| 28 | 1Ch | 2.0 $V_{RMS}$ and 2.4 $V_{RMS}$ selection for line output | RSV | RSV | RSV | G242 | RSV | RSV | RSV | G241 |
| 29 | 1Dh | Clock halt detection control | RSV | RSV | RSV | RSV | RSV | RSV | ACTH | CHDE |
| 30 | 1Eh | Headphone output volume control | HUPE | RSV | HSUR | HSUL | RSV | RSV | RSV | HZRS |
| 31 | 1Fh | Headphone mute and volume level setting for R-channel | HMUL | HVOL[6:0] | | | | | | |
| 32 | 20h | Headphone mute and volume level setting for L-channel | HMUR | HVOR[6:0] | | | | | | |
| 33 | 21h | System clock output disable | RSV | RSV | SC6D | SC5D | SC4D | RSV | SC2D | SC1D |
| 34 | 22h | LRCK and BCK output disable at master mode | RSV | RSV | LB6D | LB5D | LB4D | LB3D | LB2D | LB1D |
| 35 | 23h | Read internal flag | RSV | RD12FS[2:0] | | | RHMR | RHML | RSV | RHPI |
| 36 | 24h | Read internal flag | RSV | RD34FS[2:0] | | | RDM4 | RDM3 | RDM2 | RDM1 |
| 37 | 25h | Read internal flag | RSV | RA12FS[2:0] | | | RAM4 | RAM3 | RAM2 | RAM1 |
| 38 | 26h | Read internal flag | RSV | RA34FS[2:0] | | | RDZ4 | RDZ3 | RDZ2 | RDZ1 |
| 39 | 27h | Read internal flag | CGLD | RSV | RHZR | RHZL | RAZ4 | RAZ3 | RAZ2 | RAZ1 |
| 40 | 28h | Digital attenuation and mute control for DAC12 | D12E | RSV | DUC2 | DUC1 | RSV | RSV | RSV | DZ12 |
| 41 | 29h | Digital gain boost and digital soft mute for DAC12 | RSV | RSV | RSV | RSV | DB12[1:0] | | DMU2 | DMU1 |
| 42 | 2Ah | Digital attenuation level setting for DAC12 L-channel | DAT1[7:0] | | | | | | | |
| 43 | 2Bh | Digital attenuation level setting for DAC12 R-channel | DAT2[7:0] | | | | | | | |
| 44 | 2Ch | Master/slave interface format for DAC12 | DMS12[3:0] | | | | RSV | RSV | DFM12[1:0] | |
| 45 | 2Dh | De-emphasis filter control for DAC12 | RSV | RSV | RSV | RSV | DM12 | RSV | DF12[1:0] | |
| 46 | 2Eh | Power up/down, oversampling rate control for DAC12 | PD12 | RSV | OV12[1:0] | | ZR12 | RSV | RSV | RSV |

(1) RSV = reserved (write '0' data).

**Table 30. Mode Control Register Map (continued)**

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 50 | 32h | Digital attenuation and mute control for DAC34 | D34E | RSV | DUC4 | DUC3 | RSV | RSV | RSV | DZ34 |
| 51 | 33h | Digital gain boost and digital soft mute for DAC34 | RSV | RSV | RSV | RSV | DB34[1:0] | | DMU4 | DMU3 |
| 52 | 34h | Digital attenuation level setting for DAC34 L-channel | DAT3[7:0] | | | | | | | |
| 53 | 35h | Digital attenuation level setting for DAC34 R-channel | DAT4[7:0] | | | | | | | |
| 54 | 36h | Master/slave interface format for DAC34 | DMS34[3:0] | | | | RSV | RSV | DFM34[1:0] | |
| 55 | 37h | De-emphasis filter control for DAC34 | RSV | RSV | RSV | RSV | DM34 | RSV | DF34[1:0] | |
| 56 | 38h | Power up/down, oversampling rate control for DAC34 | PD34 | RSV | OV34[1:0] | | ZR34 | RSV | RSV | RSV |
| 80 | 50h | Digital attenuation and mute control for ADC12 | A12E | RSV | AUC2 | AUC1 | RSV | RSV | RSV | AZ12 |
| 81 | 51h | Digital soft mute for ADC12 | RSV | FS12 | RSV | RSV | RSV | RSV | AMU2 | AMU1 |
| 82 | 52h | Digital attenuation level setting for ADC12 L-channel | AAT1[7:0] | | | | | | | |
| 83 | 53h | Digital attenuation level setting for ADC12 R-channel | AAT2[7:0] | | | | | | | |
| 84 | 54h | Master/slave interface format for ADC12 | AMS12[3:0] | | | | HF12 | RSV | AFM12[1:0] | |
| 85 | 55h | Power up/down for ADC12 | PA12 | RSV | RSV | RSV | RSV | RSV | RSV | RSV |
| 90 | 5Ah | Digital attenuation and mute control for ADC34 | A34E | RSV | AUC4 | AUC3 | RSV | RSV | RSV | AZ34 |
| 91 | 5Bh | Digital soft mute for ADC34 | RSV | FS34 | RSV | RSV | RSV | RSV | AMU4 | AMU3 |
| 92 | 5Ch | Digital attenuation level setting for ADC34 L-channel | AAT3[7:0] | | | | | | | |
| 93 | 5Dh | Digital attenuation level setting for ADC34 R-channel | AAT4[7:0] | | | | | | | |
| 94 | 5Eh | Master/slave, interface format for ADC34 | AMS34[3:0] | | | | HF34 | RSV | AFM34[1:0] | |
| 95 | 5Fh | Power up/down for ADC34 | PA34 | RSV | RSV | RSV | RSV | RSV | RSV | RSV |
| 101 | 65h | LRCK/BCK selection of PORT-1 and PORT-2 | LBS2[3:0] | | | | LBS1[3:0] | | | |
| 102 | 66h | DATA selection of PORT-1 and PORT-2 | DTS2[3:0] | | | | DTS1[3:0] | | | |
| 103 | 67h | SCK selection of PORT-1 and PORT-2 | RSV | SCS2[2:0] | | | RSV | SCS1[2:0] | | |
| 104 | 68h | LRCK/BCK selection of PORT-3 and PORT-4 | LBS4[3:0] | | | | LBS3[3:0] | | | |
| 105 | 69h | DATA selection of PORT-3 and PORT-4 | DTS4[3:0] | | | | DTS3[3:0] | | | |
| 106 | 6Ah | SCK selection of PORT-3 and PORT-4 | RSV | SCS4[2:0] | | | RSV | SCS3[2:0] | | |
| 107 | 6Bh | LRCK/BCK selection of PORT-5 and PORT-6 | LBS6[3:0] | | | | LBS5[3:0] | | | |
| 108 | 6Ch | DATA selection of PORT-5 and PORT-6 | DTS6[3:0] | | | | DTS5[3:0] | | | |
| 109 | 6Dh | SCK selection of PORT-5 and PORT-6 | RSV | SCS6[2:0] | | | RSV | SCS5[2:0] | | |
| 110 | 6Eh | LRCK/BCK selection of DAC12 and DAC34 | D34LB[3:0] | | | | D12LB[3:0] | | | |
| 111 | 6Fh | DATA selection of DAC12 and DAC34 | D34DT[3:0] | | | | D12DT[3:0] | | | |
| 112 | 70h | SCK selection of DAC12 and DAC34 | RSV | D34S[2:0] | | | RSV | D12S[2:0] | | |
| 113 | 71h | Not assigned | RSV | RSV | RSV | RSV | RSV | RSV | RSV | RSV |
| 114 | 72h | Not assigned | RSV | RSV | RSV | RSV | RSV | RSV | RSV | RSV |
| 115 | 73h | Not assigned | RSV | RSV | RSV | RSV | RSV | RSV | RSV | RSV |
| 116 | 74h | LRCK/BCK selection of ADC12 and ADC34 | A34LB[3:0] | | | | A12LB[3:0] | | | |
| 117 | 75h | SCK selection of ADC12 and ADC34 | RSV | A34SC[2:0] | | | RSV | A12SC[2:0] | | |
| 118 | 76h | GPIO1 and GPIO2 audio data selection | GP2S[3:0] | | | | GP1S[3:0] | | | |

## REGISTER DESCRIPTIONS

### Register 01 (01h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 01 | 01h | Reset function | MRST | SRST | RSV | RSV | RSV | RSV | RSV | RSV |

#### MRST: Reset of All Registers Except for Other Internal Circuit

This bit enables the reset signal for register data only. All registers are initialized to default data by setting MRST = '0'. After the reset sequence completes, MRST is automatically set to '1'.

Default value: 1

| | |
|---|---|
| 0 | Reset (set to '0' automatically after set to '1') |
| 1 | Not reset (default) |

#### SRST: Reset of All Internal Circuits Including All Registers

This bit enables the internal system reset. All circuits including the registers are initialized by setting SRST = '0'. After completing the reset sequence, SRST is automatically set to '1'.

Default value: 1

| | |
|---|---|
| 0 | Reset (set to '0' automatically after set to '1') |
| 1 | Not reset (default) |

### Register 08 (08h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 08 | 08h | GPIO pin output control | RSV | RSV | RSV | RSV | RSV | GPO3 | GPO2 | GPO1 |
| 42 | 2Ah | Digital attenuation level setting for DAC12 L-channel | DAT1[7:0] | | | | | | | |

#### GPO1: General-Purpose Output (pin 55)

#### GPO2: General-Purpose Output (pin 56)

#### GPO3: General-Purpose Output (pin 57)

These three bits control the three GPIO pins that control external devices. These register data are effective by setting '01000', '01001', or '01010' to bits GSL1[4:0], GSL2[4:0] and GSL[4:0] of registers 9 to 11.

Default value: 0

| | |
|---|---|
| 0 | Low level output (default) |
| 1 | High level output |

### Registers 09-12 (09h-0Ch)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 09 | 09h | GPIO PORT-1 selection | RSV | RSV | RSV | GSL1[4:0] | | | | |
| 10 | 0Ah | GPIO PORT-2 selection | RSV | RSV | RSV | GSL2[4:0] | | | | |
| 11 | 0Bh | GPIO PORT-3 selection | RSV | RSV | RSV | GSL3[4:0] | | | | |
| 12 | 0Ch | Not assigned | RSV | RSV | RSV | RSV | RSV | RSV | RSV | RSV |

**GSL1[4:0]: GPO1 Function Selection (pin 55)**

**GSL2[4:0]: GPO2 Function Selection (pin 56)**

**GSL3[4:0]: GPO3 Function Selection (pin 57)**

The three GPIO pins can be used as an input flag, output flag, and logic function, as shown in Table 31.

Default value: 00000

**Table 31. GPIO Functions**

| GSL1-3[4:0] | GSL1[4:0]/GPIO1 | GSL2[4:0]/GPIO2 | GSL3[4:0]/GPIO3 |
|---|---|---|---|
| 00000 | No assigned and input mode (default) | No assigned and input mode (default) | No assigned and input mode (default) |
| 00001 | Headphone insertion detection input | Headphone insertion detection input | Headphone insertion detection input |
| 00010 | Headphone insertion detection output | Headphone insertion detection output | Headphone insertion detection output |
| 00011 | Headphone short detection status L-channel | Headphone short detection status L-channel | Headphone short detection status L-channel |
| 00100 | Headphone short detection status R-channel | Headphone short detection status R-channel | Headphone short detection status R-channel |
| 00101 | Zero flag output for digital input (DAC12) | Zero flag output for digital input (DAC12) | Zero flag output for digital input (DAC12) |
| 00110 | Zero flag output for digital input (DAC34) | Zero flag output for digital input (DAC34) | Zero flag output for digital input (DAC34) |
| 00111 | Zero flag output for digital input (DAC12 and DAC34) | Zero flag output for digital input (DAC12 and DAC34) | Zero flag output for digital input (DAC12 and DAC34) |
| 01000 | Output register data to GPIO1 pin | Output register data to GPIO1 pin | Output register data to GPIO1 pin |
| 01001 | Output register data to GPIO2 pin | Output register data to GPIO2 pin | Output register data to GPIO2 pin |
| 01010 | Output register data to GPIO3 pin | Output register data to GPIO3 pin | Output register data to GPIO3 pin |
| 01011 | AND logic (GPIO1 = output, GPIO2,3 = input) | AND logic (GPIO2 = output, GPIO1,3 = input) | AND logic (GPIO2 = output, GPIO1,3 = input) |
| 01100 | NAND logic (GPIO1 = output, GPIO2,3 = input) | NAND logic (GPIO2 = output, GPIO1,3 = input) | NAND logic (GPIO2 = output, GPIO1,3 = input) |
| 01101 | OR logic (GPIO1 = output, GPIO2,3 = input) | OR logic (GPIO2 = output, GPIO1,3 = input) | OR logic (GPIO2 = output, GPIO1,3 = input) |
| 01110 | NOR logic (GPIO1 = output, GPIO2,3 = input) | NOR logic (GPIO2 = output, GPIO1,3 = input) | NOR logic (GPIO2 = output, GPIO1,3 = input) |
| 01111 | Buffer logic (GPIO1 = output, GPIO2 = input) | Buffer logic (GPIO2 = output, GPIO1 = input) | Buffer logic (GPIO2 = output, GPIO1 = input) |
| 10000 | Buffer logic (GPIO1 = output, GPIO3 = input) | Buffer logic (GPIO2 = output, GPIO3 = input) | Buffer logic (GPIO2 = output, GPIO3 = input) |
| 10001 | Inverter logic (GPIO1 = output, GPIO2 = input) | Inverter logic (GPIO2 = output, GPIO1 = input) | Inverter logic (GPIO2 = output, GPIO1 = input) |
| 10010 | Inverter logic (GPIO1 = output, GPIO3 = input) | Inverter logic (GPIO2 = output, GPIO3 = input) | Inverter logic (GPIO2 = output, GPIO3 = input) |
| Others | Reserved | Reserved | Reserved |

### Registers 13-16 (0Dh-10h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 13 | 0Dh | Headphone short-circuit protection enable/disable | RSV | SRCR | SHCR | SPDR | RSV | SRCL | SHCL | SPDL |
| 14 | 0Eh | Headphone short-circuit protection detect time | RSV | RSV | SDTR[1:0] | | RSV | RSV | SDTL[1:0] | |
| 15 | 0Fh | Headphone short-circuit protection release time, auto control | RSV | SADR | SRTR[1:0] | | RSV | SADL | SRTL[1:0] | |
| 16 | 10h | Headphone short-circuit protection status read | RSV | RSV | RSV | SSHR | RSV | RSV | RSV | SSHL |

**SRCR: Reset Short-Circuit Protection for Headphone Output R-Channel**

**SRCL: Reset Short-Circuit Protection for Headphone Output L-Channel**

These bits initialize the short-circuit protection for the headphone outputs by setting SRCR = SRCL = '1'. After completing the initialization, the data of both registers are automatically set to '1'.

Default value: 1

| | |
|---|---|
| 0 | Reset (set to '1' automatically after set to '0') |
| 1 | Normal operation (default) |

**SPDR: Short-Circuit Protection Disable for Headphone Output R-Channel**

**SPDL: Short-Circuit Protection Disable for Headphone Output L-Channel**

These bits disable the short-circuit protection for the headphone outputs.

Default value: 0

| | |
|---|---|
| 0 | Enable (default) |
| 1 | Disable |

**SDTR[1:0]: Short-Circuit Protection Detect Time Control for Headphone Output R-Channel**

**SDTL[1:0]: Short-Circuit Protection Detect Time Control for Headphone Output L-Channel**

These bits define the continuous time until a short-circuit is detected on the headphone outputs. If the short-circuit time does not reach the defined time, the PCM5310 does not enable short-circuit protection.

Default value: 11

| | |
|---|---|
| 00 | 4096 $f_S$, 85.2 ms at $f_S$ = 48 kHz |
| 01 | 8192 $f_S$, 170.4 ms at $f_S$ = 48 kHz |
| 10 | 16384 $f_S$, 340.8 ms at $f_S$ = 48 kHz |
| 11 | 32768 $f_S$, 681.6 ms at $f_S$ = 48 kHz (default) |

**SRTR[1:0]: Short-Circuit Protection Release Time Control for Headphone Output R-Channel**

**SRTL[1:0]: Short-Circuit Protection Release Time Control for Headphone Output L-Channel**

These bits define the time until the short-circuit protection is released after detecting a short-circuit.

Default value: 11

| | |
|---|---|
| 00 | 4096 $f_S$, 85.2 ms at $f_S$ = 48 kHz |
| 01 | 8192 $f_S$, 170.4 ms at $f_S$ = 48 kHz |
| 10 | 16384 $f_S$, 340.8 ms at $f_S$ = 48 kHz |
| 11 | 32768 $f_S$, 681.6 ms at $f_S$ = 48 kHz (default) |

### SADR: Short-Circuit Protection Automatic Release Disable for Headphone Output R-Channel

### SADL: Short-Circuit Protection Automatic Release Disable for Headphone Output L-Channel

These bits disable the automatic power down when a short-circuit is detected.

Default value: 0

| | |
|---|---|
| 0 | Enable (default) |
| 1 | Disable |

### SSHR: Short-Circuit Status Read for Headphone Output R-Channel

### SSHL: Short-Circuit Status Read for Headphone Output L-Channel

These bits are used to read the short-circuit status on the headphone through the $I^2C$ interface. If the status is '1', then the headphone output is in short-circuit.

Default value: 0

| | |
|---|---|
| 0 | Not shorted (default) |
| 1 | Short-circuit |

### Registers 17 and 18 (11h and 12h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 17 | 11h | Power up/down (bias) | PBIS | RSV | RSV | RSV | RSV | PDCF[1:0] | | PDCS |
| 18 | 12h | Power up/down (analog), power up/down time | RSV | PABE | PAFE | PCOM | RSV | PDTM[2:0] | | |

### PBIS: Power Up/Down Control for Analog Bias Circuit

This bit is used to power up/down the analog bias circuit.

Default value: 1

| | |
|---|---|
| 0 | Power up |
| 1 | Power down (default) |

### PDCF[1:0]: Power Up/Down Time Control

These bits set the power up/down time for each sampling rate. Set this register when the sampling rate is greater than 48 kHz at power up/down.

Default value: 00

| | |
|---|---|
| 00 | x1 (default) |
| 01 | x1/2 |
| 10 | x1/4 |
| 11 | Reserved |

### PDCS: Power Up/Down Clock Selection

The PCM5310 has six clock inputs for the four DAC and four ADC channels. The power on/off sequence starts using the DAC12 clock or the DAC34 clock. The appropriate clock source must be selected for the power up/down sequence.

Default value: 0

| | |
|---|---|
| 0 | Use the DAC12 clock for power up/down (default) |
| 1 | Use the DAC34 clock for power up/down |

### PAFE: Power Up/Down Control for Input Mux and Gain Amplifier

This bit powers up/down the input mux and the gain amplifier.

Default value: 1

| | |
|---|---|
| 0 | Power up |
| 1 | Power down (default) |

### PABE: Power Up/Down Control for Output Mux, Line Amp, and Headphone Amplifier

This bit powers up/down the output mux, the line amplifiers, and the headphone amplifier.

Default value: 1

| | |
|---|---|
| 0 | Power up |
| 1 | Power down (default) |

### PCOM: Power Up/Down Control for Common Voltage Circuit

This bit powers up/down the common voltage circuit for the ADC and DAC channels.

Default value: 1

| | |
|---|---|
| 0 | Power up |
| 1 | Power down (default) |

### PDTM[2:0]: Power Up/Down Time Control

The power-up time selection for the PCM5310 can be from ground level to common voltage for analog outputs. The power-down time selection can be from the common voltage to ground level for analog outputs at the power on/off sequence. The time described in Figure 32 is defined for a 48-kHz sampling rate. Set bits PDCF[1:0] in Register 17 when the sampling rate is more than 48 kHz at the power up/down sequence.

Default value: 001

| PDTM[2:0] | POWER-UP TIME | POWER-DOWN TIME |
|---|---|---|
| 000 | 37.5 ms | 75 ms |
| 001 | 75 ms (default) | 150 ms |
| 010 | 150 ms | 300 ms |
| 011 | 300 ms | 600 ms |
| 100 | 1000 ms | 2000 ms |
| 101 | Reserved | Reserved |
| 110 | Reserved | Reserved |
| 111 | Reserved | Reserved |

### Register 19 (13h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 19 | 13h | Mute control linked to the AMUTE pin | MD12 | MD34 | MHPR | MHPL | ML2R | ML2L | ML1R | ML1L |

**MD12: Mute Enable/Disable Linked to the AMUTE Pin for Digital Input (DAC12)**

**MD34: Mute Enable/Disable Linked to the AMUTE Pin for Digital Input (DAC34)**

The PCM5310 has a mute control pin (AMUTE, 59 pin). When AMUTE = '1' and MD12 = '1' or MD34 = '1', the digital soft mute of digital input data is enabled. When AMUTE = '0', mute is disabled.

Default value: 0

| | |
|---|---|
| 0 | Mute disabled if the AMUTE pin is at a high or lo2w level (default) |
| 1 | Mute enabled if the AMUTE pin is at a high level |

**MHPR: Mute Enable/Disable Linked AMUTE Pin for Headphone Output, R-Channel**

**MHPL: Mute Enable/Disable Linked AMUTE Pin for Headphone Output, L-Channel**

The PCM5310 has a mute control pin (AMUTE, 59 pin). When AMUTE = '1' and MHPR = '1' or MHPL = '1', the analog mute for headphone outputs HPOL and HPOR is enabled. When AMUTE = '0', mute is disabled.

Default value: 1

| | |
|---|---|
| 0 | Mute disabled if the AMUTE pin is at a high or low level |
| 1 | Mute enabled if the AMUTE pin is at a high level (default) |

**ML1R: Mute Enable/Disable Linked AMUTE Pin for Line Output 1, R-Channel**

**ML1L: Mute Enable/Disable Linked AMUTE Pin for Line Output 1, L-Channel**

The PCM5310 has a mute control pin (AMUTE, 59 pin). When AMUTE = '1' and ML1R = '1' or ML1L = '1', the analog mute for line outputs LO1L and LO1R are enabled. When AMUTE = '0', mute is disabled.

Default value: 1

| | |
|---|---|
| 0 | Mute disabled if AMUTE pin is high or low level |
| 1 | Mute enabled if AMUTE pin is high level (default) |

**MML2R: Mute Enable/Disable Linked AMUTE Pin for Line Output 2, R-Channel**

**MML2L: Mute Enable/Disable Linked AMUTE Pin for Line Output 2, L-Channel**

The PCM5310 has a mute control pin (AMUTE, 59 pin). When AMUTE = '1' and ML2R = '1' or ML2L = '1', the analog mute for line outputs LO2L and LO2R are enabled. When AMUTE = '0', mute is disabled.

Default value: 1

| | |
|---|---|
| 0 | Mute disabled if AMUTE pin is high or low level |
| 1 | Mute enabled if AMUTE pin is high level (default) |

### Registers 20 and 21 (14h and 15h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 20 | 14h | Analog input mux selection for ADC12 | RSV | AX1R[2:0] | | | RSV | AX1L[2:0] | | |
| 21 | 15h | Analog input mux selection for ADC34 | RSV | AX2R[2:0] | | | RSV | AX2L[2:0] | | |

**AX1R[2:0]: Analog Input Mux Selection for ADC12, R-Channel**

**AX1L[2:0]: Analog Input Mux Selection for ADC12, L-Channel**

**AX2R[2:0]: Analog Input Mux Selection for ADC34, R-Channel**

**AX2L[2:0]: Analog Input Mux Selection for ADC34, L-Channel**

The PCM5310 has six stereo inputs that can select one stereo input for each ADC. It is recommended to use the digital soft mute to reduce audible noise when the analog inputs are changed; see Figure 44 for details.

Default value: 000

| | |
|---|---|
| 000 | No connection (default) |
| 001 | AIN1L or AIN1R |
| 010 | AIN2L or AIN2R |
| 011 | AIN3L or AIN3R |
| 100 | AIN4L or AIN4R |
| 101 | AIN5L or AIN5R |
| 110 | AIN6L or AIN6R |
| Others | Reserved |

### Registers 22 and 23 (16h and 17h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 22 | 16h | Analog input gain control for ADC12 | RSV | RSV | AG1R[1:0] | | RSV | RSV | AG1L[1:0] | |
| 23 | 17h | Analog input gain control for ADC34 | RSV | RSV | AG2R[1:0] | | RSV | RSV | AG2L[1:0] | |

**AG1R[1:0]: Analog Input Gain Control for ADC12, R-Channel**

**AG1L[1:0]: Analog Input Gain Control for ADC12, L-Channel**

**AG2R[1:0]: Analog Input Gain Control for ADC34, R-Channel**

**AG2L[1:0]: Analog Input Gain Control for ADC34, L-Channel**

The PCM5310 has analog gain amplifiers in front of each ADC input that can be programmed to between 0 dB to +9 dB in 3-dB steps; refer to Figure 28 for details.

Default value: 00

| | |
|---|---|
| 00 | 0 dB (default) |
| 01 | 3 dB |
| 10 | 6 dB |
| 11 | 9 dB |

### Registers 24-26 (18h-1Ah)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 24 | 18h | Analog output mux selection for line output 1 | AL1R[3:0] | | | | AL1L[3:0] | | | |
| 25 | 19h | Analog output mux selection for line output 2 | AL2R[3:0] | | | | AL2L[3:0] | | | |
| 26 | 1Ah | Analog output mux selection for headphone output | AHPR[3:0] | | | | AHPL[3:0] | | | |

**AL1R[3:0]: Analog Output Mux Selection for Line Output 1, R-Channel**

**AL1L[3:0]: Analog Output Mux Selection for Line Output 1, L-Channel**

**AL2R[3:0]: Analog Output Mux Selection for Line Output 2, R-Channel**

**AL2L[3:0]: Analog Output Mux Selection for Line Output 2, L-Channel**

**AHPR[3:0]: Analog Output Mux Selection for Headphone Output, R-Channel**

**AHPL[3:0]: Analog Output Mux Selection for Headphone Output, L-Channel**

Analog outputs LO1L/LO1R, LO2L/LO2R, and HPOL/HPOR can be selected as one of all the analog inputs and DAC outputs; see Figure 29 for details.

Default value: 0000

| | |
|---|---|
| 0000 | No connection (default) |
| 0001 | AIN1L or AIN1R |
| 0010 | AIN2L or AIN2R |
| 0011 | AIN3L or AIN3R |
| 0100 | AIN4L or AIN4R |
| 0101 | AIN5L or AIN5R |
| 0110 | AIN6L or AIN6R |
| 0111 | DAC12-L-channel or DAC12-R-channel |
| 1000 | DAC34-L-channel or DAC34-R-channel |
| Others | Reserved |

### Register 27 (1Bh)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 27 | 1Bh | Gain control for line output | GL2R[1:0] | | GL2L[1:0] | | GL1R[1:0] | | GL1L[1:0] | |

**GL2R[1:0]: Gain Control for Line Output 2, R-Channel**

**GL2L[1:0]: Gain Control for Line Output 2, L-Channel**

**GL1R[1:0]: Gain Control for Line Output 1, R-Channel**

**GL1L[1:0]: Gain Control for Line Output 1, L-Channel**

The gain level for line outputs LO1L, LO1R, LO2L, and LO2R can be each be selected as 0 dB, –0.5 dB, or –1.0 dB.

Default value: 00

| | |
|---|---|
| 00 | 0 dB (default) |
| 01 | –0.5 dB |
| 10 | –1.0 dB |
| 11 | 0 dB when selecting analog input to line output |

### Register 28 (1Ch)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 28 | 1Ch | 2.0 Vrms and 2.4 Vrms selection for line output | RSV | RSV | RSV | G242 | RSV | RSV | RSV | G241 |

#### G242: 2-$V_{RMS}$ or 2.4-$V_{RMS}$ Output Mode Selection for Line Output 2

#### G241: 2-$V_{RMS}$ or 2.4-$V_{RMS}$ Output Mode Selection for Line Output 1

The line outputs can drive a 2-$V_{RMS}$ or 2.4-$V_{RMS}$ output with 10 kΩ. The 2.4-$V_{RMS}$ setting is recommend for use when the equipment requires greater than 2-$V_{RMS}$ output.

Default value: 0

| | |
|---|---|
| 0 | 2 $V_{RMS}$ (default) |
| 1 | 2.4 $V_{RMS}$ |

### Register 29 (1Dh)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 29 | 1Dh | Clock halt detection control | RSV | RSV | RSV | RSV | RSV | RSV | ACTH | CHDE |

#### ACTH: Activate Control for Clock Halt Detection

#### CHDE: Enable Clock Halt Detection

ACTH is used to control the power up/down for clock halt detection and CHDE is used to enable it. Setting ACTH = CHDE = '1' activates and enables clock halt detection.

Clock halt detection can reduce audible noise. The analog outputs are muted when the clock input to DAC12 and DAC34 is suddenly stopped.

Default value: 0

| | |
|---|---|
| ACTH = 0 | Deactivate clock halt detection (default) |
| ACTH = 1 | Activate clock halt detection |

| | |
|---|---|
| CHDE = 0 | Clock halt detection disabled (default) |
| CHDE = 1 | Clock halt detection enabled |

### Register 30 (1Eh)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 30 | 1Eh | Headphone output volume control | HUPE | RSV | HSUR | HSUL | RSV | RSV | RSV | HZRS |

**HUPE: Headphone Volume Update Control Enable**

**HSUR: Headphone Volume Setting Update for Headphone Output, R-Channel**

**HSUL: Headphone Volume Setting Update for Headphone Output, L-Channel**

**HZRS: Headphone Volume Zero Cross Enable**

The volume level of the headphone output can be changed independently to any level by setting HMUL/HMUR and HVOL[6:0]/HVOR[6:0] when HUPE = '0'. When HUPE = '1', the volume level is changed to any level at the same time when HSUR = '1' or HSUL = '1'. Both bits are automatically set to '0' after being set to '1'. HSUR and HSUL must be set to '1' for every volume level setting during HUPE = '1'.

Default value of HUPE and HZRS: 0. Default value of HSUR and HSUL: 0.

| | |
|---|---|
| HUPE = 0 | Headphone volume update control disable (default) |
| HUPE = 1 | Headphone volume update control enable |

| | |
|---|---|
| HSUR, HSUL = 0 | No update volume setting data (default) |
| HSUR, HSUL = 1 | Update volume setting data (set to '0' automatically after setting to '1') |

| | |
|---|---|
| HZRS = 0 | Headphone volume zero crossing disable (default) |
| HZRS = 1 | Headphone volume zero crossing enable |

### Register 31 and 32 (1Fh and 20h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 1Fh | Headphone mute and volume level setting for R-channel | HMUL | HVOL[6:0] | | | | | | |
| 32 | 20h | Headphone mute and volume level setting for L-channel | HMUR | HVOR[6:0] | | | | | | |

**HMUL: Headphone Volume Mute Control for L-Channel**

**HMUR: Headphone Volume Mute Control for R-Channel**

The headphone output can be independently muted to zero level when HMUL and HMUR = '1'. These settings take precedence over volume level settings by HVOL and HVOR. The headphone output may have audible *zipper* noise while changing levels. This noise can be reduced by selecting zero-crossing detection (Register 30, HZRS).

Default value: 0

| | |
|---|---|
| 0 | Mute disabled (default) |
| 1 | Mute enabled |

**HVOL[6:0]: Headphone Volume Level Control for L-Channel**

**HVOR[6:0]: Headphone Volume Level Control for R-Channel**

The headphone output can be independently programmed to between 12 dB to –70 dB in 1-dB steps. The headphone output may have audible zipper noise while changing levels. This noise can be reduced by selecting zero-crossing detection (Register 30, HZRS).

Default value: 010 1101

**Table 32. Headphone Volume Level Control**

| HVOL[6:0] HVOR[6:0] | | HP VOLUME LEVEL CONTROL | HVOL[6:0] HVOR[6:0] | | HP VOLUME LEVEL CONTROL | HVOL[6:0] HVOR[6:0] | | HP VOLUME LEVEL CONTROL |
|---|---|---|---|---|---|---|---|---|
| 111 1111 | 7F | 12 dB | 110 0010 | 62 | –17 dB | 100 0101 | 45 | –46 dB |
| 111 1110 | 7E | 11 dB | 110 0001 | 61 | –18 dB | 100 0100 | 44 | –47 dB |
| 111 1101 | 7D | 10 dB | 110 0000 | 60 | –19 dB | 100 0011 | 43 | –48 dB |
| 111 1100 | 7C | 9 dB | 101 1111 | 5F | –20 dB | 100 0010 | 42 | –49 dB |
| 111 1011 | 7B | 8 dB | 101 1110 | 5E | –21 dB | 100 0001 | 41 | –50 dB |
| 111 1010 | 7A | 7 dB | 101 1101 | 5D | –22 dB | 100 0000 | 40 | –51 dB |
| 111 1001 | 79 | 6 dB | 101 1100 | 5C | –23 dB | 011 1111 | 3F | –52 dB |
| 111 1000 | 78 | 5 dB | 101 1011 | 5B | –24 dB | 011 1110 | 3E | –53 dB |
| 111 0111 | 77 | 4 dB | 101 1010 | 5A | –25 dB | 011 1101 | 3D | –54 dB |
| 111 0110 | 76 | 3 dB | 101 1001 | 59 | –26 dB | 011 1100 | 3C | –55 dB |
| 111 0101 | 75 | 2 dB | 101 1000 | 58 | –27 dB | 011 1011 | 3B | –56 dB |
| 111 0100 | 74 | 1 dB | 101 0111 | 57 | –28 dB | 011 1010 | 3A | –57 dB |
| 111 0011 | 73 | 0 dB | 101 0110 | 56 | –29 dB | 011 1001 | 39 | –58 dB |
| 1110010 | 72 | –1 dB | 101 0101 | 55 | –30 dB | 011 1000 | 38 | –59 dB |
| 111 0001 | 71 | –2 dB | 101 0100 | 54 | –31 dB | 011 0111 | 37 | –60 dB |
| 111 0000 | 70 | –3 dB | 101 0011 | 53 | –32 dB | 011 0110 | 36 | –61 dB |
| 110 1111 | 6F | –4 dB | 101 0010 | 52 | –33 dB | 011 0101 | 35 | –62 dB |
| 110 1110 | 6E | –5 dB | 101 0001 | 51 | –34 dB | 011 0100 | 34 | –63 dB |
| 110 1101 | 6D | –6 dB | 101 0000 | 50 | –35 dB | 011 0011 | 33 | –64 dB |
| 110 1100 | 6C | –7 dB | 100 1111 | 4F | –36 dB | 011 0010 | 32 | –65 dB |
| 110 1011 | 6B | –8 dB | 100 1110 | 4E | –37 dB | 011 0001 | 31 | –66 dB |
| 110 1010 | 6A | –9 dB | 100 1101 | 4D | –38 dB | 011 0000 | 30 | –67 dB |
| 110 1001 | 69 | –10 dB | 100 1100 | 4C | –39 dB | 010 1111 | 2F | –68 dB |
| 110 1000 | 68 | –11 dB | 100 1011 | 4B | –40 dB | 010 1110 | 2E | –69 dB |
| 110 0111 | 67 | –12 dB | 100 1010 | 4A | –41 dB | 010 1101 | 2D | –70 dB (default) |
| 110 0110 | 66 | –13 dB | 100 1001 | 49 | –42 dB | 010 1100 ⋮ 000 0000 | 2C ⋮ 00 | Mute |
| 110 0101 | 65 | –14 dB | 100 1000 | 48 | –43 dB | | | |
| 110 0100 | 64 | –15 dB | 100 0111 | 47 | –44 dB | | | |
| 110 0011 | 63 | –16 dB | 100 0110 | 46 | –45 dB | | | |

### Register 33 (21h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 33 | 21h | System clock output disable | RSV | RSV | SC6D | SC5D | SC4D | SC3D | SC2D | SC1D |

**SC6D: SCK6 Output Disable**

**SC5D: SCK5 Output Disable**

**SC4D: SCK4 Output Disable**

**SC3D: SCK3 Output Disable**

**SC2D: SCK2 Output Disable**

**SC1D: SCK1 Output Disable**

These bits are used to disable (low-level output) the clock ports (SCK1, SCK2, SCK3, SCK4, SCK5 and SCK6) in output mode. It is necessary to use these bits with Register 103 (SCS2[2:0], SCS1[2:0]), Register 106 (SCS4[2:0], SCS3[2:0]), and Register 109 (SCS6[2:0], SCS5[2:0]). Each clock port is set to input mode at the default setting.

Default value: 1

| | |
|---|---|
| 0 | Normal output |
| 1 | Disable, low-level output (default) |

### Register 34 (22h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 34 | 22h | LRCK and BCK output disable at master mode | RSV | RSV | LB6D | LB5D | LB4D | LB3D | LB2D | LB1D |

**LB6D: LRCK6 and BCK6 Output Disable**

**LB5D: LRCK5 and BCK5 Output Disable**

**LB4D: LRCK4 and BCK4 Output Disable**

**LB3D: LRCK3 and BCK3 Output Disable**

**LB2D: LRCK2 and BCK2 Output Disable**

**LB1D: LRCK1 and BCK1 Output Disable**

These bits are used to disable (low-level output) the LRCK/BCK ports (LRCK1/BCK1, LRCK2/BCK2, LRCK3/BCK3, LRCK4/BCK4, LRCK5/BCK5 and LRCK6/BCK6) in output mode. It is necessary to use these bits with Register 101 (LBS2[3:0], LBS1[3:0]), Register 104 (LBS4[3:0], LBS3[3:0]), and Register 107 (LBS6[3:0], LBS5[3:0]). Each LRCK/BCK port is set to input mode at the default setting.

Default value: 1

| | |
|---|---|
| 0 | Normal output |
| 1 | Disable, low-level output (default) |

### Registers 35-39 (23h-27h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 35 | 23h | Read internal flag | RSV | RD12FS[2:0] | | | RHMR | RHML | RSV | RHPI |
| 36 | 24h | Read internal flag | RSV | RD34FS[2:0] | | | RDM4 | RDM3 | RDM2 | RDM1 |
| 37 | 25h | Read internal flag | RSV | RA12FS[2:0] | | | RAM4 | RAM3 | RAM2 | RAM1 |
| 38 | 26h | Read internal flag | RSV | RA34FS[2:0] | | | RDZ4 | RDZ3 | RDZ2 | RDZ1 |
| 39 | 27h | Read internal flag | CGLD | RSV | RHZR | RHZL | RAZ4 | RAZ3 | RAZ2 | RAZ1 |

**RD12FS[2:0]: Read System Clock $f_S$ Rate Detection Status for DAC12**

**RD34FS[2:0]: Read System Clock $f_S$ Rate Detection Status for DAC34**

**RA12FS[2:0]: Read System Clock $f_S$ Rate Detection Status for ADC12**

**RA34FS[2:0]: Read System Clock $f_S$ Rate Detection Status for ADC34**

The PCM5310 includes automatic clock rate detection, which provides a divided clock to the ADC and DAC channels. The result of the detected clock rate can be read through the $I^2C$ port.

Default value: 111

| | |
|---|---|
| 000 | Reserved |
| 001 | 128 $f_S$ (default) |
| 010 | 192 $f_S$ |
| 011 | 256 $f_S$ |
| 100 | 384 $f_S$ |
| 101 | 512 $f_S$ |
| 110 | 768 $f_S$ |
| 111 | Reserved (default) |

**RHMR: Read Mute Status for Headphone Output R-Channel**

**RHML: Read Mute Status for Headphone Output L-Channel**

These bits are used to read the mute status of the headphone output. The results can be read through the $I^2C$ port.

Default value: 0

| | |
|---|---|
| 0 | Mute disabled (default) |
| 1 | Mute enabled |

**RHPI: Read Headphone Insertion Detection Status for Headphone Output**

This bit is used to read the headphone output insertion detection status through the $I^2C$ port. Headphone insertion is set by Register 09 to Register 11 (GSL1[4:0], GSL2[4:0], GSL3[4:0]) with the GPIO port.

Default value: 0

| | |
|---|---|
| 0 | Headphone not inserted (default) |
| 1 | Headphone inserted |

**RDM4: Read Digital Mute Status for DAC34, R-Channel**

**RDM3: Read Digital Mute Status for DAC34, L-Channel**

**RDM2: Read Digital Mute Status for DAC12, R-Channel**

**RDM1: Read Digital Mute Status for DAC12, L-Channel**

These bits are used to read the digital soft mute status for each DAC channel through the $I^2C$ port.

Default value: 1

| | |
|---|---|
| 0 | Mute disabled |
| 1 | Mute enabled (default) |

**RAM4: Read Digital Mute Status for ADC34, R-Channel**

**RAM3: Read Digital Mute Status for ADC34, L-Channel**

**RAM2: Read Digital Mute Status for ADC12, R-Channel**

**RAM1: Read Digital Mute Status for ADC12, L-Channel**

These bits are used to read the digital soft mute status for each ADC channel through the $I^2C$ port.

Default value: 1

| | |
|---|---|
| 0 | Mute disabled |
| 1 | Mute enabled (default) |

**RRHZR: Read Volume Zero Cross Time Out Status for Headphone, R-Channel**

**RHZL: Read Volume Zero Cross Time Out Status for Headphone, L-Channel**

**RDZ4: Read Digital Attenuation/Mute Zero Cross Timeout Status for DAC34, R-Channel**

**RDZ3: Read Digital Attenuation/Mute Zero Cross Timeout Status for DAC34, L-Channel**

**RDZ2: Read Digital Attenuation/Mute Zero Cross Timeout Status for DAC12, R-Channel**

**RDZ1: Read Digital Attenuation/Mute Zero Cross Timeout Status for DAC12, L-Channel**

**RAZ4: Read Digital Attenuation/Mute Zero Cross Timeout Status for ADC34, R-Channel**

**RAZ3: Read Digital Attenuation/Mute Zero Cross Timeout Status for ADC34, L-Channel**

**RAZ2: Read Digital Attenuation/Mute Zero Cross Timeout Status for ADC12, R-Channel**

**RAZ1: Read Digital Attenuation/Mute Zero Cross Timeout Status for ADC12, L-Channel**

These bits are used to read the zero-crossing timeout status of digital soft mute and digital attenuation for each ADCs and DACs channel and for headphone output volume through the $I^2C$ port.

Default value: 0

| | |
|---|---|
| 0 | not timed out (default) |
| 1 | Timed out |

**CGLD: Glitch Reduction Disable when Changing Clock Source**

This bit disables the glitch reduction circuit, which reduces audible pop noise when changing the clock input from any SCKx to SCKx.

Default value: 0

| | |
|---|---|
| 0 | Enabled (default) |
| 1 | Disabled |

### Registers 40 and 41 (28h and 29h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 40 | 28h | Digital attenuation and mute control for DAC12 | D12E | RSV | DUC2 | DUC1 | RSV | RSV | RSV | DZ12 |
| 41 | 29h | Digital gain boost and digital soft mute for DAC12 | RSV | RSV | RSV | RSV | DB12[1:0] | | DMU2 | DMU1 |

#### D12E: Digital Attenuation and Mute Update Control Enable for DAC12

#### DUC2: Digital Attenuation and Mute Setting Update for DAC12, R-Channel

#### DUC1: Digital Attenuation and Mute Setting Update for DAC12, L-Channel

The digital attenuation and mute levels of DAC12 can be changed independently to any level by setting bits DMU2 and DMU1 of Register 41, bits DAT1[7:0] of Register 42, and bits DAT2[7:0] of Register 43 when D12E = '0'. When D12E = '1', the level is changed to any level at the same time when DUC2 = '1' or DUC1 = '1'. Both bits are automatically set to '0' after being set to '1'. DUC2 and DUC1 must be set to '1' for every volume level setting while HUPE = '1'.

Default value of D12E: 1. Default value of DUC2 and DUC1: 0

| | |
|---|---|
| D12E = 0 | Digital attenuation and mute update control disabled |
| D12E = 1 | Digital attenuation and mute update control enabled (default) |

| | |
|---|---|
| DUC2, DUC1 = 0 | No update level (default) |
| DUC2, DUC1 = 1 | Update level (set to '0' automatically after setting to '1') |

#### DZ12: Digital Attenuation and Mute Zero Crossing Enable for DAC12

This bit enables zero-crossing detection, which reduces zipper noise while the DAC digital attenuator and mute settings are being changed. If no zero-crossing data are input for a $512/f_S$ period (10.6 ms at a 48-kHz sampling rate), then a timeout occurs and the PCM5310 volume level changes. Zero-crossing detection cannot be used with continuous zero and dc data.

Default value: 0

| | |
|---|---|
| 0 | Disabled (default) |
| 1 | Enabled |

#### DB12[1:0]: Digital Gain Boost for DAC12

These bits boost the gain for the digital data input to the DAC12 channels before the digital attenuation.

Default value: 00

| | |
|---|---|
| 00 | 0dB (default) |
| 01 | 6 dB |
| 10 | 12 dB |
| 11 | 18 dB |

#### DMU2: Digital Mute Control for DAC12, R-Channel

#### DMU1: Digital Mute Control for DAC12, L-Channel

The PCM5310 can independently mute the DACs digital input data to zero level when DMU2 and DMU1 = '1'. These settings take precedence over the attenuation level settings set by bits DAT1[7:0] and DAT2[7:0] in register 42. The analog outputs may have audible zipper noise while changing levels. This noise can be reduced by selecting zero-crossing detection (Register 40, DZ12).

Default value: 0

| | |
|---|---|
| 0 | Mute disabled (default) |
| 1 | Mute enabled |

### Registers 42 and 43 (2Ah and 2Bh)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 42 | 2Ah | Digital attenuation level setting for DAC12 L-channel | DAT1[7:0] | | | | | | | |
| 43 | 2Bh | Digital attenuation level setting for DAC12 R-channel | DAT2[7:0] | | | | | | | |

### DAT1[7:0]: Digital Attenuation Setting for DAC12, L-Channel

### DAT2[7:0]: Digital Attenuation Setting for DAC12, R-Channel

The digital attenuator of DAC12 can be independently set from 0 dB to –100 dB in 0.5-dB steps. The DAC12 output may have audible zipper noise while changing levels. This noise can be reduced by selecting zero crossing detection (Register 40, DZ12).

Default value : 1111 1111

**Table 33. Digital Attenuation Level Setting for DAC12**

| DAT1[7:0] DAT2[7:0] | | DIGITAL ATT LEVEL SETTING | DAT1[7:0] DAT2[7:0] | | DIGITAL ATT LEVEL SETTING | DAT1[7:0] DAT2[7:0] | | DIGITAL ATT LEVEL SETTING | DAT1[7:0] DAT2[7:0] | | DIGITAL ATT LEVEL SETTING |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1111 1111 | FF | 0 dB (default) | 1100 1100 | CC | –25.5 dB | 1001 1001 | 99 | – 51 dB | 0110 0110 | 66 | –76.5 dB |
| 1111 1110 | FE | –0.5 dB | 1100 1011 | CB | –26 dB | 1001 1000 | 98 | –51.5 dB | 0110 0101 | 65 | –77 dB |
| 1111 1101 | FD | –1 dB | 1100 1010 | CA | –26.5 dB | 1001 0111 | 97 | –52 dB | 0110 0100 | 64 | –77.5 dB |
| 1111 1100 | FC | –1.5 dB | 1100 1001 | C9 | –27 dB | 1001 0110 | 96 | –52.5 dB | 0110 0011 | 63 | –78 dB |
| 1111 1011 | FB | –2 dB | 1100 1000 | C8 | –27.5 dB | 1001 0101 | 95 | –53 dB | 0110 0010 | 62 | –78.8 dB |
| 1111 1010 | FA | –2.5 dB | 1100 0111 | C7 | –28 dB | 1001 0100 | 94 | –53.5 dB | 0110 0001 | 61 | –79 dB |
| 1111 1001 | F9 | –3 dB | 1100 0110 | C6 | –28.5 dB | 1001 0011 | 93 | –54 dB | 0110 0000 | 60 | –79.5 dB |
| 1111 1000 | F8 | –3.5 dB | 1100 0101 | C5 | –29 dB | 1001 0010 | 92 | –54.5 dB | 0101 1111 | 5F | –80 dB |
| 1111 0111 | F7 | –4 dB | 1100 0100 | C4 | –29.5 dB | 1001 0001 | 91 | –55 dB | 0101 1110 | 5E | –80.5 dB |
| 1111 0110 | F6 | –4.5 dB | 1100 0011 | C3 | –30 dB | 1001 0000 | 90 | –55.5 dB | 0101 1101 | 5D | –81 dB |
| 1111 0101 | F5 | –5 dB | 1100 0010 | C2 | –30.5 dB | 1000 1111 | 8F | –56 dB | 0101 1100 | 5C | –81.5 dB |
| 1111 0100 | F4 | –5.5 dB | 1100 0001 | C1 | –31 dB | 1000 1110 | 8E | –56.5 dB | 0101 1011 | 5B | –82 dB |
| 1111 0011 | F3 | –6 dB | 1100 0000 | C0 | –31.5 dB | 1000 1101 | 8D | –57 dB | 0101 1010 | 5A | –82.5 dB |
| 1111 0010 | F2 | –6.5 dB | 1011 1111 | BF | –32 dB | 1000 1100 | 8C | –57.5 dB | 0101 1001 | 59 | –83 dB |
| 1111 0001 | F1 | –7 dB | 1011 1110 | BE | –32.5 dB | 1000 1011 | 8B | –58 dB | 0101 1000 | 58 | –83.5 dB |
| 1111 0000 | F0 | –7.5 dB | 1011 1101 | BD | –33 dB | 1000 1010 | 8A | –58.5 dB | 0101 0111 | 57 | –84 dB |
| 1110 1111 | EF | –8 dB | 1011 1100 | BC | –33.5 dB | 1000 1001 | 89 | –59 dB | 0101 0110 | 56 | –84.5 dB |
| 1110 1110 | EE | –8.5 dB | 1011 1011 | BB | –34 dB | 1000 1000 | 88 | –59.5 dB | 0101 0101 | 55 | –85 dB |
| 1110 1101 | ED | –9 dB | 1011 1010 | BA | –34.5 dB | 1000 0111 | 87 | –60 dB | 0101 0100 | 54 | –85.5 dB |
| 1110 1100 | EC | –9.5 dB | 1011 1001 | B9 | –35 dB | 1000 0110 | 86 | –60.5 dB | 0101 0011 | 53 | –86 dB |
| 1110 1011 | EB | –10 dB | 1011 1000 | B8 | –35.5 dB | 1000 0101 | 85 | –61 dB | 0101 0010 | 52 | –86.5 dB |
| 1110 1010 | EA | –10.5 dB | 1011 0111 | B7 | –36 dB | 1000 0100 | 84 | –61.5 dB | 0101 0001 | 51 | –87 dB |
| 1110 1001 | E9 | –11 dB | 1011 0110 | B6 | –36.5 dB | 1000 0011 | 83 | –62 dB | 0101 0000 | 50 | –87.5 dB |
| 1110 1000 | E8 | –11.5 dB | 1011 0101 | B5 | –37 dB | 1000 0010 | 82 | –62.5 dB | 0100 1111 | 4F | –88 dB |
| 1110 0111 | E7 | –12 dB | 1011 0100 | B4 | –37.5 dB | 1000 0001 | 81 | –63 dB | 0100 1110 | 4E | –88.5 dB |
| 1110 0110 | E6 | –12.5 dB | 1011 0011 | B3 | –38 dB | 1000 0000 | 80 | –63.5 dB | 0100 1101 | 4D | –89 dB |
| 1110 0101 | E5 | –13 dB | 1011 0010 | B2 | –38.5 dB | 0111 1111 | 7F | –64 dB | 0100 1100 | 4C | –89.5 dB |
| 1110 0100 | E4 | –13.5 dB | 1011 0001 | B1 | –39 dB | 0111 1110 | 7E | –64.5 dB | 0100 1011 | 4B | –90 dB |
| 1110 0011 | E3 | –14 dB | 1011 0000 | B0 | –39.5 dB | 0111 1101 | 7D | –65 dB | 0100 1010 | 4A | –90.5 dB |
| 1110 0010 | E2 | –14.5 dB | 1010 1111 | AF | –40 dB | 0111 1100 | 7C | –65.5 dB | 0100 1001 | 49 | –91 dB |
| 1110 0001 | E1 | –15 dB | 1010 1110 | AE | –40.5 dB | 0111 1011 | 7B | –66 dB | 0100 1000 | 48 | –91.5 dB |
| 1110 0000 | E0 | –15.5 dB | 1010 1101 | AD | –41 dB | 0111 1010 | 7A | –66.5 dB | 0100 0111 | 47 | –92 dB |
| 1101 1111 | DF | –16 dB | 1010 1100 | AC | –41.5 dB | 0111 1001 | 79 | –67 dB | 0100 0110 | 46 | –92.5 dB |
| 1101 1110 | DE | –16.5 dB | 1010 1011 | AB | –42 dB | 0111 1000 | 78 | –67.5 dB | 0100 0101 | 45 | –93 dB |

**Table 33. Digital Attenuation Level Setting for DAC12 (continued)**

| DAT1[7:0] DAT2[7:0] | | DIGITAL ATT LEVEL SETTING | DAT1[7:0] DAT2[7:0] | | DIGITAL ATT LEVEL SETTING | DAT1[7:0] DAT2[7:0] | | DIGITAL ATT LEVEL SETTING | DAT1[7:0] DAT2[7:0] | | DIGITAL ATT LEVEL SETTING |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1101 1101 | DD | –17 dB | 1010 1010 | AA | –42.5 dB | 0111 0111 | 77 | –68 dB | 0100 0100 | 44 | –93.5 dB |
| 1101 1100 | DC | –17.5 dB | 1010 1001 | A9 | –43 dB | 0111 0110 | 76 | –68.5 dB | 0100 0011 | 43 | –94 dB |
| 1101 1011 | DB | –18 dB | 1010 1000 | A8 | –43.5 dB | 0111 0101 | 75 | –69 dB | 0100 0010 | 42 | –94.5 dB |
| 1101 1010 | DA | –18.5 dB | 1010 0111 | A7 | –44 dB | 0111 0100 | 74 | –69.5 dB | 0100 0001 | 41 | –95 dB |
| 1101 1001 | D9 | –19 dB | 1010 0110 | A6 | –44.5 dB | 0111 0011 | 73 | –70 dB | 0100 0000 | 40 | –95.5 dB |
| 1101 1000 | D8 | –19.5 dB | 1010 0101 | A5 | –45 dB | 0111 0010 | 72 | –70.5 dB | 0011 1111 | 3F | –96 dB |
| 1101 0111 | D7 | –20 dB | 1010 0100 | A4 | –45.5 dB | 0111 0001 | 71 | –71 dB | 0011 1110 | 3E | –96.5 dB |
| 1101 0110 | D6 | –20.5 dB | 1010 0011 | A3 | –46 dB | 0111 0000 | 70 | –71.5 dB | 0011 1101 | 3D | –97 dB |
| 1101 0101 | D5 | –21 dB | 1010 0010 | A2 | –46.5 dB | 0110 1111 | 6F | –72 dB | 0011 1100 | 3C | –97.5 dB |
| 1101 0100 | D4 | –21.5 dB | 1010 0001 | A1 | –47 dB | 0110 1110 | 6E | –72.5 dB | 0011 1011 | 3B | –98 dB |
| 1101 0011 | D3 | –22 dB | 1010 0000 | A0 | –47.5 dB | 0110 1101 | 6D | –73 dB | 0011 1010 | 3A | –98.5 dB |
| 1101 0010 | D2 | –22.5 dB | 1001 1111 | 9F | –48 dB | 0110 1100 | 6C | –73.5 dB | 0011 1001 | 39 | –99 dB |
| 1101 0001 | D1 | –23 dB | 1001 1110 | 9E | –48.5 dB | 0110 1011 | 6B | –74 dB | 0011 1000 | 38 | –99.5 dB |
| 1101 0000 | D0 | –23.5 dB | 1001 1101 | 9D | –49 dB | 0110 1010 | 6A | –74.5 dB | 0011 0111 | 37 | –100 dB |
| 1100 1111 | CF | –24 dB | 1001 1100 | 9C | –49.5 dB | 0110 1001 | 69 | –75 dB | 0011 0110 ⋮ 0000 0000 | 36 ⋮ 00 | Mute |
| 1100 1110 | CE | –24.5 dB | 1001 1011 | 9B | –50 dB | 0110 1000 | 68 | –75.5 dB | | | |
| 1100 1101 | CD | –25 dB | 1001 1010 | 9A | –50.5 dB | 0110 0111 | 67 | –76 dB | | | |

### Registers 44 and 45 (2Ch and 2Dh)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 44 | 2Ch | Master/slave interface format for DAC12 | DMS12[3:0] | | | | RSV | RSV | DFM12[1:0] | |
| 45 | 2Dh | De-emphasis filter control for DAC12 | RSV | RSV | RSV | RSV | DM12 | RSV | DF12[1:0] | |

### DMS12[3:0]: Master/Slave Audio Interface Setting for DAC12

These bits set the master or slave mode. DAC12 receives LRCK and BCK from PORT-1, PORT-2, PORT-3, PORT-4, PORT-5 or PORT-6 in slave mode, and generates LRCK and BCK from SCK in master mode.

Default value: 1000

| DMS12[3:0] | MASTER/SLAVE AUDIO INTERFACE SETTING FOR DAC12 | DMS12[3:0] | MASTER/SLAVE AUDIO INTERFACE SETTING FOR DAC12 |
|---|---|---|---|
| 0000 | Reserved | 1000 | Slave and system clock $f_S$ auto-detect mode (default) |
| 0001 | Master and system clock 768 $f_S$ | 1001 | Slave and system clock 768 $f_S$ |
| 0010 | Master and system clock 512 $f_S$ | 1010 | Slave and system clock 512 $f_S$ |
| 0011 | Master and system clock 384 $f_S$ | 1011 | Slave and system clock 384 $f_S$ |
| 0100 | Master and system clock 256 $f_S$ | 1100 | Slave and system clock 256 $f_S$ |
| 0101 | Master and system clock 192 $f_S$ | 1101 | Slave and system clock 192 $f_S$ |
| 0110 | Master and system clock 128 $f_S$ | 1110 | Slave and system clock 128 $f_S$ |
| 0111 | Reserved | 1111 | Reserved |

### DFM12[1:0]: Audio Interface Format for DAC12

These bits select the DAC12 audio data format as $I^2S$, right-justified, or left-justified.

Default value: 00

| | |
|---|---|
| 00 | 16 to 24 bits, $I^2S$ (default) |
| 01 | 16 to 24 bits, left-justified |
| 10 | 24 bits, right-justified |
| 11 | 16 bits, right-justified |

### DM12: De-Emphasis Filter Enable for DAC12

This bit enables the DAC12 de-emphasis filter. The frequency can be selected by setting bits DF12[1:0] of Register 45.

Default value: 0

| | |
|---|---|
| 0 | Disable (default) |
| 1 | Enable |

### DF12[1:0]: De-Emphasis Filter Sampling Rate Selection for DAC12

A digital de-emphasis filter is in front of the interpolation filter. One of three de-emphasis filters can be selected corresponding to the sampling rate: 32 kHz, 44.1 kHz, or 48 kHz.

Default value: 00

| | |
|---|---|
| 00 | 44.1 kHz (default) |
| 01 | 48 kHz |
| 10 | 32 kHz |
| 11 | Reserved |

### Register 46 (2Eh)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 46 | 2Eh | Power up/down, oversampling rate control for DAC12 | PD12 | RSV | OV12[1:0] | | ZR12 | RSV | RSV | RSV |

### PD12: Power Up/Down Control for DAC12

This bit controls the power up/down for DAC12, including the interpolation filter.

Default value: 1

| | |
|---|---|
| 0 | Power up |
| 1 | Power down (default) |

### OV12[1:0]: Oversampling Rate Control for DAC12

These bits are used to control the oversampling rate of the DAC12 delta-sigma modulator.

Default value: 01

| | SYSTEM CLOCK RATE | | |
|---|---|---|---|
| OV12 | 128 $f_S$, 192 $f_S$ | 256 $f_S$, 384 $f_S$ | 128 $f_S$, 192 $f_S$ |
| 00 | 16 $f_S$ | 32 $f_S$ | 64 $f_S$ |
| 01 (default) | 32 $f_S$ | 64 $f_S$ | 128 $f_S$ |
| 10 | | — | — |
| 11 | 32 $f_S$ | 128 $f_S$ (1) | 128 $f_S$ (1) |

(1) Less than $f_S$ = 48 kHz

### ZR12: Zero Flag Reverse

This bit reverses the polarity of the zero flag output. The zero flag goes from low to high after the digital input data are continuously zero during 1024 $f_S$ when ZR12 = '0'. The zero flag can output from the GPIO pins by setting Registers 9 to 11 (GSL1[4:0], GSL2[4:0], GSL3[4:0]).

Default value: 0

| | |
|---|---|
| 0 | Buffered output (default) |
| 1 | Inverted output |

### Registers 50 and 51 (32h and 33h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 50 | 32h | Digital attenuation and mute control for DAC34 | D34E | RSV | DUC4 | DUC3 | RSV | RSV | RSV | DZ34 |
| 51 | 33h | Digital gain boost and digital soft mute for DAC34 | RSV | RSV | RSV | RSV | DB34[1:0] | | DMU4 | DMU3 |

### D34E: Digital Attenuation and Mute Update Control Enable for DAC34

### DUC4: Digital Attenuation and Mute Setting Update for DAC34, R-Channel

### DUC3: Digital Attenuation and Mute Setting Update for DAC34, L-Channel

The digital attenuation and mute levels of DAC34 can be changed independently to any level by setting bits DMU4 and DMU3 in Register 51, bits DAT3[7:0] in Register 52, and bits DAT4[7:0] in Register 53 when D34E = '0'. When D34E = '1', the level is changed to any level at the same time when DUC4 = '1' or DUC3 = '1'. Both bits are automatically set to '0' after they are set to '1'. DUC4 and DUC3 must be set to '1' for every volume level setting while D34E = '1'.

Default value of D34E: 1. Default value of DUC4 and DUC3: 0

| | |
|---|---|
| D34E = 0 | Digital attenuation and mute update control disabled |
| D34E = 1 | Digital attenuation and mute update control enabled (default) |

| | |
|---|---|
| DUC4, DUC3 = 0 | No update level (default) |
| DUC4, DUC3 = 1 | Update level (set to '0' automatically after setting to '1') |

### DZ34: Digital Attenuation and Mute Zero Cross Enable for DAC34

This bit enables zero-crossing detection, which reduces zipper noise while the DAC digital attenuator and mute settings are being changed. If no zero-crossing data are input for a 512/$f_S$ period (10.6 ms at a 48-kHz sampling rate), then a timeout occurs and the PCM5310 volume level changes. Zero-crossing detection cannot be used with continuous zero and dc data.

Default value: 0

| | |
|---|---|
| 0 | Disable (default) |
| 1 | Enable |

### DB34[1:0]: Digital Gain Boost for DAC34

These bits are used to boost the gain of digital data input to the DACs in front of the digital attenuator.

Default value: 00

| | |
|---|---|
| 00 | 0 dB (default) |
| 01 | 6 dB |
| 10 | 12 dB |
| 11 | 18 dB |

### DMU4: Digital Mute Control for DAC34, R-Channel

### DMU3: Digital Mute Control for DAC34, L-Channel

The PCM5310 can independently mute the DAC digital input data to a zero level when DMU4 and DMU3 = '1'. These settings take precedence over the attenuation level settings of bits DAT3[7:0] and DAT4[7:0] in registers 52 and 53. The analog outputs may have audible zipper noise while changing levels. This noise can be reduced by selecting zero-crossing detection (Register 50, DZ34).

Default value: 0

| | |
|---|---|
| 0 | Mute disabled (default) |
| 1 | Mute enabled |

### Registers 52 and 53 (34h and 35h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 52 | 34h | Digital attenuation level setting for DAC34 L-channel | DAT3[7:0] | | | | | | | |
| 53 | 35h | Digital attenuation level setting for DAC34 R-channel | DAT4[7:0] | | | | | | | |

### DAT3[7:0]: Digital Attenuation Setting for DAC34, L-Channel

### DAT4[7:0]: Digital Attenuation Setting for DAC34, R-Channel

The digital attenuator of DAC34 can be independently set from 0 dB to –100 dB in 0.5-dB steps. The DAC34 output may have audible zipper noise while changing levels. This noise can be reduced by selecting zero crossing detection (Register 50, DZ34).

Default value : 1111 1111

**Table 34. Digital Attenuation Level Setting for DAC34**

| DAT3[7:0] DAT4[7:0] | | DIGITAL ATT LEVEL SETTING | DAT3[7:0] DAT4[7:0] | | DIGITAL ATT LEVEL SETTING | DAT3[7:0] DAT4[7:0] | | DIGITAL ATT LEVEL SETTING | DAT3[7:0] DAT4[7:0] | | DIGITAL ATT LEVEL SETTING |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1111 1111 | FF | 0 dB (default) | 1100 1100 | CC | –25.5 dB | 1001 1001 | 99 | – 51 dB | 0110 0110 | 66 | –76.5 dB |
| 1111 1110 | FE | –0.5 dB | 1100 1011 | CB | –26 dB | 1001 1000 | 98 | –51.5 dB | 0110 0101 | 65 | –77 dB |
| 1111 1101 | FD | –1 dB | 1100 1010 | CA | –26.5 dB | 1001 0111 | 97 | –52 dB | 0110 0100 | 64 | –77.5 dB |
| 1111 1100 | FC | –1.5 dB | 1100 1001 | C9 | –27 dB | 1001 0110 | 96 | –52.5 dB | 0110 0011 | 63 | –78 dB |
| 1111 1011 | FB | –2 dB | 1100 1000 | C8 | –27.5 dB | 1001 0101 | 95 | –53 dB | 0110 0010 | 62 | –78.8 dB |
| 1111 1010 | FA | –2.5 dB | 1100 0111 | C7 | –28 dB | 1001 0100 | 94 | –53.5 dB | 0110 0001 | 61 | –79 dB |
| 1111 1001 | F9 | –3 dB | 1100 0110 | C6 | –28.5 dB | 1001 0011 | 93 | –54 dB | 0110 0000 | 60 | –79.5 dB |
| 1111 1000 | F8 | –3.5 dB | 1100 0101 | C5 | –29 dB | 1001 0010 | 92 | –54.5 dB | 0101 1111 | 5F | –80 dB |
| 1111 0111 | F7 | –4 dB | 1100 0100 | C4 | –29.5 dB | 1001 0001 | 91 | –55 dB | 0101 1110 | 5E | –80.5 dB |
| 1111 0110 | F6 | –4.5 dB | 1100 0011 | C3 | –30 dB | 1001 0000 | 90 | –55.5 dB | 0101 1101 | 5D | –81 dB |
| 1111 0101 | F5 | –5 dB | 1100 0010 | C2 | –30.5 dB | 1000 1111 | 8F | –56 dB | 0101 1100 | 5C | –81.5 dB |
| 1111 0100 | F4 | –5.5 dB | 1100 0001 | C1 | –31 dB | 1000 1110 | 8E | –56.5 dB | 0101 1011 | 5B | –82 dB |
| 1111 0011 | F3 | –6 dB | 1100 0000 | C0 | –31.5 dB | 1000 1101 | 8D | –57 dB | 0101 1010 | 5A | –82.5 dB |
| 1111 0010 | F2 | –6.5 dB | 1011 1111 | BF | –32 dB | 1000 1100 | 8C | –57.5 dB | 0101 1001 | 59 | –83 dB |
| 1111 0001 | F1 | –7 dB | 1011 1110 | BE | –32.5 dB | 1000 1011 | 8B | –58 dB | 0101 1000 | 58 | –83.5 dB |
| 1111 0000 | F0 | –7.5 dB | 1011 1101 | BD | –33 dB | 1000 1010 | 8A | –58.5 dB | 0101 0111 | 57 | –84 dB |
| 1110 1111 | EF | –8 dB | 1011 1100 | BC | –33.5 dB | 1000 1001 | 89 | –59 dB | 0101 0110 | 56 | –84.5 dB |
| 1110 1110 | EE | –8.5 dB | 1011 1011 | BB | –34 dB | 1000 1000 | 88 | –59.5 dB | 0101 0101 | 55 | –85 dB |
| 1110 1101 | ED | –9 dB | 1011 1010 | BA | –34.5 dB | 1000 0111 | 87 | –60 dB | 0101 0100 | 54 | –85.5 dB |
| 1110 1100 | EC | –9.5 dB | 1011 1001 | B9 | –35 dB | 1000 0110 | 86 | –60.5 dB | 0101 0011 | 53 | –86 dB |
| 1110 1011 | EB | –10 dB | 1011 1000 | B8 | –35.5 dB | 1000 0101 | 85 | –61 dB | 0101 0010 | 52 | –86.5 dB |
| 1110 1010 | EA | –10.5 dB | 1011 0111 | B7 | –36 dB | 1000 0100 | 84 | –61.5 dB | 0101 0001 | 51 | –87 dB |
| 1110 1001 | E9 | –11 dB | 1011 0110 | B6 | –36.5 dB | 1000 0011 | 83 | –62 dB | 0101 0000 | 50 | –87.5 dB |

**Table 34. Digital Attenuation Level Setting for DAC34 (continued)**

| DAT3[7:0] DAT4[7:0] | | DIGITAL ATT LEVEL SETTING | DAT3[7:0] DAT4[7:0] | | DIGITAL ATT LEVEL SETTING | DAT3[7:0] DAT4[7:0] | | DIGITAL ATT LEVEL SETTING | DAT3[7:0] DAT4[7:0] | | DIGITAL ATT LEVEL SETTING |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1110 1000 | E8 | –11.5 dB | 1011 0101 | B5 | –37 dB | 1000 0010 | 82 | –62.5 dB | 0100 1111 | 4F | –88 dB |
| 1110 0111 | E7 | –12 dB | 1011 0100 | B4 | –37.5 dB | 1000 0001 | 81 | –63 dB | 0100 1110 | 4E | –88.5 dB |
| 1110 0110 | E6 | –12.5 dB | 1011 0011 | B3 | –38 dB | 1000 0000 | 80 | –63.5 dB | 0100 1101 | 4D | –89 dB |
| 1110 0101 | E5 | –13 dB | 1011 0010 | B2 | –38.5 dB | 0111 1111 | 7F | –64 dB | 0100 1100 | 4C | –89.5 dB |
| 1110 0100 | E4 | –13.5 dB | 1011 0001 | B1 | –39 dB | 0111 1110 | 7E | –64.5 dB | 0100 1011 | 4B | –90 dB |
| 1110 0011 | E3 | –14 dB | 1011 0000 | B0 | –39.5 dB | 0111 1101 | 7D | –65 dB | 0100 1010 | 4A | –90.5 dB |
| 1110 0010 | E2 | –14.5 dB | 1010 1111 | AF | –40 dB | 0111 1100 | 7C | –65.5 dB | 0100 1001 | 49 | –91 dB |
| 1110 0001 | E1 | –15 dB | 1010 1110 | AE | –40.5 dB | 0111 1011 | 7B | –66 dB | 0100 1000 | 48 | –91.5 dB |
| 1110 0000 | E0 | –15.5 dB | 1010 1101 | AD | –41 dB | 0111 1010 | 7A | –66.5 dB | 0100 0111 | 47 | –92 dB |
| 1101 1111 | DF | –16 dB | 1010 1100 | AC | –41.5 dB | 0111 1001 | 79 | –67 dB | 0100 0110 | 46 | –92.5 dB |
| 1101 1110 | DE | –16.5 dB | 1010 1011 | AB | –42 dB | 0111 1000 | 78 | –67.5 dB | 0100 0101 | 45 | –93 dB |
| 1101 1101 | DD | –17 dB | 1010 1010 | AA | –42.5 dB | 0111 0111 | 77 | –68 dB | 0100 0100 | 44 | –93.5 dB |
| 1101 1100 | DC | –17.5 dB | 1010 1001 | A9 | –43 dB | 0111 0110 | 76 | –68.5 dB | 0100 0011 | 43 | –94 dB |
| 1101 1011 | DB | –18 dB | 1010 1000 | A8 | –43.5 dB | 0111 0101 | 75 | –69 dB | 0100 0010 | 42 | –94.5 dB |
| 1101 1010 | DA | –18.5 dB | 1010 0111 | A7 | –44 dB | 0111 0100 | 74 | –69.5 dB | 0100 0001 | 41 | –95 dB |
| 1101 1001 | D9 | –19 dB | 1010 0110 | A6 | –44.5 dB | 0111 0011 | 73 | –70 dB | 0100 0000 | 40 | –95.5 dB |
| 1101 1000 | D8 | –19.5 dB | 1010 0101 | A5 | –45 dB | 0111 0010 | 72 | –70.5 dB | 0011 1111 | 3F | –96 dB |
| 1101 0111 | D7 | –20 dB | 1010 0100 | A4 | –45.5 dB | 0111 0001 | 71 | –71 dB | 0011 1110 | 3E | –96.5 dB |
| 1101 0110 | D6 | –20.5 dB | 1010 0011 | A3 | –46 dB | 0111 0000 | 70 | –71.5 dB | 0011 1101 | 3D | –97 dB |
| 1101 0101 | D5 | –21 dB | 1010 0010 | A2 | –46.5 dB | 0110 1111 | 6F | –72 dB | 0011 1100 | 3C | –97.5 dB |
| 1101 0100 | D4 | –21.5 dB | 1010 0001 | A1 | –47 dB | 0110 1110 | 6E | –72.5 dB | 0011 1011 | 3B | –98 dB |
| 1101 0011 | D3 | –22 dB | 1010 0000 | A0 | –47.5 dB | 0110 1101 | 6D | –73 dB | 0011 1010 | 3A | –98.5 dB |
| 1101 0010 | D2 | –22.5 dB | 1001 1111 | 9F | –48 dB | 0110 1100 | 6C | –73.5 dB | 0011 1001 | 39 | –99 dB |
| 1101 0001 | D1 | –23 dB | 1001 1110 | 9E | –48.5 dB | 0110 1011 | 6B | –74 dB | 0011 1000 | 38 | –99.5 dB |
| 1101 0000 | D0 | –23.5 dB | 1001 1101 | 9D | –49 dB | 0110 1010 | 6A | –74.5 dB | 0011 0111 | 37 | –100 dB |
| 1100 1111 | CF | –24 dB | 1001 1100 | 9C | –49.5 dB | 0110 1001 | 69 | –75 dB | 0011 0110 ⋮ 0000 0000 | 36 ⋮ 00 | Mute |
| 1100 1110 | CE | –24.5 dB | 1001 1011 | 9B | –50 dB | 0110 1000 | 68 | –75.5 dB | | | |
| 1100 1101 | CD | –25 dB | 1001 1010 | 9A | –50.5 dB | 0110 0111 | 67 | –76 dB | | | |

### Registers 54 and 55 (36h and 37h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 54 | 36h | Master/slave interface format for DAC34 | DMS34[3:0] | | | | RSV | RSV | DFM34[1:0] | |
| 55 | 37h | De-emphasis filter control for DAC34 | RSV | RSV | RSV | RSV | DM34 | RSV | DF34[1:0] | |

### DMS34[3:0]: Master/Slave Audio Interface Setting for DAC34

These bits set the master or slave mode. DAC34 receives LRCK and BCK from PORT-1, PORT-2, PORT-3, PORT-4, PORT-5 or PORT-6 in slave mode, and generates LRCK and BCK from SCK in master mode.

Default value: 1000

| DMS34[3:0] | MASTER/SLAVE AUDIO INTERFACE SETTING FOR DAC34 | DMS34[3:0] | MASTER/SLAVE AUDIO INTERFACE SETTING FOR DAC34 |
|---|---|---|---|
| 0000 | Reserved | 1000 | Slave and system clock $f_S$ auto-detect mode (default) |
| 0001 | Master and system clock 768 $f_S$ | 1001 | Slave and system clock 768 $f_S$ |
| 0010 | Master and system clock 512 $f_S$ | 1010 | Slave and system clock 512 $f_S$ |
| 0011 | Master and system clock 384 $f_S$ | 1011 | Slave and system clock 384 $f_S$ |
| 0100 | Master and system clock 256 $f_S$ | 1100 | Slave and system clock 256 $f_S$ |
| 0101 | Master and system clock 192 $f_S$ | 1101 | Slave and system clock 192 $f_S$ |
| 0110 | Master and system clock 128 $f_S$ | 1110 | Slave and system clock 128 $f_S$ |
| 0111 | Reserved | 1111 | Reserved |

### DFM34[1:0]: Audio Interface Format for DAC34

These bits select the DAC34 audio data format as $I^2S$, right-justified, or left-justified.

Default value: 00

| | |
|---|---|
| 00 | 16 to 24 bits, $I^2S$ (default) |
| 01 | 16 to 24 bits, left-justified |
| 10 | 24 bits, right-justified |
| 11 | 16 bits, right-justified |

### DM34: De-Emphasis Filter Enable for DAC34

This bit enables the DAC34 de-emphasis filter. The frequency can be selected by setting bits DF34[1:0] of Register 55.

Default value: 0

| | |
|---|---|
| 0 | Disable (default) |
| 1 | Enable |

### DF34[1:0]: De-Emphasis Filter Sampling Rate Selection for DAC34

A digital de-emphasis filter is in front of the interpolation filter. One of three de-emphasis filters can be selected corresponding to the sampling rate: 32 kHz, 44.1 kHz, or 48 kHz.

Default value: 00

| | |
|---|---|
| 00 | 44.1 kHz (default) |
| 01 | 48 kHz |
| 10 | 32 kHz |
| 11 | Reserved |

### Register 56 (38h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 56 | 38h | Power up/down, oversampling rate control for DAC34 | PD34 | RSV | OV34[1:0] | | ZR34 | RSV | RSV | RSV |

### PD34: Power Up/Down Control for DAC34

This bit controls the power up/down for DAC34, including the interpolation filter.

Default value: 1

| | |
|---|---|
| 0 | Power up |
| 1 | Power down (default) |

### OV34[1:0]: Oversampling Rate Control for DAC34

These bits control the oversampling rate of the DAC34 delta-sigma modulator.

Default value: 01

| OV34 | SYSTEM CLOCK RATE | | |
|---|---|---|---|
| | **128 $f_S$, 192 $f_S$** | **256 $f_S$, 384 $f_S$** | **128 $f_S$, 192 $f_S$** |
| 00 | 16 $f_S$ | 32 $f_S$ | 64 $f_S$ |
| 01 (default) | 32 $f_S$ | 64 $f_S$ | 128 $f_S$ |
| 10 | | — | — |
| 11 | 32 $f_S$ | 128 $f_S$ (1) | 128 $f_S$ (1) |

(1) Less than $f_S$ = 48 kHz

### ZR34: Zero Flag Reverse

This bit reverses the polarity of the zero flag output. The zero flag is high after input data are zero during 1024 $f_S$ when ZR34 = '0', and is set with the GPIO port by bits GSL1[4:0], GSL2[4:0], GSL3[4:0] in registers 09 to 11.

Default value: 0

| | |
|---|---|
| 0 | Buffered output (default) |
| 1 | Inverted output |

### Registers 80 and 81 (50h and 51h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 80 | 50h | Digital attenuation and mute control for ADC12 | A12E | RSV | AUC2 | AUC1 | RSV | RSV | RSV | AZ12 |
| 81 | 51h | Digital soft mute for ADC12 | RSV | FS12 | RSV | RSV | RSV | RSV | AMU2 | AMU1 |

#### A12E: Digital Attenuation and Mute Update Control Enable for ADC12

#### AUC2: Digital Attenuation and Mute Setting Update for ADC12, R-Channel

#### AUC1: Digital Attenuation and Mute Setting Update for ADC12, L-Channel

The digital attenuation and mute levels of ADC12 can be changed independently to any level by setting bits AMU2 and AMU1 in Register 81, bits AAT1[7:0] in Register 82, and bits AAT2[7:0] in Register 83 when A12E = '0'. When A12E = '1', the level is changed to any level at the same time when AUC2 = '1' or AUC1 = '1'. Both bits are automatically set to '0' after they are set to '1'. AUC2 and AUC1 must be set to '1' for every volume level setting while A12E = '1'.

Default value of A12E: 1. Default value of AUC2 and AUC1: 0

| | |
|---|---|
| A12E = 0 | Digital attenuation and mute update control disabled |
| A12E = 1 | Digital attenuation and mute update control enabled (default) |

| | |
|---|---|
| AUC2, AUC1 = 0 | No update level (default) |
| AUC2, AUC1 = 1 | Update level (set to '1' automatically after setting to '0') |

#### AZ12: Digital Attenuation and Mute Zero Crossing Enable for ADC12

This bit enables zero-crossing detection, which reduces zipper noise while the ADC digital attenuator and mute settings are being changed. If no zero-crossing data are input for a $512/f_S$ period (10.6 ms at a 48-kHz sampling rate), then a timeout occurs and the PCM5310 volume level changes. Zero-crossing detection cannot be used with continuous zero and dc data.

Default value: 0

| | |
|---|---|
| 0 | Disable (default) |
| 1 | Enable |

#### FS12: Sampling Rate Selection for ADC12

This bit is used to select the ADS12 sampling rate. FS12 must be set to '1' when the sampling rate is greater than 48 kHz.

Default value: 0

| | |
|---|---|
| 0 | $f_S \leq 48$ kHz (default) |
| 1 | $f_S > 48$ kHz |

#### AMU2: Digital Mute Control for ADC12, R-Channel

#### AMU1: Digital Mute Control for ADC12, L-Channel

The PCM5310 can independently mute the DAC digital input data to a zero level when AMU2 and AMU1 = '1'. These settings take precedence over the attenuation level settings of bits AAT1[7:0] and AAT2[7:0] in registers 82 and 83. The analog outputs may have audible zipper noise while changing levels. This noise can be reduced by selecting zero-crossing detection (Register 80, AZ12).

Default value: 0

| | |
|---|---|
| 0 | Mute disabled (default) |
| 1 | Mute enabled |

### Registers 82 and 83 (52h and 53h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 82 | 52h | Digital attenuation level setting for ADC12 L-channel | AAT1[7:0] | | | | | | | |
| 83 | 53h | Digital attenuation level setting for ADC12 R-channel | AAT2[7:0] | | | | | | | |

### AAT1[7:0]: Digital Attenuation Setting for ADC12, L-Channel

### AAT2[7:0]: Digital Attenuation Setting for ADC12, R-Channel

The digital attenuator of ADC12 can be independently set from 20 dB to –100 dB in 0.5-dB steps. The ADC12 output may have audible zipper noise while changing levels. This noise can be reduced by selecting zero crossing detection (Register 80, AZ12).

Default value : 1101 0111

**Table 35. Digital Attenuation Level Setting for ADC12**

| AAT1[7:0] AAT2[7:0] | | DIGITAL ATT LEVEL SETTING | AAT1[7:0] AAT2[7:0] | | DIGITAL ATT LEVEL SETTING | AAT1[7:0] AAT2[7:0] | | DIGITAL ATT LEVEL SETTING | AAT1[7:0] AAT2[7:0] | | DIGITAL ATT LEVEL SETTING |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1111 1111 | FF | 20 dB | 1100 0010 | C2 | –10.5 dB | 1000 0101 | 85 | –41 dB | 0100 1000 | 48 | –71.5 dB |
| 1111 1110 | FE | 19.5 dB | 1100 0001 | C1 | –11 dB | 1000 0100 | 84 | –41.5 dB | 0100 0111 | 47 | –72 dB |
| 1111 1101 | FD | 19 dB | 1100 0000 | C0 | –11.5 dB | 1000 0011 | 83 | –42 dB | 0100 0110 | 46 | –72.5 dB |
| 1111 1100 | FC | 18.5 dB | 1011 1111 | BF | –12 dB | 1000 0010 | 82 | –42.5 dB | 0100 0101 | 45 | –73 dB |
| 1111 1011 | FB | 18 dB | 1011 1110 | BE | –12.5 dB | 1000 0001 | 81 | –43 dB | 0100 0100 | 44 | –73.5 dB |
| 1111 1010 | FA | 17.5 dB | 1011 1101 | BD | –13 dB | 1000 0000 | 80 | –43.5 dB | 0100 0011 | 43 | –74 dB |
| 1111 1001 | F9 | 17 dB | 1011 1100 | BC | –13.5 dB | 0111 1111 | 7F | –44 dB | 0100 0010 | 42 | –74.5 dB |
| 1111 1000 | F8 | 16.5 dB | 1011 1011 | BB | –14 dB | 0111 1110 | 7E | –44.5 dB | 0100 0001 | 41 | –75 dB |
| 1111 0111 | F7 | 16 dB | 1011 1010 | BA | –14.5 dB | 0111 1101 | 7D | –45 dB | 0100 0000 | 40 | –75.5 dB |
| 1111 0110 | F6 | 15.5 dB | 1011 1001 | B9 | –15 dB | 0111 1100 | 7C | –45.5 dB | 0011 1111 | 3F | –76 dB |
| 1111 0101 | F5 | 15 dB | 1011 1000 | B8 | –15.5 dB | 0111 1011 | 7B | –46 dB | 0011 1110 | 3E | –76.5 dB |
| 1111 0100 | F4 | 14.5 dB | 1011 0111 | B7 | –16 dB | 0111 1010 | 7A | –46.5 dB | 0011 1101 | 3D | –77 dB |
| 1111 0011 | F3 | 14 dB | 1011 0110 | B6 | –16.5 dB | 0111 1001 | 79 | –47 dB | 0011 1100 | 3C | –77.5 dB |
| 1111 0010 | F2 | 13.5 dB | 1011 0101 | B5 | –17 dB | 0111 1000 | 78 | –47.5 dB | 0011 1011 | 3B | –78 dB |
| 1111 0001 | F1 | 13 dB | 1011 0100 | B4 | –17.5 dB | 0111 0111 | 77 | –48 dB | 0011 1010 | 3A | –78.8 dB |
| 1111 0000 | F0 | 12.5 dB | 1011 0011 | B3 | –18 dB | 0111 0110 | 76 | –48.5 dB | 0011 1001 | 39 | –79 dB |
| 1110 1111 | EF | 12 dB | 1011 0010 | B2 | –18.5 dB | 0111 0101 | 75 | –49 dB | 0011 1000 | 38 | –79.5 dB |
| 1110 1110 | EE | 11.5 dB | 1011 0001 | B1 | –19 dB | 0111 0100 | 74 | –49.5 dB | 0011 0111 | 37 | –80 dB |
| 1110 1101 | ED | 11 dB | 1011 0000 | B0 | –19.5 dB | 0111 0011 | 73 | –50 dB | 0011 0110 | 36 | –80.5 dB |
| 1110 1100 | EC | 10.5 dB | 1010 1111 | AF | –20 dB | 0111 0010 | 72 | –50.5 dB | 0011 0101 | 35 | –81 dB |
| 1110 1011 | EB | 10 dB | 1010 1110 | AE | –20.5 dB | 0111 0001 | 71 | – 51 dB | 0011 0100 | 34 | –81.5 dB |
| 1110 1010 | EA | 9.5 dB | 1010 1101 | AD | –21 dB | 0111 0000 | 70 | –51.5 dB | 0011 0011 | 33 | –82 dB |
| 1110 1001 | E9 | 9 dB | 1010 1100 | AC | –21.5 dB | 0110 1111 | 6F | –52 dB | 0011 0010 | 32 | –82.5 dB |
| 1110 1000 | E8 | 8.5 dB | 1010 1011 | AB | –22 dB | 0110 1110 | 6E | –52.5 dB | 0011 0001 | 31 | –83 dB |
| 1110 0111 | E7 | 8 dB | 1010 1010 | AA | –22.5 dB | 0110 1101 | 6D | –53 dB | 0011 0000 | 30 | –83.5 dB |
| 1110 0110 | E6 | 7.5 dB | 1010 1001 | A9 | –23 dB | 0110 1100 | 6C | –53.5 dB | 0010 1111 | 2F | –84 dB |
| 1110 0101 | E5 | 7 dB | 1010 1000 | A8 | –23.5 dB | 0110 1011 | 6B | –54 dB | 0010 1110 | 2E | –84.5 dB |
| 1110 0100 | E4 | 6.5 dB | 1010 0111 | A7 | –24 dB | 0110 1010 | 6A | –54.5 dB | 0010 1101 | 2D | –85 dB |
| 1110 0011 | E3 | 6 dB | 1010 0110 | A6 | –24.5 dB | 0110 1001 | 69 | –55 dB | 0010 1100 | 2C | –85.5 dB |
| 1110 0010 | E2 | 5.5 dB | 1010 0101 | A5 | –25 dB | 0110 1000 | 68 | –55.5 dB | 0010 1011 | 2B | –86 dB |
| 1110 0001 | E1 | 5 dB | 1010 0100 | A4 | –25.5 dB | 0110 0111 | 67 | –56 dB | 0010 1010 | 2A | –86.5 dB |
| 1110 0000 | E0 | 4.5 dB | 1010 0011 | A3 | –26 dB | 0110 0110 | 66 | –56.5 dB | 0010 1001 | 29 | –87 dB |
| 1101 1111 | DF | 4 dB | 1010 0010 | A2 | –26.5 dB | 0110 0101 | 65 | –57 dB | 0010 1000 | 28 | –87.5 dB |
| 1101 1110 | DE | 3.5 dB | 1010 0001 | A1 | –27 dB | 0110 0100 | 64 | –57.5 dB | 0010 0111 | 27 | –88 dB |

**Table 35. Digital Attenuation Level Setting for ADC12 (continued)**

| AAT1[7:0] AAT2[7:0] | | DIGITAL ATT LEVEL SETTING | AAT1[7:0] AAT2[7:0] | | DIGITAL ATT LEVEL SETTING | AAT1[7:0] AAT2[7:0] | | DIGITAL ATT LEVEL SETTING | AAT1[7:0] AAT2[7:0] | | DIGITAL ATT LEVEL SETTING |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1101 1101 | DD | 3 dB | 1010 0000 | A0 | –27.5 dB | 0110 0011 | 63 | –58 dB | 0010 0110 | 26 | –88.5 dB |
| 1101 1100 | DC | 2.5 dB | 1001 1111 | 9F | –28 dB | 0110 0010 | 62 | –58.5 dB | 0010 0101 | 25 | –89 dB |
| 1101 1011 | DB | 2 dB | 1001 1110 | 9E | –28.5 dB | 0110 0001 | 61 | –59 dB | 0010 0100 | 24 | –89.5 dB |
| 1101 1010 | DA | 1.5 dB | 1001 1101 | 9D | –29 dB | 0110 0000 | 60 | –59.5 dB | 0010 0011 | 23 | –90 dB |
| 1101 1001 | D9 | 1 dB | 1001 1100 | 9C | –29.5 dB | 0101 1111 | 5F | –60 dB | 0010 0010 | 22 | –90.5 dB |
| 1101 1000 | D8 | 0.5 dB | 1001 1011 | 9B | –30 dB | 0101 1110 | 5E | –60.5 dB | 0010 0001 | 21 | –91 dB |
| 1101 0111 | D7 | 0 dB (default) | 1001 1010 | 9A | –30.5 dB | 0101 1101 | 5D | –61 dB | 0010 0000 | 20 | –91.5 dB |
| 1101 0110 | D6 | –0.5 dB | 1001 1001 | 99 | –31 dB | 0101 1100 | 5C | –61.5 dB | 0001 1111 | 1F | –92 dB |
| 1101 0101 | D5 | –1 dB | 1001 1000 | 98 | –31.5 dB | 0101 1011 | 5B | –62 dB | 0001 1110 | 1E | –92.5 dB |
| 1101 0100 | D4 | –1.5 dB | 1001 0111 | 97 | –32 dB | 0101 1010 | 5A | –62.5 dB | 0001 1101 | 1D | –93 dB |
| 1101 0011 | D3 | –2 dB | 1001 0110 | 96 | –32.5 dB | 0101 1001 | 59 | –63 dB | 0001 1100 | 1C | –93.5 dB |
| 1101 0010 | D2 | –2.5 dB | 1001 0101 | 95 | –33 dB | 0101 1000 | 58 | –63.5 dB | 0001 1011 | 1B | –94 dB |
| 1101 0001 | D1 | –3 dB | 1001 0100 | 94 | –33.5 dB | 0101 0111 | 57 | –64 dB | 0001 1010 | 1A | –94.5 dB |
| 1101 0000 | D0 | –3.5 dB | 1001 0011 | 93 | –34 dB | 0101 0110 | 56 | –64.5 dB | 0001 1001 | 19 | –95 dB |
| 1100 1111 | CF | –4 dB | 1001 0010 | 92 | –34.5 dB | 0101 0101 | 55 | –65 dB | 0001 1000 | 18 | –95.5 dB |
| 1100 1110 | CE | –4.5 dB | 1001 0001 | 91 | –35 dB | 0101 0100 | 54 | –65.5 dB | 0001 0111 | 17 | –96 dB |
| 1100 1101 | CD | –5 dB | 1001 0000 | 90 | –35.5 dB | 0101 0011 | 53 | –66 dB | 0001 0110 | 16 | –96.5 dB |
| 1100 1100 | CC | –5.5 dB | 1000 1111 | 8F | –36 dB | 0101 0010 | 52 | –66.5 dB | 0001 0101 | 15 | –97 dB |
| 1100 1011 | CB | –6 dB | 1000 1110 | 8E | –36.5 dB | 0101 0001 | 51 | –67 dB | 0001 0100 | 14 | –97.5 dB |
| 1100 1010 | CA | –6.5 dB | 1000 1101 | 8D | –37 dB | 0101 0000 | 50 | –67.5 dB | 0001 0011 | 13 | –98 dB |
| 1100 1001 | C9 | –7 dB | 1000 1100 | 8C | –37.5 dB | 0100 1111 | 4F | –68 dB | 0001 0010 | 12 | –98.5 dB |
| 1100 1000 | C8 | –7.5 dB | 1000 1011 | 8B | –38 dB | 0100 1110 | 4E | –68.5 dB | 0001 0001 | 11 | –99 dB |
| 1100 0111 | C7 | –8 dB | 1000 1010 | 8A | –38.5 dB | 0100 1101 | 4D | –69 dB | 0001 0000 | 10 | –99.5 dB |
| 1100 0110 | C6 | –8.5 dB | 1000 1001 | 89 | –39 dB | 0100 1100 | 4C | –69.5 dB | 0000 1111 | 0F | –100 dB |
| 1100 0101 | C5 | –9 dB | 1000 1000 | 88 | –39.5 dB | 0100 1011 | 4B | –70 dB | 0000 1110 ⋮ 0000 0000 | 0E ⋮ 00 | Mute |
| 1100 0100 | C4 | –9.5 dB | 1000 0111 | 87 | –40 dB | 0100 1010 | 4A | –70.5 dB | | | |
| 1100 0011 | C3 | –10 dB | 1000 0110 | 86 | –40.5 dB | 0100 1001 | 49 | –71 dB | | | |

### Register 84 (54h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 84 | 54h | Master/slave interface format for ADC12 | AMS12[3:0] | | | | HF12 | RSV | AFM12[1:0] | |

### AMS12[3:0]: Master/Slave Audio Interface Setting for ADC12

These bits set the master or slave mode. ADC12 receives LRCK and BCK from PORT-1, PORT-2, PORT-3, PORT-4, PORT-5 or PORT-6 in slave mode, and generates LRCK and BCK from SCK in master mode.

Default value: 1000

| AMS12[3:0] | MASTER/SLAVE AUDIO INTERFACE SETTING FOR ADC12 | AMS12[3:0] | MASTER/SLAVE AUDIO INTERFACE SETTING FOR ADC12 |
|---|---|---|---|
| 0000 | Reserved | 1000 | Slave and system clock $f_S$ auto-detect mode (default) |
| 0001 | Master and system clock 768 $f_S$ | 1001 | Slave and system clock 768 $f_S$ |
| 0010 | Master and system clock 512 $f_S$ | 1010 | Slave and system clock 512 $f_S$ |
| 0011 | Master and system clock 384 $f_S$ | 1011 | Slave and system clock 384 $f_S$ |
| 0100 | Master and system clock 256 $f_S$ | 1100 | Slave and system clock 256 $f_S$ |
| 0101 | Reserved | 1101 | Reserved |
| 0110 | Reserved | 1110 | Reserved |
| 0111 | Reserved | 1111 | Reserved |

### HF12: High-Pass Filter Disable for ADC12

This bit disables the digital high-pass filter of ADC12.

Default value: 0

| | |
|---|---|
| 0 | (0.019 $f_S$/1000) Hz (default) |
| 1 | Off |

### AFM12[1:0]: Audio Interface Format for ADC12

These bits select the ADC12 audio data format as $I^2S$, right-justified, or left-justified.

Default value: 00

| | |
|---|---|
| 00 | 16 to 24 bits, $I^2S$ (default) |
| 01 | 16 to 24 bits, left-justified |
| 10 | 24 bits, right-justified |
| 11 | 16 bits, right-justified |

### Register 85 (55h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 85 | 55h | Power up/down for ADC12 | PA12 | RSV | RSV | RSV | RSV | RSV | RSV | RSV |

#### PA12: Power Up/Down Control for ADC12

This bit controls the power up/down for ADC12, including the decimation filter.

Default value: 1

| | |
|---|---|
| 0 | Power up |
| 1 | Power down (default) |

### Register 90 (5Ah)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 90 | 5Ah | Digital attenuation and mute control for ADC34 | A34E | RSV | AUC4 | AUC3 | RSV | RSV | RSV | AZ34 |

#### A34E: Digital Attenuation and Mute Update Control Enable for ADC34

#### AUC4: Digital Attenuation and Mute Setting Update for ADC34, R-Channel

#### AUC3: Digital Attenuation and Mute Setting Update for ADC34, L-Channel

The digital attenuation and mute levels of ADC12 can be changed independently to any level by setting bits AMU4 and AMU3 in Register 91, bits AAT3[7:0] in Register 92, and bits AAT4[7:0] in Register 93 when A34E = '0'. When A34E = '1', the level is changed to any level at the same time when AUC4 = '1' or AUC3 = '1'. Both bits are automatically set to '0' after they are to '1'. AUC4 and AUC3 must be set to '1' for every volume level setting while A34E = '1'.

Default value of A34E: 1. Default value of AUC4 and AUC3: 0

| | |
|---|---|
| A34E = 0 | Digital attenuation and mute update control disabled |
| A34E = 1 | Digital attenuation and mute update control enabled (default) |

| | |
|---|---|
| AUC4, AUC3 = 0 | No update level (default) |
| AUC4, AUC3 = 1 | Update level (set to '0' automatically after setting to '1') |

#### AZ34: Digital Attenuation and Mute Zero Cross Enable for ADC34

This bit enables zero-crossing detection, which reduces zipper noise while the ADC digital attenuator and mute settings are being changed. If no zero-crossing data are input for a $512/f_S$ period (10.6 ms at a 48-kHz sampling rate), then a timeout occurs and the PCM5310 volume level changes. Zero-crossing detection cannot be used with continuous zero and dc data.

Default value: 0

| | |
|---|---|
| 0 | Disable (default) |
| 1 | Enable |

### Register 91 (5Bh)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 91 | 5Bh | Digital soft mute for ADC34 | RSV | FS34 | RSV | RSV | RSV | RSV | AMU4 | AMU3 |

#### FS34: Sampling Rate Selection for ADC34

This bit sets the ADS34 sampling rate. FS34 must be set to '1' when the sampling rate is greater than 48 kHz.

Default value: 0

| | |
|---|---|
| 0 | $f_S \leq 48$ kHz (default) |
| 1 | $f_S > 48$ kHz |

#### AMU4: Digital Mute Control for ADC34, R-Channel

#### AMU3: Digital Mute Control for ADC34, L-Channel

The PCM5310 can independently mute the DAC digital input data to a zero level when AMU4 and AMU3 = '1'. These settings take precedence over the attenuation level settings of bits AAT3[7:0] and AAT4[7:0] in registers 92 and 93. The analog outputs may have audible zipper noise while changing levels. This noise can be reduced by selecting zero-crossing detection (Register 90, AZ34).

Default value: 0

| | |
|---|---|
| 0 | Mute disabled (default) |
| 1 | Mute enabled |

### Registers 92 and 93 (5Ch and 5Dh)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 92 | 5Ch | Digital attenuation level setting for ADC34 L-channel | AAT3[7:0] | | | | | | | |
| 93 | 5Dh | Digital attenuation level setting for ADC34 R-channel | AAT4[7:0] | | | | | | | |

#### AAT3[7:0]: Digital Attenuation Setting for ADC34, L-Channel

#### AAT4[7:0]: Digital Attenuation Setting for ADC34, R-Channel

The digital attenuator of ADC34 can be independently set from 20 dB to –100 dB in 0.5-dB steps. The ADC34 output may have audible zipper noise while changing levels. This noise can be reduced by selecting zero crossing detection (Register 90, AZ34).

Default value : 1101 0111

**Table 36. Digital Attenuation Level Setting for ADC34**

| AAT1[7:0] AAT2[7:0] | | DIGITAL ATT LEVEL SETTING | AAT1[7:0] AAT2[7:0] | | DIGITAL ATT LEVEL SETTING | AAT1[7:0] AAT2[7:0] | | DIGITAL ATT LEVEL SETTING | AAT1[7:0] AAT2[7:0] | | DIGITAL ATT LEVEL SETTING |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1111 1111 | FF | 20 dB | 1100 0010 | C2 | –10.5 dB | 1000 0101 | 85 | –41 dB | 0100 1000 | 48 | –71.5 dB |
| 1111 1110 | FE | 19.5 dB | 1100 0001 | C1 | –11 dB | 1000 0100 | 84 | –41.5 dB | 0100 0111 | 47 | –72 dB |
| 1111 1101 | FD | 19 dB | 1100 0000 | C0 | –11.5 dB | 1000 0011 | 83 | –42 dB | 0100 0110 | 46 | –72.5 dB |
| 1111 1100 | FC | 18.5 dB | 1011 1111 | BF | –12 dB | 1000 0010 | 82 | –42.5 dB | 0100 0101 | 45 | –73 dB |
| 1111 1011 | FB | 18 dB | 1011 1110 | BE | –12.5 dB | 1000 0001 | 81 | –43 dB | 0100 0100 | 44 | –73.5 dB |
| 1111 1010 | FA | 17.5 dB | 1011 1101 | BD | –13 dB | 1000 0000 | 80 | –43.5 dB | 0100 0011 | 43 | –74 dB |
| 1111 1001 | F9 | 17 dB | 1011 1100 | BC | –13.5 dB | 0111 1111 | 7F | –44 dB | 0100 0010 | 42 | –74.5 dB |
| 1111 1000 | F8 | 16.5 dB | 1011 1011 | BB | –14 dB | 0111 1110 | 7E | –44.5 dB | 0100 0001 | 41 | –75 dB |
| 1111 0111 | F7 | 16 dB | 1011 1010 | BA | –14.5 dB | 0111 1101 | 7D | –45 dB | 0100 0000 | 40 | –75.5 dB |
| 1111 0110 | F6 | 15.5 dB | 1011 1001 | B9 | –15 dB | 0111 1100 | 7C | –45.5 dB | 0011 1111 | 3F | –76 dB |
| 1111 0101 | F5 | 15 dB | 1011 1000 | B8 | –15.5 dB | 0111 1011 | 7B | –46 dB | 0011 1110 | 3E | –76.5 dB |
| 1111 0100 | F4 | 14.5 dB | 1011 0111 | B7 | –16 dB | 0111 1010 | 7A | –46.5 dB | 0011 1101 | 3D | –77 dB |
| 1111 0011 | F3 | 14 dB | 1011 0110 | B6 | –16.5 dB | 0111 1001 | 79 | –47 dB | 0011 1100 | 3C | –77.5 dB |

**Table 36. Digital Attenuation Level Setting for ADC34 (continued)**

| AAT1[7:0] AAT2[7:0] | | DIGITAL ATT LEVEL SETTING | AAT1[7:0] AAT2[7:0] | | DIGITAL ATT LEVEL SETTING | AAT1[7:0] AAT2[7:0] | | DIGITAL ATT LEVEL SETTING | AAT1[7:0] AAT2[7:0] | | DIGITAL ATT LEVEL SETTING |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1111 0010 | F2 | 13.5 dB | 1011 0101 | B5 | –17 dB | 0111 1000 | 78 | –47.5 dB | 0011 1011 | 3B | –78 dB |
| 1111 0001 | F1 | 13 dB | 1011 0100 | B4 | –17.5 dB | 0111 0111 | 77 | –48 dB | 0011 1010 | 3A | –78.8 dB |
| 1111 0000 | F0 | 12.5 dB | 1011 0011 | B3 | –18 dB | 0111 0110 | 76 | –48.5 dB | 0011 1001 | 39 | –79 dB |
| 1110 1111 | EF | 12 dB | 1011 0010 | B2 | –18.5 dB | 0111 0101 | 75 | –49 dB | 0011 1000 | 38 | –79.5 dB |
| 1110 1110 | EE | 11.5 dB | 1011 0001 | B1 | –19 dB | 0111 0100 | 74 | –49.5 dB | 0011 0111 | 37 | –80 dB |
| 1110 1101 | ED | 11 dB | 1011 0000 | B0 | –19.5 dB | 0111 0011 | 73 | –50 dB | 0011 0110 | 36 | –80.5 dB |
| 1110 1100 | EC | 10.5 dB | 1010 1111 | AF | –20 dB | 0111 0010 | 72 | –50.5 dB | 0011 0101 | 35 | –81 dB |
| 1110 1011 | EB | 10 dB | 1010 1110 | AE | –20.5 dB | 0111 0001 | 71 | – 51 dB | 0011 0100 | 34 | –81.5 dB |
| 1110 1010 | EA | 9.5 dB | 1010 1101 | AD | –21 dB | 0111 0000 | 70 | –51.5 dB | 0011 0011 | 33 | –82 dB |
| 1110 1001 | E9 | 9 dB | 1010 1100 | AC | –21.5 dB | 0110 1111 | 6F | –52 dB | 0011 0010 | 32 | –82.5 dB |
| 1110 1000 | E8 | 8.5 dB | 1010 1011 | AB | –22 dB | 0110 1110 | 6E | –52.5 dB | 0011 0001 | 31 | –83 dB |
| 1110 0111 | E7 | 8 dB | 1010 1010 | AA | –22.5 dB | 0110 1101 | 6D | –53 dB | 0011 0000 | 30 | –83.5 dB |
| 1110 0110 | E6 | 7.5 dB | 1010 1001 | A9 | –23 dB | 0110 1100 | 6C | –53.5 dB | 0010 1111 | 2F | –84 dB |
| 1110 0101 | E5 | 7 dB | 1010 1000 | A8 | –23.5 dB | 0110 1011 | 6B | –54 dB | 0010 1110 | 2E | –84.5 dB |
| 1110 0100 | E4 | 6.5 dB | 1010 0111 | A7 | –24 dB | 0110 1010 | 6A | –54.5 dB | 0010 1101 | 2D | –85 dB |
| 1110 0011 | E3 | 6 dB | 1010 0110 | A6 | –24.5 dB | 0110 1001 | 69 | –55 dB | 0010 1100 | 2C | –85.5 dB |
| 1110 0010 | E2 | 5.5 dB | 1010 0101 | A5 | –25 dB | 0110 1000 | 68 | –55.5 dB | 0010 1011 | 2B | –86 dB |
| 1110 0001 | E1 | 5 dB dB | 1010 0100 | A4 | –25.5 dB | 0110 0111 | 67 | –56 dB | 0010 1010 | 2A | –86.5 dB |
| 1110 0000 | E0 | 4.5 dB | 1010 0011 | A3 | –26 dB | 0110 0110 | 66 | –56.5 dB | 0010 1001 | 29 | –87 dB |
| 1101 1111 | DF | 4 dB | 1010 0010 | A2 | –26.5 dB | 0110 0101 | 65 | –57 dB | 0010 1000 | 28 | –87.5 dB |
| 1101 1110 | DE | 3.5 dB | 1010 0001 | A1 | –27 dB | 0110 0100 | 64 | –57.5 dB | 0010 0111 | 27 | –88 dB |
| 1101 1101 | DD | 3 dB | 1010 0000 | A0 | –27.5 dB | 0110 0011 | 63 | –58 dB | 0010 0110 | 26 | –88.5 dB |
| 1101 1100 | DC | 2.5 dB | 1001 1111 | 9F | –28 dB | 0110 0010 | 62 | –58.5 dB | 0010 0101 | 25 | –89 dB |
| 1101 1011 | DB | 2 dB | 1001 1110 | 9E | –28.5 dB | 0110 0001 | 61 | –59 dB | 0010 0100 | 24 | –89.5 dB |
| 1101 1010 | DA | 1.5 dB | 1001 1101 | 9D | –29 dB | 0110 0000 | 60 | –59.5 dB | 0010 0011 | 23 | –90 dB |
| 1101 1001 | D9 | 1 dB | 1001 1100 | 9C | –29.5 dB | 0101 1111 | 5F | –60 dB | 0010 0010 | 22 | –90.5 dB |
| 1101 1000 | D8 | 0.5 dB | 1001 1011 | 9B | –30 dB | 0101 1110 | 5E | –60.5 dB | 0010 0001 | 21 | –91 dB |
| 1101 0111 | D7 | 0 dB (default) | 1001 1010 | 9A | –30.5 dB | 0101 1101 | 5D | –61 dB | 0010 0000 | 20 | –91.5 dB |
| 1101 0110 | D6 | –0.5 dB | 1001 1001 | 99 | –31 dB | 0101 1100 | 5C | –61.5 dB | 0001 1111 | 1F | –92 dB |
| 1101 0101 | D5 | –1 dB | 1001 1000 | 98 | –31.5 dB | 0101 1011 | 5B | –62 dB | 0001 1110 | 1E | –92.5 dB |
| 1101 0100 | D4 | –1.5 dB | 1001 0111 | 97 | –32 dB | 0101 1010 | 5A | –62.5 dB | 0001 1101 | 1D | –93 dB |
| 1101 0011 | D3 | –2 dB | 1001 0110 | 96 | –32.5 dB | 0101 1001 | 59 | –63 dB | 0001 1100 | 1C | –93.5 dB |
| 1101 0010 | D2 | –2.5 dB | 1001 0101 | 95 | –33 dB | 0101 1000 | 58 | –63.5 dB | 0001 1011 | 1B | –94 dB |
| 1101 0001 | D1 | –3 dB | 1001 0100 | 94 | –33.5 dB | 0101 0111 | 57 | –64 dB | 0001 1010 | 1A | –94.5 dB |
| 1101 0000 | D0 | –3.5 dB | 1001 0011 | 93 | –34 dB | 0101 0110 | 56 | –64.5 dB | 0001 1001 | 19 | –95 dB |
| 1100 1111 | CF | –4 dB | 1001 0010 | 92 | –34.5 dB | 0101 0101 | 55 | –65 dB | 0001 1000 | 18 | –95.5 dB |
| 1100 1110 | CE | –4.5 dB | 1001 0001 | 91 | –35 dB | 0101 0100 | 54 | –65.5 dB | 0001 0111 | 17 | –96 dB |
| 1100 1101 | CD | –5 dB | 1001 0000 | 90 | –35.5 dB | 0101 0011 | 53 | –66 dB | 0001 0110 | 16 | –96.5 dB |
| 1100 1100 | CC | –5.5 dB | 1000 1111 | 8F | –36 dB | 0101 0010 | 52 | –66.5 dB | 0001 0101 | 15 | –97 dB |
| 1100 1011 | CB | –6 dB | 1000 1110 | 8E | –36.5 dB | 0101 0001 | 51 | –67 dB | 0001 0100 | 14 | –97.5 dB |
| 1100 1010 | CA | –6.5 dB | 1000 1101 | 8D | –37 dB | 0101 0000 | 50 | –67.5 dB | 0001 0011 | 13 | –98 dB |
| 1100 1001 | C9 | –7 dB | 1000 1100 | 8C | –37.5 dB | 0100 1111 | 4F | –68 dB | 0001 0010 | 12 | –98.5 dB |
| 1100 1000 | C8 | –7.5 dB | 1000 1011 | 8B | –38 dB | 0100 1110 | 4E | –68.5 dB | 0001 0001 | 11 | –99 dB |
| 1100 0111 | C7 | –8 dB | 1000 1010 | 8A | –38.5 dB | 0100 1101 | 4D | –69 dB | 0001 0000 | 10 | –99.5 dB |
| 1100 0110 | C6 | –8.5 dB | 1000 1001 | 89 | –39 dB | 0100 1100 | 4C | –69.5 dB | 0000 1111 | 0F | –100 dB |
| 1100 0101 | C5 | –9 dB | 1000 1000 | 88 | –39.5 dB | 0100 1011 | 4B | –70 dB | 0000 1110 ⋮ 0000 0000 | 0E ⋮ 00 | Mute |
| 1100 0100 | C4 | –9.5 dB | 1000 0111 | 87 | –40 dB | 0100 1010 | 4A | –70.5 dB | | | |
| 1100 0011 | C3 | –10 dB | 1000 0110 | 86 | –40.5 dB | 0100 1001 | 49 | –71 dB | | | |

### Register 94 (5Eh)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 94 | 5Eh | Master/slave interface format for ADC34 | AMS34[3:0] | | | | HF34 | RSV | AFM34[1:0] | |

### AMS34[3:0]: Master/Slave Audio Interface Setting for ADC34

These bits set the master or slave mode. ADC34 receives LRCK and BCK from PORT-1, PORT-2, PORT-3, PORT-4, PORT-5 or PORT-6 in slave mode, and generates LRCK and BCK from SCK in master mode.

Default value: 1000

| AMS34[3:0] | MASTER/SLAVE AUDIO INTERFACE SETTING FOR ADC34 | AMS34[3:0] | MASTER/SLAVE AUDIO INTERFACE SETTING FOR ADC34 |
|---|---|---|---|
| 0000 | Reserved | 1000 | Slave and system clock $f_S$ auto-detect mode (default) |
| 0001 | Master and system clock 768 $f_S$ | 1001 | Slave and system clock 768 $f_S$ |
| 0010 | Master and system clock 512 $f_S$ | 1010 | Slave and system clock 512 $f_S$ |
| 0011 | Master and system clock 384 $f_S$ | 1011 | Slave and system clock 384 $f_S$ |
| 0100 | Master and system clock 256 $f_S$ | 1100 | Slave and system clock 256 $f_S$ |
| 0101 | Reserved | 1101 | Reserved |
| 0110 | Reserved | 1110 | Reserved |
| 0111 | Reserved | 1111 | Reserved |

### HF34: High-Pass Filter Disable for ADC34

This bit disables the digital high-pass filter of ADC34.

Default value: 0

| | |
|---|---|
| 0 | (0.019 $f_S$/1000) Hz (default) |
| 1 | Off |

### AFM34[1:0]: Audio Interface Format for ADC34

These bits select the ADC34 audio data format as $I^2S$, right-justified, or left-justified.

Default value: 00

| | |
|---|---|
| 00 | 16 to 24 bits, $I^2S$ (default) |
| 01 | 16 to 24 bits, left-justified |
| 10 | 24 bits, right-justified |
| 11 | 16 bits, right-justified |

### Register 95 (5Fh)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 95 | 5Fh | Power up/down for ADC34 | PA34 | RSV | RSV | RSV | RSV | RSV | RSV | RSV |

### PA34: Power Up/Down Control for ADC34

This bit controls the power up/down for ADC34, including the decimation filter.

Default value: 1

| | |
|---|---|
| 0 | Power up |
| 1 | Power down (default) |

### Register 101 (65h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 101 | 65h | LRCK/BCK selection of PORT-1 and PORT-2 | LBS2[3:0] | | | | LBS1[3:0] | | | |

### LBS2[3:0]: LRCK/BCK Selection of PORT-2 (MUX_P2BL)

These bits are used for routing LRCK and BCK of PORT-2. Any combination of LRCK1/BCK1 to LRCK6/BCK6 and LRCK/BCK of ADCs/DACs in master mode can be connected to PORT-2. Figure 47 shows a detailed diagram of PORT-2.

Default value: 0001

| | |
|---|---|
| 0000 | Output LRCK1 and BCK1 |
| 0001 | Input LRCK2 and BCK2 (default) |
| 0010 | Output LRCK3 and BCK3 |
| 0011 | Output LRCK4 and BCK4 |
| 0100 | Output LRCK5 and BCK5 |
| 0101 | Output LRCK6 and BCK6 |
| 0110 | Output LRCK and BCK from DAC12 in master mode |
| 0111 | Output LRCK and BCK from DAC34 in master mode |
| 1000 | Output LRCK and BCK from ADC12 in master mode |
| 1001 | Output LRCK and BCK from ADC34 in master mode |
| Others | Reserved |

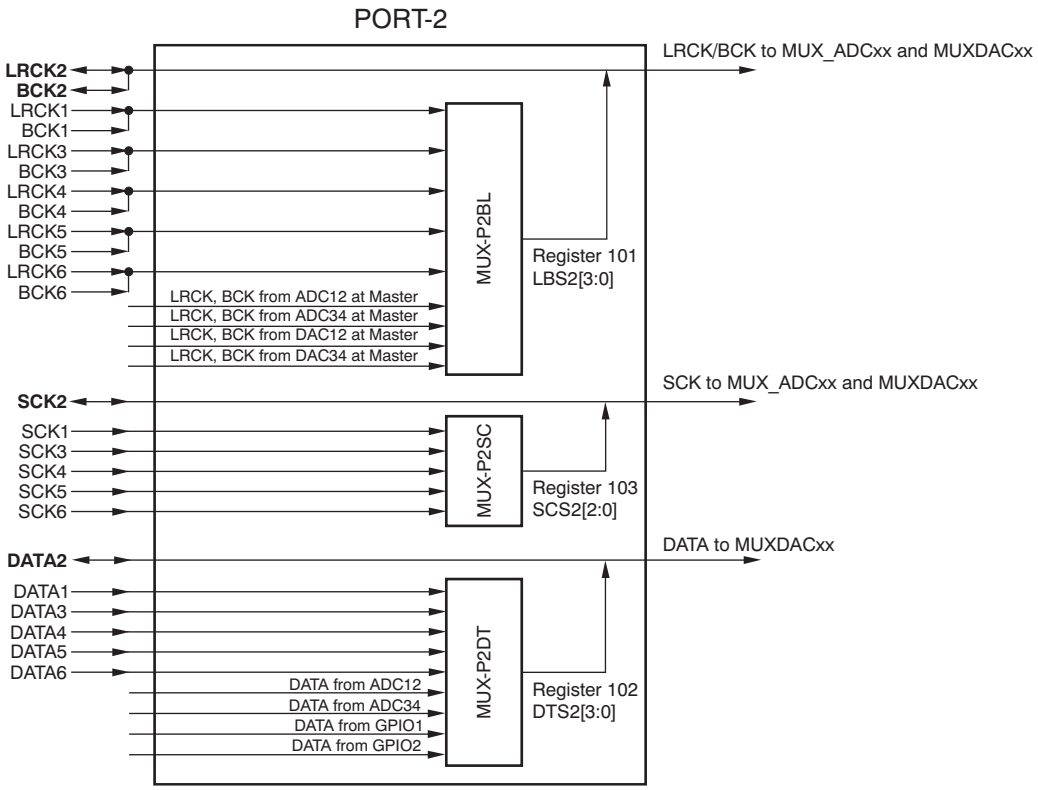



**Figure 47. Detailed Diagram of PORT-2**

### LBS1[3:0]: LRCK/BCK Selection of PORT-1 (MUX_P2BL)

These bits are used for routing LRCK and BCK of PORT-1. Any combination of LRCK1/BCK1 to LRCK6/BCK6 and LRCK/BCK of ADCs/DACs in master mode can be connected to PORT-1. Figure 48 shows a detailed diagram of PORT-1.

Default value: 0000

| | |
|---|---|
| 0000 | Input LRCK1 and BCK1 (default) |
| 0001 | Output LRCK2 and BCK2 |
| 0010 | Output LRCK3 and BCK3 |
| 0011 | Output LRCK4 and BCK4 |
| 0100 | Output LRCK5 and BCK5 |
| 0101 | Output LRCK6 and BCK6 |
| 0110 | Output LRCK and BCK from DAC12 in master mode |
| 0111 | Output LRCK and BCK from DAC34 in master mode |
| 1000 | Output LRCK and BCK from ADC12 in master mode |
| 1001 | Output LRCK and BCK from ADC34 in master mode |
| Others | Reserved |

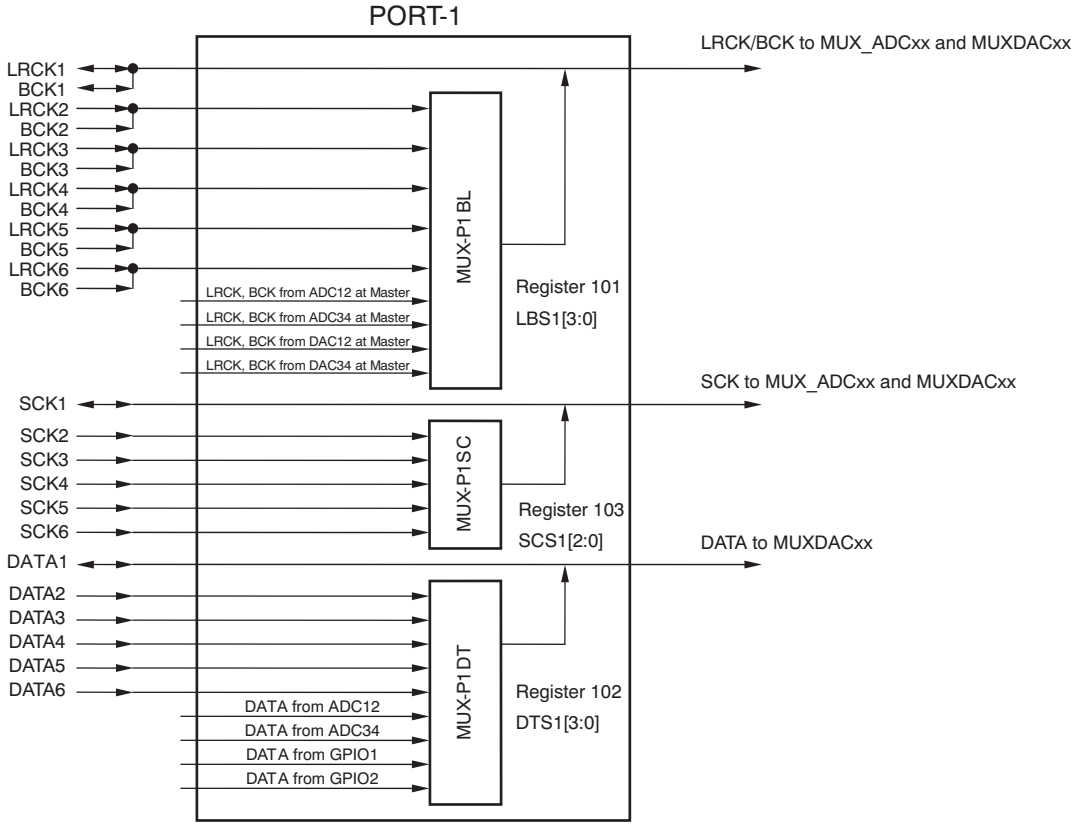



**Figure 48. Detailed Diagram of PORT-1**

### Register 102 (66h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 102 | 66h | DATA selection of PORT-1 and PORT-2 | DTS2[3:0] | | | | DTS1[3:0] | | | |

### DTS2[3:0]: DATA Selection of PORT-2 (MUX_P2DT)

These bits are used for routing DATA of PORT-2. Any combination of DATA1 to DATA6 and DATA of ADCs in master mode can be connected to PORT-2. Refer to Figure 47 for more details.

Default value: 0001

| | |
|---|---|
| 0000 | Output DATA1 |
| 0001 | Input DATA2 (default) |
| 0010 | Output DATA3 |
| 0011 | Output DATA4 |
| 0100 | Output DATA5 |
| 0101 | Output DATA6 |
| 0110 | Output GPIO1 |
| 0111 | Output GPIO2 |
| 1000 | Output DATA from ADC12 |
| 1001 | Output DATA from ADC34 |
| Others | Reserved |

### DTS1[3:0]: DATA Selection of PORT-1 (MUX_P1DT)

These bits are used for routing DATA of PORT-1. Any combination of DATA1 to DATA6 and DATA of ADCs in master mode can be connected to PORT-1. Refer to Figure 48 for more details.

Default value: 0000

| | |
|---|---|
| 0000 | Input DATA1 (default) |
| 0001 | Output DATA2 |
| 0010 | Output DATA3 |
| 0011 | Output DATA4 |
| 0100 | Output DATA5 |
| 0101 | Output DATA6 |
| 0110 | Output GPIO1 |
| 0111 | Output GPIO2 |
| 1000 | Output DATA from ADC12 |
| 1001 | Output DATA from ADC34 |
| Others | Reserved |

### Register 103 (67h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 103 | 67h | SCK selection of PORT-1 and PORT-2 | RSV | SCS2[3:0] | | | RSV | SCS1[3:0] | | |

### SCS2[3:0]: SCK Selection of PORT-2 (MUX_P2SC)

These bits are used for routing SCK of PORT-2. Any combination of SCK1 to SCK6 and SCK can be connected to PORT-2. Refer to Figure 47 for more details.

Default value: 001

| | |
|---|---|
| 000 | Output SCK1 |
| 001 | Input SCK2 (default) |
| 010 | Output SCK3 |
| 011 | Output SCK4 |
| 100 | Output SCK5 |
| 101 | Output SCK6 |
| Others | Reserved |

### SCS1[3:0]: SCK Selection of PORT-1 (MUX_P1SC)

These bits are used for routing SCK of PORT-2. Any combination of SCK1 to SCK6 and SCK can be connected to PORT-1. Refer to Figure 48 for more details.

Default value: 000

| | |
|---|---|
| 000 | Input SCK1 (default) |
| 001 | Output SCK2 |
| 010 | Output SCK3 |
| 011 | Output SCK4 |
| 100 | Output SCK5 |
| 101 | Output SCK6 |
| Others | Reserved |

### Register 104 (68h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 104 | 68h | LRCK/BCK selection of PORT-3 and PORT-4 | LBS4[3:0] | | | | LBS3[3:0] | | | |

### LBS4[3:0]: LRCK/BCK Selection of PORT-4 (MUX_P4BL)

These bits are used for routing LRCK and BCK of PORT-4. Any combination of LRCK1/BCK1 to LRCK6/BCK6 and LRCK/BCK of ADCs/DACs in master mode can be connected to PORT-4. Figure 49 shows a detailed diagram of PORT-4.

Default value: 0011

| | |
|---|---|
| 0000 | Output LRCK1 and BCK1 |
| 0001 | Output LRCK2 and BCK2 |
| 0010 | Output LRCK3 and BCK3 |
| 0011 | Input LRCK4 and BCK4 (default) |
| 0100 | Output LRCK5 and BCK5 |
| 0101 | Output LRCK6 and BCK6 |
| 0110 | Output LRCK and BCK from DAC12 in master mode |
| 0111 | Output LRCK and BCK from DAC34 in master mode |
| 1000 | Output LRCK and BCK from ADC12 in master mode |
| 1001 | Output LRCK and BCK from ADC34 in master mode |
| Others | Reserved |

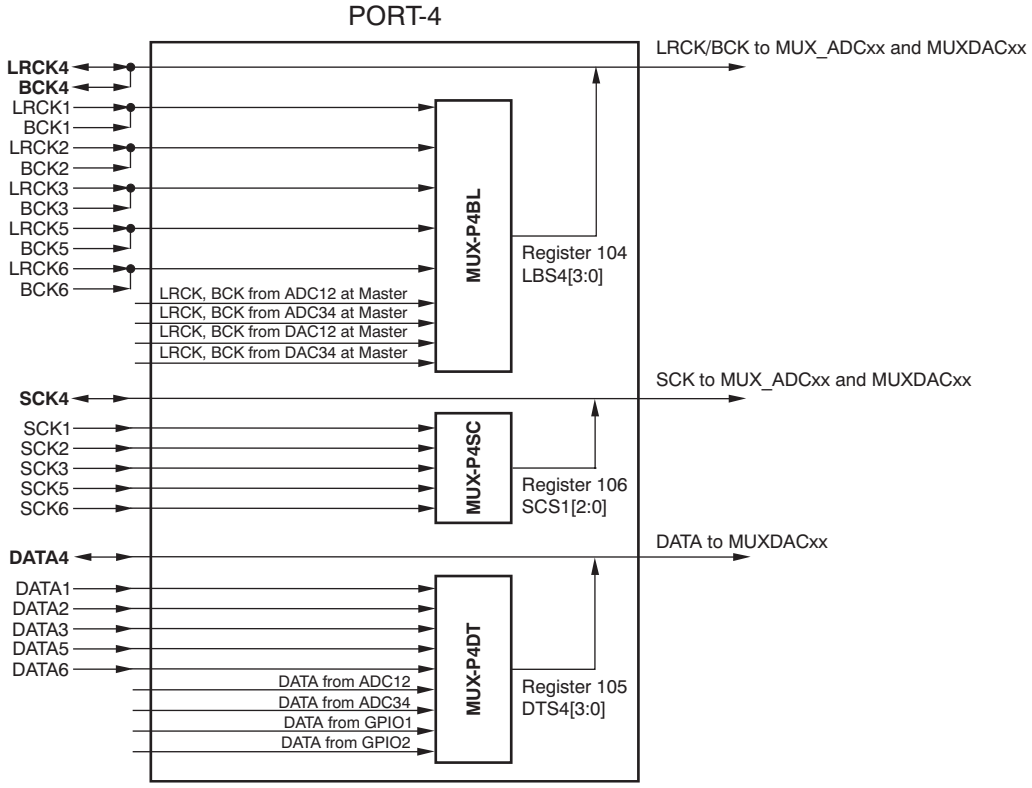



**Figure 49. Detailed Diagram of PORT-4**

### LBS3[3:0]: LRCK/BCK Selection of PORT-3 (MUX_P3BL)

These bits are used for routing LRCK and BCK of PORT-3. Any combination of LRCK1/BCK1 to LRCK6/BCK6 and LRCK/BCK of ADCs/DACs in master mode can be connected to PORT-3. Figure 50 shows a detailed diagram of PORT-3.

Default value: 0010

| | |
|---|---|
| 0000 | Output LRCK1 and BCK1 |
| 0001 | Output LRCK2 and BCK2 |
| 0010 | Input LRCK3 and BCK3 (default) |
| 0011 | Output LRCK4 and BCK4 |
| 0100 | Output LRCK5 and BCK5 |
| 0101 | Output LRCK6 and BCK6 |
| 0110 | Output LRCK and BCK from DAC12 in master mode |
| 0111 | Output LRCK and BCK from DAC34 in master mode |
| 1000 | Output LRCK and BCK from ADC12 in master mode |
| 1001 | Output LRCK and BCK from ADC34 in master mode |
| Others | Reserved |

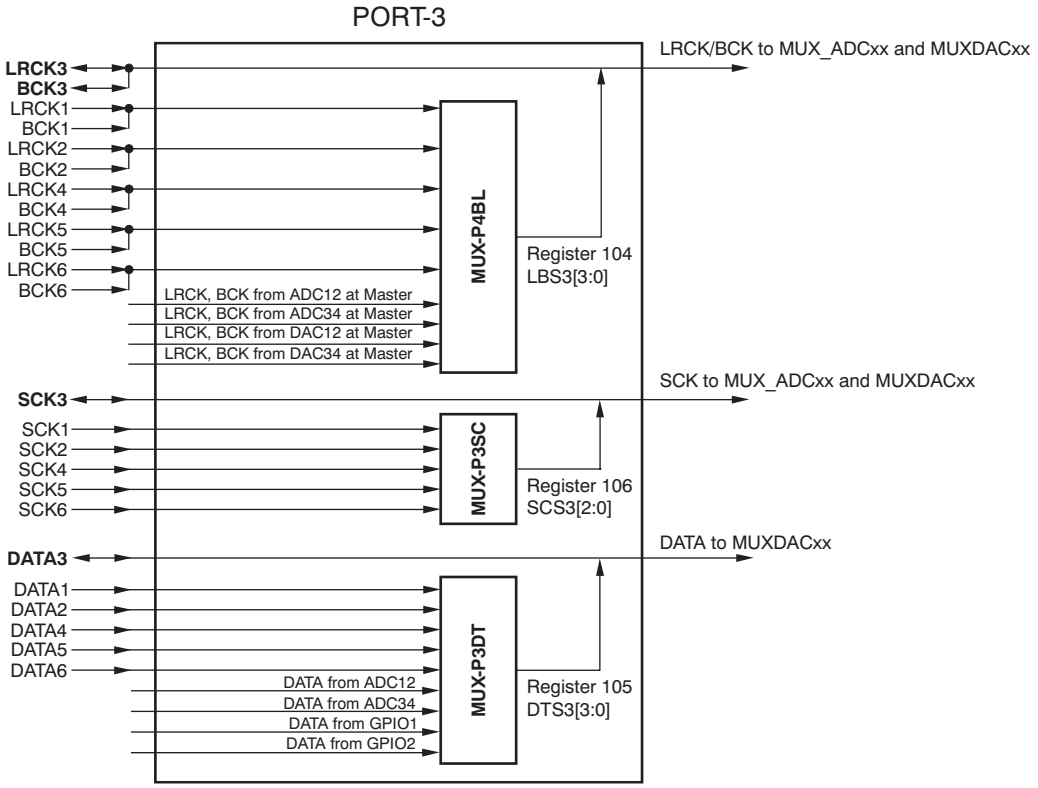



**Figure 50. Detailed Diagram of PORT-3**

### Register 105 (69h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 105 | 69h | DATA selection of PORT-3 and PORT-4 | DTS4[3:0] | | | | DTS3[3:0] | | | |

### DTS4[3:0]: DATA Selection of PORT-4 (MUX_P4DT)

These bits are used for routing DATA of PORT-4. Any combination of DATA1 to DATA6 and DATA of ADCs in master mode can be connected to PORT-4. Refer to Figure 49 for more details.

Default value: 0011

| | |
|---|---|
| 0000 | Output DATA1 |
| 0001 | Output DATA2 |
| 0010 | Output DATA3 |
| 0011 | Input DATA4 (default) |
| 0100 | Output DATA5 |
| 0101 | Output DATA6 |
| 0110 | Output GPIO1 |
| 0111 | Output GPIO2 |
| 1000 | Output DATA from ADC12 |
| 1001 | Output DATA from ADC34 |
| Others | Reserved |

### DTS3[3:0]: DATA Selection of PORT-3 (MUX_P3DT)

These bits are used for routing DATA of PORT-3. Any combination of DATA1 to DATA6 and DATA of ADCs in master mode can be connected to PORT-3. Refer to Figure 50 for more details.

Default value: 0010

| | |
|---|---|
| 0000 | Output DATA1 |
| 0001 | Output DATA2 |
| 0010 | Input DATA3 (default) |
| 0011 | Output DATA4 |
| 0100 | Output DATA5 |
| 0101 | Output DATA6 |
| 0110 | Output GPIO1 |
| 0111 | Output GPIO2 |
| 1000 | Output DATA from ADC12 |
| 1001 | Output DATA from ADC34 |
| Others | Reserved |

### Register 106 (6Ah)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 106 | 6Ah | SCK selection of PORT-3 and PORT-4 | RSV | SCS4[3:0] | | | RSV | SCS3[3:0] | | |

### SCS4[3:0]: SCK Selection of PORT-4 (MUX_P4SC)

These bits are used for routing SCK of PORT-4. Any combination of SCK1 to SCK6 and SCK can be connected to PORT-4. Refer to Figure 49 for more details.

Default value: 011

| | |
|---|---|
| 000 | Output SCK1 |
| 001 | Output SCK2 |
| 010 | Output SCK3 |
| 011 | Input SCK4 (default) |
| 100 | Output SCK5 |
| 101 | Output SCK6 |
| Others | Reserved |

### SCS3[3:0]: SCK Selection of PORT-3 (MUX_P3SC)

These bits are used for routing SCK of PORT-3. Any combination of SCK1 to SCK6 and SCK can be connected to PORT-3. Refer to Figure 50 for more details.

Default value: 010

| | |
|---|---|
| 000 | Output SCK1 |
| 001 | Output SCK2 |
| 010 | Input SCK3 (default) |
| 011 | Output SCK4 |
| 100 | Output SCK5 |
| 101 | Output SCK6 |
| Others | Reserved |

### Register 107 (6Bh)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 107 | 6Bh | LRCK/BCK selection of PORT-5 and PORT-6 | LBS6[3:0] | | | | LBS5[3:0] | | | |

### LBS6[3:0]: LRCK/BCK Selection of PORT-6 (MUX_P6BL)

These bits are used for routing LRCK and BCK of PORT-6. Any combination of LRCK1/BCK1 to LRCK6/BCK6 and LRCK/BCK of ADCs/DACs in master mode can be connected to PORT-6. Figure 51 shows a detailed diagram of PORT-6.

Default value: 0101

| | |
|---|---|
| 0000 | Output LRCK1 and BCK1 |
| 0001 | Output LRCK2 and BCK2 |
| 0010 | Output LRCK3 and BCK3 |
| 0011 | Output LRCK4 and BCK4 |
| 0100 | Output LRCK5 and BCK5 |
| 0101 | Input LRCK6 and BCK6 (default) |
| 0110 | Output LRCK and BCK from DAC12 in master mode |
| 0111 | Output LRCK and BCK from DAC34 in master mode |
| 1000 | Output LRCK and BCK from ADC12 in master mode |
| 1001 | Output LRCK and BCK from ADC34 in master mode |
| Others | Reserved |

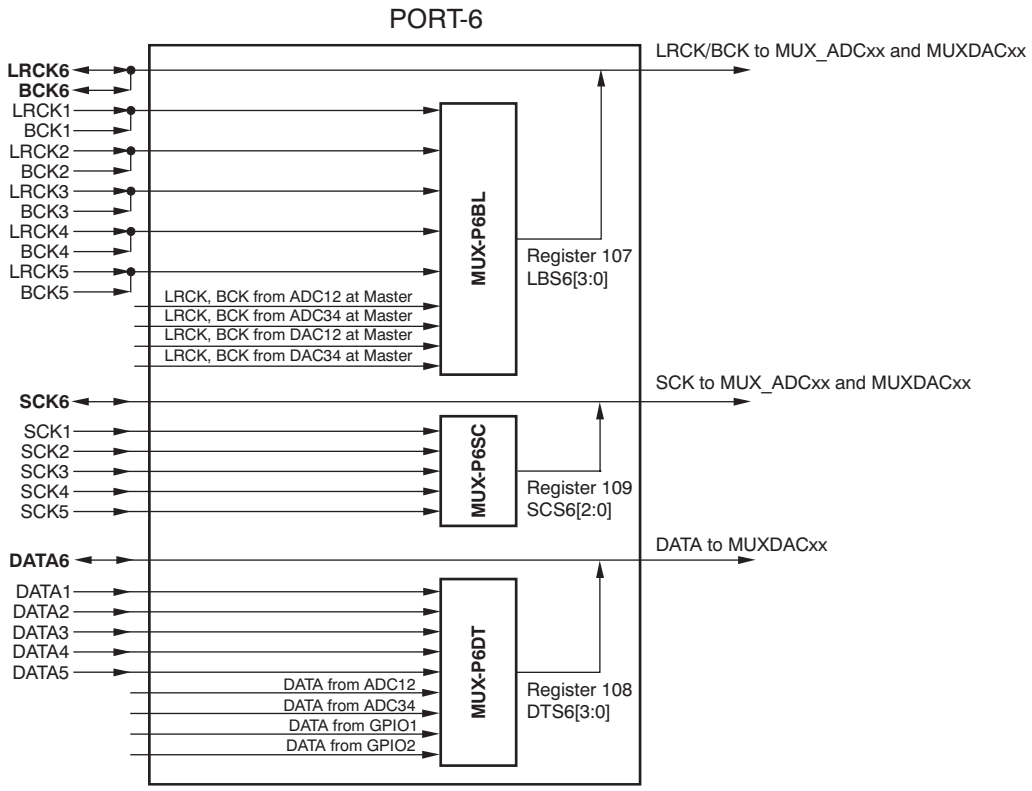



**Figure 51. Detailed Diagram of PORT-6**

### LBS5[3:0]: LRCK/BCK Selection of PORT-5 (MUX_P5BL)

These bits are used for routing LRCK and BCK of PORT-5. Any combination of LRCK1/BCK1 to LRCK6/BCK6 and LRCK/BCK of ADCs/DACs in master mode can be connected to PORT-5. Figure 52 shows a detailed diagram of PORT-5.

Default value: 0100

| | |
|---|---|
| 0000 | Output LRCK1 and BCK1 |
| 0001 | Output LRCK2 and BCK2 |
| 0010 | Output LRCK3 and BCK3 |
| 0011 | Output LRCK4 and BCK4 |
| 0100 | Input LRCK5 and BCK5 (default) |
| 0101 | Output LRCK6 and BCK6 |
| 0110 | Output LRCK and BCK from DAC12 in master mode |
| 0111 | Output LRCK and BCK from DAC34 in master mode |
| 1000 | Output LRCK and BCK from ADC12 in master mode |
| 1001 | Output LRCK and BCK from ADC34 in master mode |
| Others | Reserved |

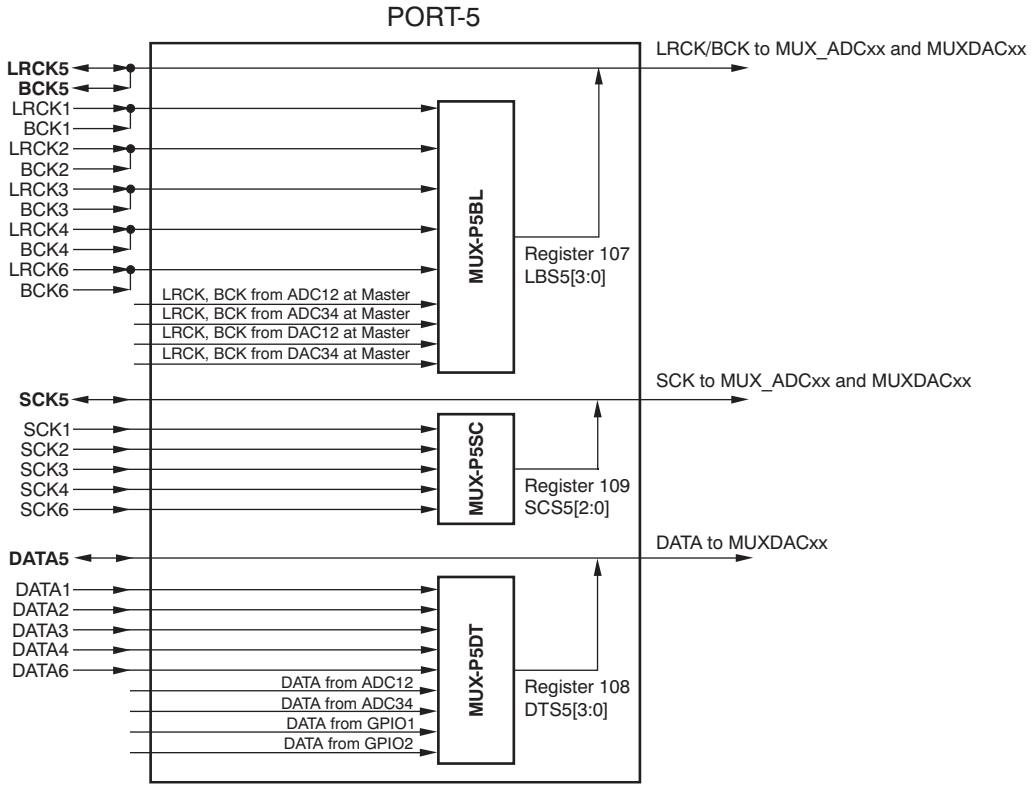



**Figure 52. Detailed Diagram of PORT-5**

### Register 108 (6Ch)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 108 | 6Ch | DATA selection of PORT-5 and PORT-6 | DTS6[3:0] | | | | DTS5[3:0] | | | |

### DTS6[3:0]: DATA Selection of PORT-6 (MUX_P6DT)

These bits are used for routing DATA of PORT-6. Any combination of DATA1 to DATA6 and DATA of ADCs in master mode can be connected to PORT-6. Refer to Figure 51 for more details.

Default value: 0101

| | |
|---|---|
| 0000 | Output DATA1 |
| 0001 | Output DATA2 |
| 0010 | Output DATA3 |
| 0011 | Output DATA4 |
| 0100 | Output DATA5 |
| 0101 | Input DATA6 (default) |
| 0110 | Output GPIO1 |
| 0111 | Output GPIO2 |
| 1000 | Output DATA from ADC12 |
| 1001 | Output DATA from ADC34 |
| Others | Reserved |

### DTS5[3:0]: DATA Selection of PORT-5 (MUX_P5DT)

These bits are used for routing DATA of PORT-5. Any combination of DATA1 to DATA6 and DATA of ADCs in master mode can be connected to PORT-5. Refer to Figure 52 for more details.

Default value: 0100

| | |
|---|---|
| 0000 | Output DATA1 |
| 0001 | Output DATA2 |
| 0010 | Output DATA3 |
| 0011 | Output DATA4 |
| 0100 | Input DATA5 (default) |
| 0101 | Output DATA6 |
| 0110 | Output GPIO1 |
| 0111 | Output GPIO2 |
| 1000 | Output DATA from ADC12 |
| 1001 | Output DATA from ADC34 |
| Others | Reserved |

### Register 109 (6Dh)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 109 | 6Dh | SCK selection of PORT-5 and PORT-6 | RSV | SCS6[3:0] | | | RSV | SCS5[3:0] | | |

#### SCS6[3:0]: SCK Selection of PORT-6 (MUX_P6SC)

These bits are used for routing SCK of PORT-6. Any combination of SCK1 to SCK6 and SCK can be connected to PORT-6. Refer to Figure 51 for more details.

Default value: 101

| | |
|---|---|
| 000 | Output SCK1 |
| 001 | Output SCK2 |
| 010 | Output SCK3 |
| 011 | Output SCK4 |
| 100 | Output SCK5 |
| 101 | Input SCK6 (default) |
| Others | Reserved |

#### SCS5[3:0]: SCK Selection of PORT-5 (MUX_P5SC)

These bits are used for routing SCK of PORT-5. Any combination of SCK1 to SCK6 and SCK can be connected to PORT-5. Refer to Figure 52 for more details.

Default value: 100

| | |
|---|---|
| 000 | Output SCK1 |
| 001 | Output SCK2 |
| 010 | Output SCK3 |
| 011 | Output SCK4 |
| 100 | Input SCK5 (default) |
| 101 | Output SCK6 |
| Others | Reserved |

### Register 110 (6Eh)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 110 | 6Eh | LRCK/BCK selection of DAC12 and DAC34 | D34LB[3:0] | | | | D12LB[3:0] | | | |

### D34LB[3:0]: LRCK/BCK Selection of DAC34 (MUX_DA34)

These bits are used for routing LRCK and BCK from each audio interface port to DAC34, or routing LRCK and BCK from DACs/ADCs to each audio interface port in master mode. Refer to Figure 33 for more details.

Default value: 0100

| | |
|---|---|
| 0000 | Select LRCK and BCK from PORT-1 |
| 0001 | Select LRCK and BCK from PORT-2 |
| 0010 | Select LRCK and BCK from PORT-3 |
| 0011 | Select LRCK and BCK from PORT-4 |
| 0100 | Select LRCK and BCK from PORT-5 (default) |
| 0101 | Select LRCK and BCK from PORT-6 |
| 0110 | Select LRCK and BCK from DAC12 in master mode |
| 0111 | Select LRCK and BCK from DAC34 in master mode |
| 1000 | Select LRCK and BCK from ADC12 in master mode |
| 1001 | Select LRCK and BCK from ADC34 in master mode |
| Others | Reserved |

### D12LB[3:0] LRCK/BCK Selection of DAC12 (MUX_DA12)

These bits are used for routing LRCK and BCK from each audio interface port to DAC12, or routing LRCK and BCK from DACs/ADCs to each audio interface port in master mode. Refer to Figure 33 for more details.

Default value: 0011

| | |
|---|---|
| 0000 | Select LRCK and BCK from PORT-1 |
| 0001 | Select LRCK and BCK from PORT-2 |
| 0010 | Select LRCK and BCK from PORT-3 |
| 0011 | Select LRCK and BCK from PORT-4 (default) |
| 0100 | Select LRCK and BCK from PORT-5 |
| 0101 | Select LRCK and BCK from PORT-6 |
| 0110 | Select LRCK and BCK from DAC12 in master mode |
| 0111 | Select LRCK and BCK from DAC34 in master mode |
| 1000 | Select LRCK and BCK from ADC12 in master mode |
| 1001 | Select LRCK and BCK from ADC34 in master mode |
| Others | Reserved |

### Register 111 (6Fh)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 111 | 6Fh | DATA selection of DAC12 and DAC34 | D34DT[3:0] | | | | D12DT[3:0] | | | |

### D34DT[3:0] DATA Selection of DAC34 (MUX_DA34)

These bits are used for routing DATA from each audio interface port to DAC34, or routing DATA from ADCs to each audio interface port in master mode. Refer to Figure 33 for more details.

Default value: 0100

| | |
|---|---|
| 0000 | Select DATA from PORT-1 |
| 0001 | Select DATA from PORT-2 |
| 0010 | Select DATA from PORT-3 |
| 0011 | Select DATA from PORT-4 |
| 0100 | Select DATA from PORT-5 (default) |
| 0101 | Select DATA from PORT-6 |
| 0110 | Select DATA from GPIO1 |
| 0111 | Select DATA from GPIO2 |
| 1000 | Select DATA from ADC12 |
| 1001 | Select DATA from ADC34 |
| Others | Reserved |

### D12DT[3:0] DATA Selection of DAC12 (MUX_DA12)

These bits are used for routing DATA from each audio interface port to DAC12, or routing DATA from ADCs to each audio interface port in master mode. Refer to Figure 33 for more details.

Default value: 0011

| | |
|---|---|
| 0000 | Select DATA from PORT-1 |
| 0001 | Select DATA from PORT-2 |
| 0010 | Select DATA from PORT-3 |
| 0011 | Select DATA from PORT-4 (default) |
| 0100 | Select DATA from PORT-5 |
| 0101 | Select DATA from PORT-6 |
| 0110 | Select DATA from GPIO1 |
| 0111 | Select DATA from GPIO2 |
| 1000 | Select DATA from ADC12 |
| 1001 | Select DATA from ADC34 |
| Others | Reserved |

### Register 112 (70h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 112 | 70h | SCK selection of DAC12 and DAC34 | RSV | D34SC[3:0] | | | RSV | D12SC[3:0] | | |

### D34SC[2:0] SCK Selection of DAC34 (MUX_DA34)

These bits are used for routing SCK from each audio interface port to DAC34. Refer to Figure 33 for more details.

Default value: 100

| | |
|---|---|
| 000 | Select SCK from PORT-1 |
| 001 | Select SCK from PORT-2 |
| 010 | Select SCK from PORT-3 |
| 011 | Select SCK from PORT-4 |
| 100 | Select SCK from PORT-5 (default) |
| 101 | Select SCK from PORT-6 |
| Others | Reserved |

### D12SC[2:0] SCK Selection of DAC12 (MUX_DA12)

These bits are used for routing SCK from each audio interface port to DAC12. Refer to Figure 33 for more details.

Default value: 011

| | |
|---|---|
| 000 | Select SCK from PORT-1 |
| 001 | Select SCK from PORT-2 |
| 010 | Select SCK from PORT-3 |
| 011 | Select SCK from PORT-4 (default) |
| 100 | Select SCK from PORT-5 |
| 101 | Select SCK from PORT-6 |
| Others | Reserved |

### Register 116 (74h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 116 | 74h | LRCK/BCK selection of ADC12 and ADC34 | A34LB[3:0] | | | | A12LB[3:0] | | | |

### A34LB[3:0]: LRCK/BCK Selection of ADC34 (MUX_AD34)

These bits are used for routing LRCK and BCK from each audio interface port to ADC34, or routing LRCK and BCK from DACs/ADCs to each audio interface port in master mode. Refer to Figure 33 for more details.

Default value: 0001

| | |
|---|---|
| 0000 | Select LRCK and BCK from PORT-1 |
| 0001 | Select LRCK and BCK from PORT-2 (default) |
| 0010 | Select LRCK and BCK from PORT-3 |
| 0011 | Select LRCK and BCK from PORT-4 |
| 0100 | Select LRCK and BCK from PORT-5 |
| 0101 | Select LRCK and BCK from PORT-6 |
| 0110 | Select LRCK and BCK from DAC12 in master mode |
| 0111 | Select LRCK and BCK from DAC34 in master mode |
| 1000 | Select LRCK and BCK from ADC12 in master mode |
| 1001 | Select LRCK and BCK from ADC34 in master mode |
| Others | Reserved |

### A12LB[3:0] LRCK/BCK Selection of ADC12 (MUX_AD12)

These bits are used for routing LRCK and BCK from each audio interface port to ADC12, or routing LRCK and BCK from DACs/ADCs to each audio interface port in master mode. Refer to Figure 33 for more details.

Default value: 0000

| | |
|---|---|
| 0000 | Select LRCK and BCK from PORT-1 (default) |
| 0001 | Select LRCK and BCK from PORT-2 |
| 0010 | Select LRCK and BCK from PORT-3 |
| 0011 | Select LRCK and BCK from PORT-4 |
| 0100 | Select LRCK and BCK from PORT-5 |
| 0101 | Select LRCK and BCK from PORT-6 |
| 0110 | Select LRCK and BCK from DAC12 in master mode |
| 0111 | Select LRCK and BCK from DAC34 in master mode |
| 1000 | Select LRCK and BCK from ADC12 in master mode |
| 1001 | Select LRCK and BCK from ADC34 in master mode |
| Others | Reserved |

### Register 117 (75h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 117 | 75h | SCK selection of ADC12 and ADC34 | RSV | A34SC[3:0] | | | RSV | A12SC[3:0] | | |

#### A34SC[2:0] SCK Selection of ADC34 (MUX_AD34)

These bits are used for routing SCK from each audio interface port to ADC34. Refer to Figure 33 for more details.

Default value: 001

| | |
|---|---|
| 000 | Select SCK from PORT-1 |
| 001 | Select SCK from PORT-2 (default) |
| 010 | Select SCK from PORT-3 |
| 011 | Select SCK from PORT-4 |
| 100 | Select SCK from PORT-5 |
| 101 | Select SCK from PORT-6 |
| Others | Reserved |

#### A12SC[2:0] SCK Selection of ADC12 (MUX_AD12)

These bits are used for routing SCK from each audio interface port to ADC12. Refer to Figure 33 for more details.

Default value: 000

| | |
|---|---|
| 000 | Select SCK from PORT-1 (default) |
| 001 | Select SCK from PORT-2 |
| 010 | Select SCK from PORT-3 |
| 011 | Select SCK from PORT-4 |
| 100 | Select SCK from PORT-5 |
| 101 | Select SCK from PORT-6 |
| Others | Reserved |

### Register 118 (76h)

| REG | HEX | DESCRIPTION | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 118 | 76h | GPIO1 and GPIO2 audio data selection | GP2S[3:0] | | | | GP1S[3:0] | | | |

### GP2S[3:0] GPIO2 Audio Data Selection

Default value: 1010

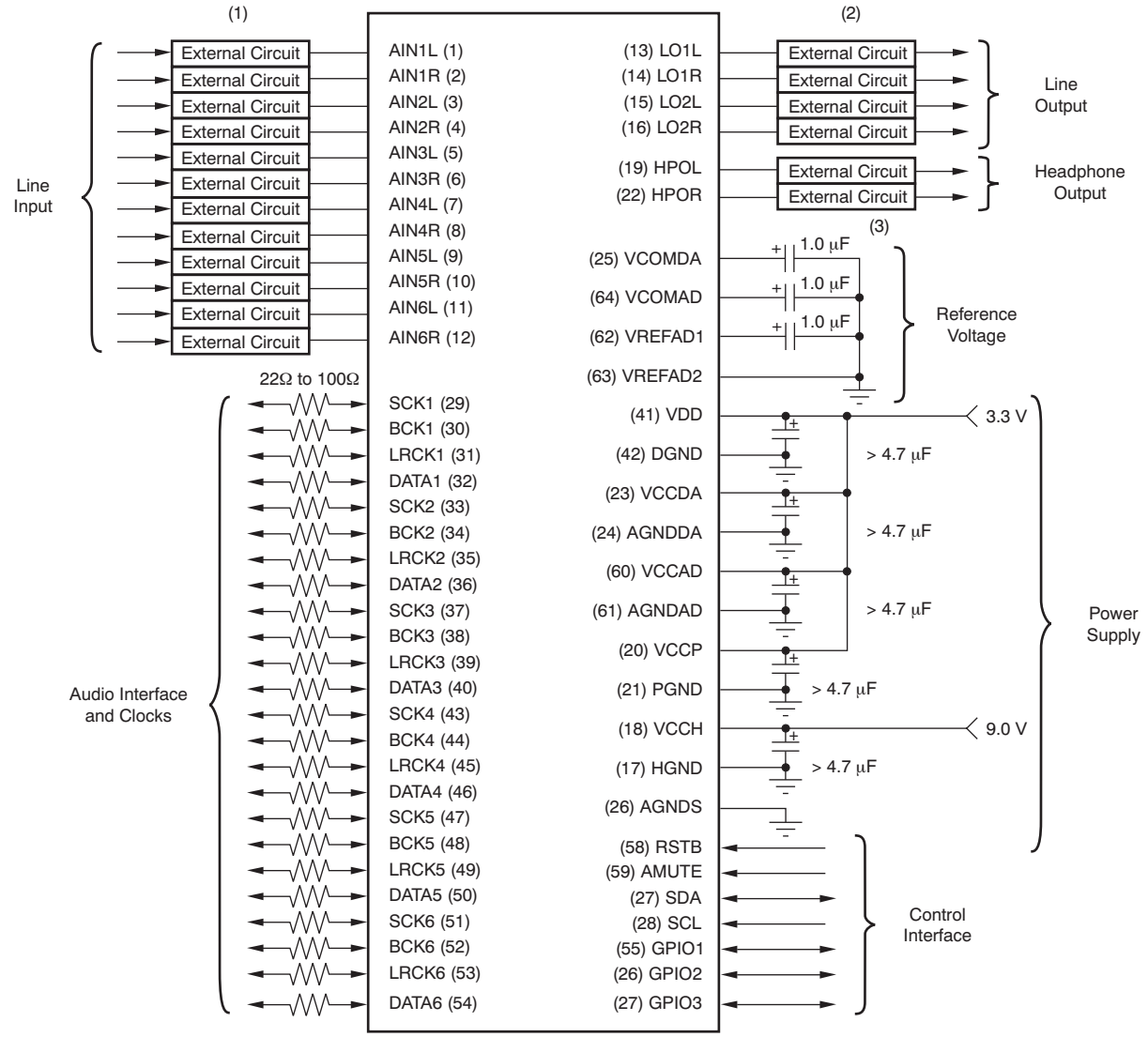
| | |
|---|---|
| 0000 | Output DATA1 |
| 0001 | Output DATA2 |
| 0010 | Output DATA3 |
| 0011 | Output DATA4 |
| 0100 | Output DATA5 |
| 0101 | Output DATA6 |
| 0110 | Output GPIO1 |
| 0111 | Input GPIO2 |
| 1000 | Output DATA from ADC12 |
| 1001 | Output DATA from ADC34 |
| 1010 | Use GPIO function (default) |
| Others | Reserved |

### GP1S[3:0] GPIO1 Audio Data Selection

Default value: 1010

| | |
|---|---|
| 0000 | Output DATA1 |
| 0001 | Output DATA2 |
| 0010 | Output DATA3 |
| 0011 | Output DATA4 |
| 0100 | Output DATA5 |
| 0101 | Output DATA6 |
| 0110 | Input GPIO1 |
| 0111 | Output GPIO2 |
| 1000 | Output DATA from ADC12 |
| 1001 | Output DATA from ADC34 |
| 1010 | Use GPIO function (default) |
| Others | Reserved |

## BASIC CONNECTION DIAGRAMS

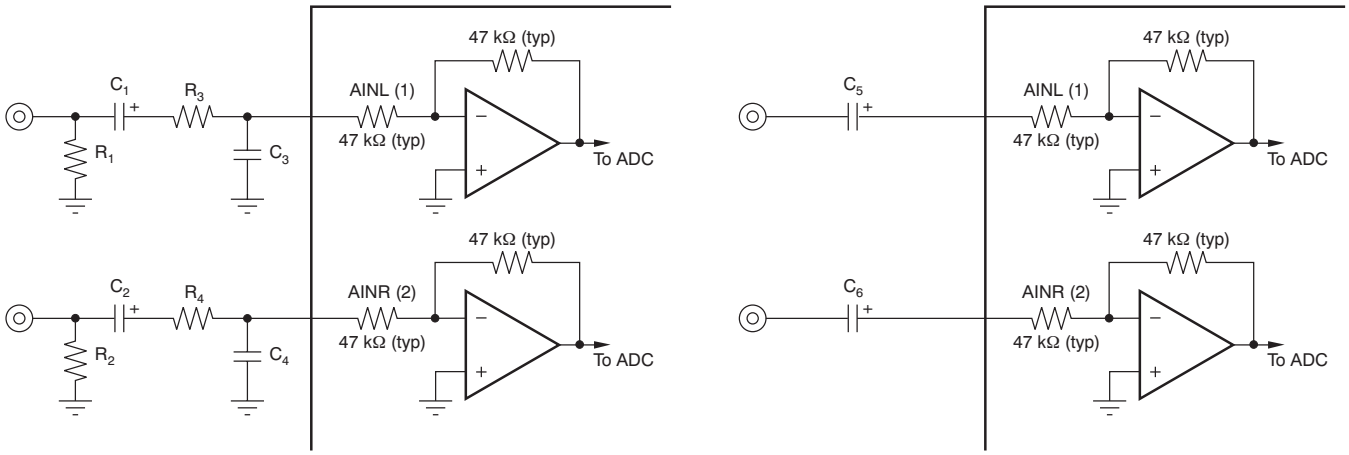



(1) See Figure 54 for the line input.

(2) See Figure 55 for the line output.

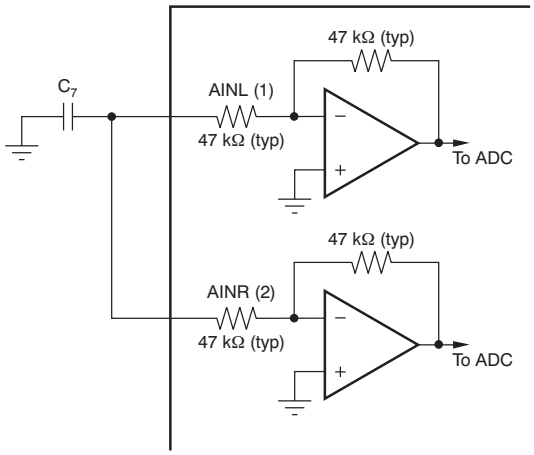
(3) See Figure 56 for the headphone output.

**Figure 53. Basic Connections**




**(a)** External Circuit for Line Input with Low-Pass Filter

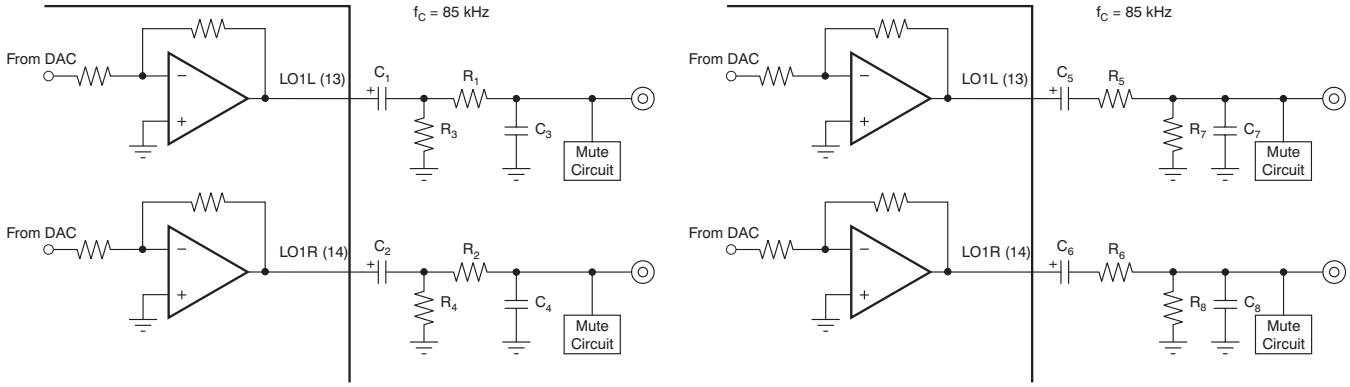
**(b)** External Circuit for Line Input without Low-Pass Filter




**(c)** External Circuit for not using Analog Input

$R_1$, $R_2$: Greater than 100 kΩ
$R_3$, $R_4$: 100 Ω to 1 kΩ
$C_1$, $C_2$, $C_5$, $C_6$: 1 µF to 47 µF
$C_3$, $C_4$: 0.01 µF to 0.001 µF
$C_7$: Less than 0.1 µF

**Figure 54. External Circuit for the Line Input**

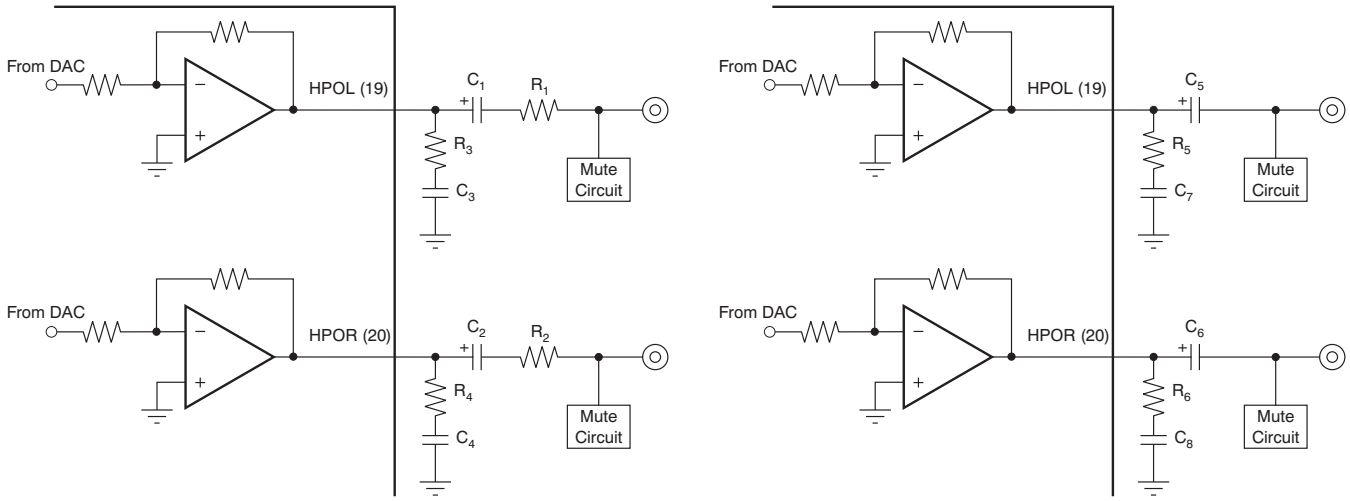



**(a)** External Circuit for Line Output with Low-Pass Filter

**(b)** External Circuit for Line Output with Low-Pass Filter

$R_1$, $R_2$, $R_5$, $R_6$: 270 Ω
$R_3$, $R_4$, $R_7$: > 100 kΩ
$C_1$, $C_2$, $C_5$, $C_6$: 1 µF to 47 µF
$C_3$, $C_4$, $C_7$, $C_8$: 6800 pF

**Figure 55. External Circuit for the Line Output**




**(a)** External Circuit with Short-Circuit protection Resistor

**(b)** External Circuit without Short-Circuit Protection Resistor

$R_1$, $R_2$ : 4 Ω to 16 Ω
$R_3$, $R_4$, $R_5$, $R_6$ : 22 Ω
$C_1$, $C_2$, $C_5$, $C_6$: 47 µF to 220 µF
$C_3$, $C_4$, $C_7$, $C_8$ : 0.022 µF

**Figure 56. External Circuit for the Headphone Output**

# BOARD DESIGN AND LAYOUT CONSIDERATIONS

## POWER-SUPPLY PINS

The digital and analog power supplies (VCC, VCCDA, VCCAD, VCCP, and VCCH) to the PCM5310 should be bypassed to the corresponding ground pins with a 1-µF to 4.7-µF electrolytic or ceramic capacitor, placed as close to the pins as possible to maximize the dynamic performance of ADC, DAC, and other analog circuits. If the power supply includes high-frequency noise, it is recommended to add a 0.1 µF ceramic capacitor as close as possible to the power-supply lines to improve the dynamic performance.

To maximize the dynamic performance of the ADC, DAC, and other analog circuits, the analog and ground pins (DGND, AGNDDA, AGNDAD, PGND, HGND and AGNDS) are not connected internally. These grounds should have a low impedance to avoid digital noise feeding to the analog ground. Therefore, they should be connected directly to each other under the device to reduce the potential of a noise problem.

## ANALOG INPUT PINS

All analog input pins (AIN1L/AIN1R to AIN6L/AIN6R) are single-ended inputs with an analog multiplexer. Antialiasing low-pass filters are included on the these inputs to remove the out-of-band nose from the audio. If the performance of these filters is not sufficient for a given application, appropriate external antialiasing filters are required. The passive RC filter (see Figure 54) is used in general. Any pins that are not used in a given application should be left open or connected to ground with a small, 0.1-µF ceramic capacitor.

## LINE OUTPUT PINS

All line output pins (LO1L, LO1R, LO2L and LO2R) are single-ended outputs with a 2-$V_{RMS}$ driver. An amplifier with a low-pass filter is not required as in a conventional DAC; however, the delta-sigma modulator generates out-of-band noise. The passive RC filter (see Figure 55) is used to remove this noise in general. If any line output pins are not used within a given application, they should be left open.

## HEADPHONE OUTPUT PINS

The headphone output pins (HPOL and HPOR) are single-ended outputs with more than 30-mW output power into either a 16-Ω or 32-Ω load. If the headphone output pins are not used within a given application, they should be left open. Adding a small resistor to these outputs is recommended (see Figure 56). in order to protect the application and device from short-circuiting.

## COMMON VOLTAGE PINS

A 1µF ceramic capacitor should be connected between the common voltage pins (VCOMAD and VCOMDA) for the analog circuit and ground to ensure low source impedance of the ADC and DAC common voltages. This capacitor should be located as close as possible to these pins.

## REFERENCE VOLTAGE PINS

A 1-µF ceramic capacitor should be connected between the VREFAD1 pin and ground to ensure low source impedance of ADC reference voltage. This capacitor should be located as close as possible to these pins. VREFAD2 pin should be connected to directly ground.

## DIGITAL OUTPUT PINS

The audio interface pins (LRCKx, BCKx, SCKx), clock pins (SCKx) and general-purpose input/output (GPIOx) pins change from input mode to output mode through register settings. In output mode, these pins have adequate load drive capability (see the *Electrical Characteristics*); however, if the signal lines are long, placing a buffer near the PCM5310 and minimizing the load capacitor is recommended in order to optimize crosstalk between the digital and analog circuits, maximize the dynamic performance of the ADC and DAC, and reduce overall power consumption. The digital output pins should be open if they are not used in a given application.

## DIGITAL INPUT PINS

Series resistors (ranging from 22 Ω to 100 Ω) are recommended for the SCKx, LRCKx, BCKx, and DATAx pins. These series resistors combine with the stray printed circuit board (PCB) and device input capacitance to form a low-pass filter that removes high-frequency noise from the digital signal, thus reducing high-frequency emissions. All digital input pins should be connected to ground if they are not used in a given application.

## PowerPAD (THERMAL PAD)

The PCM5310 is available in an HTQFP-64 PowerPAD package. The PowerPAD is a heatsink, which is exposed metal at the bottom of the package. The PowerPAD works to conduct heat away from the silicon through thermal vias located at the bottom of the PowerPAD.

The PowerPAD does not need to be soldered onto an exposed metal area of the PCB because the device works within the absolute maximum rating (junction temperature = +150°C) without soldering the PowerPAD.

Refer to application note SLMA002, *PowerPAD Thermally Enhanced Package*, when considering whether to solder the PowerPAD in order to reduce more heat from the device.

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision A (January 2010) to Revision B** **Page**

- Changed HUPE and HZRS default values in Register 30 ..... 52
- Changed DZ12 default value in Registers 40 and 41 ..... 57
- Changed DZ34 default value in Registers 50 and 51 ..... 61
- Changed AZ12 default value in Registers 80 and 81 ..... 66
- Changed AZ43 default value in Register 90 ..... 70
- Changed GP2S[3:0] and GP1S[3:0] default values in Register 118 ..... 91

**Changes from Original (February, 2009) to Revision A** **Page**

- Changed document to format to meet current standards ..... 1
- Deleted contents of the *Slave Address* subsection except for first sentence ..... 38

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCM5310PAP | ACTIVE | HTQFP | PAP | 64 | 160 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -25 to 85 | PCM5310 | Samples |
| PCM5310PAPR | ACTIVE | HTQFP | PAP | 64 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -25 to 85 | PCM5310 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

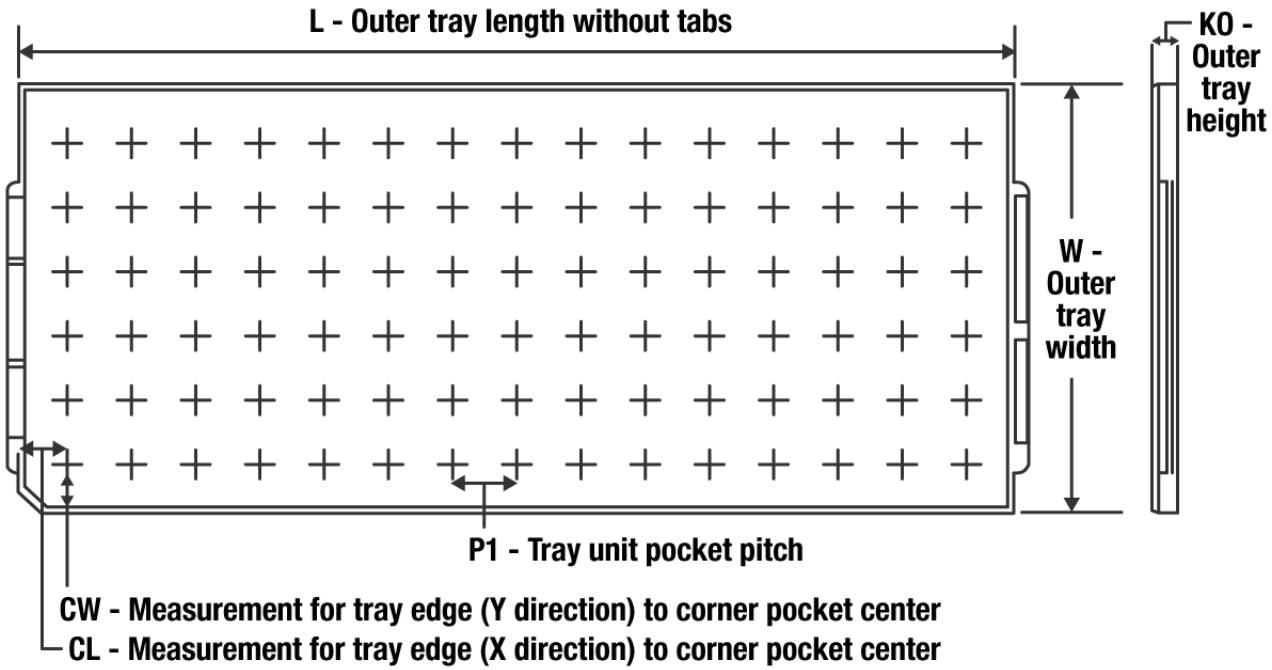
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PCM5310PAP | PAP | HTQFP | 64 | 160 | 8 x 20 | 150 | 315 | 135.9 | 7620 | 15.2 | 13.1 | 13 |

# GENERIC PACKAGE VIEW

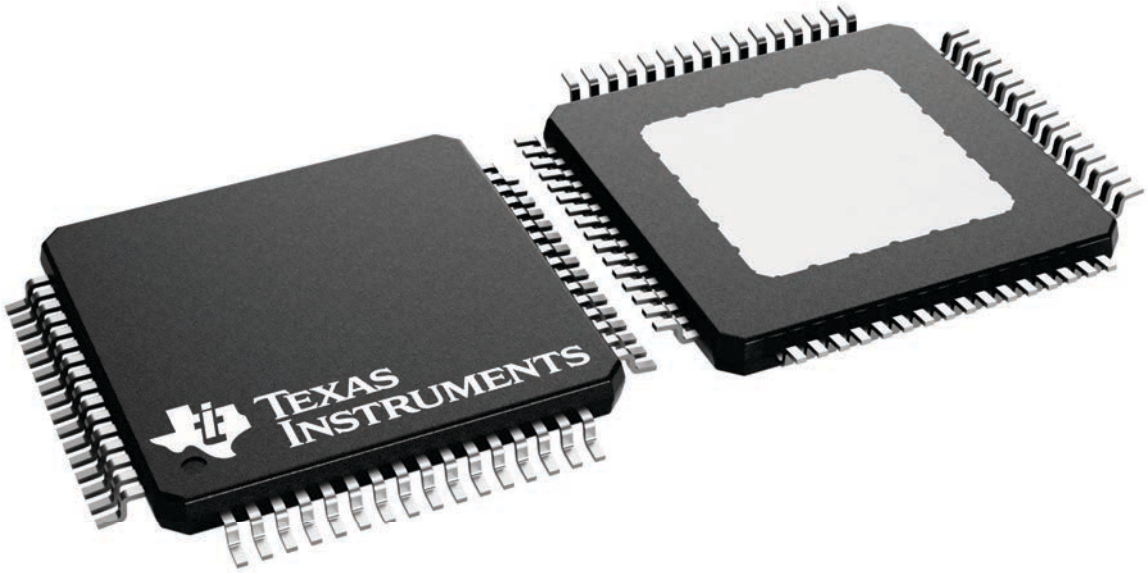
## PAP 64

## HTQFP - 1.2 mm max height

**10 x 10, 0.5 mm pitch**

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



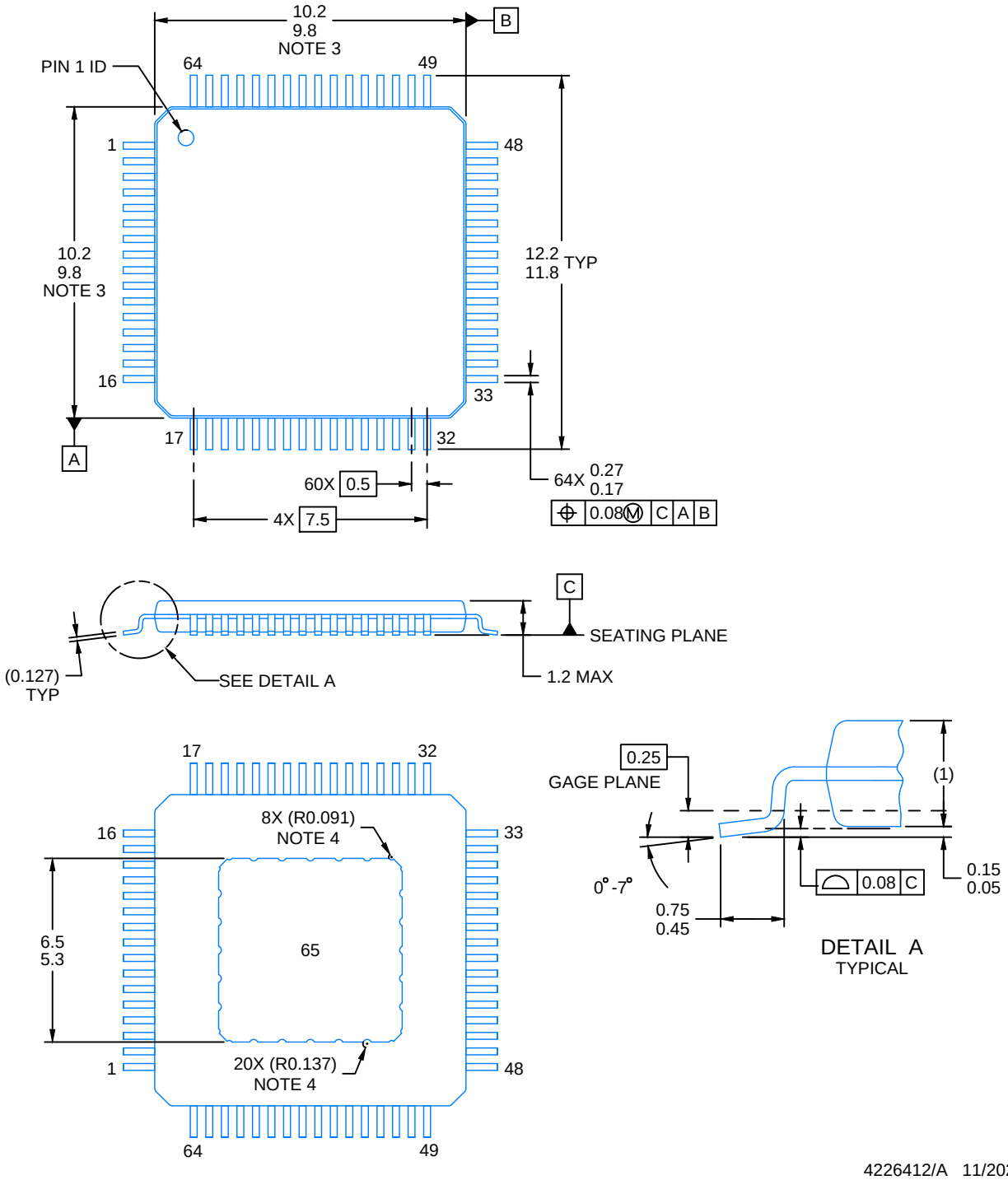

4226442/A

# PACKAGE OUTLINE

## PAP0064F

## PowerPAD™ TQFP - 1.2 mm max height

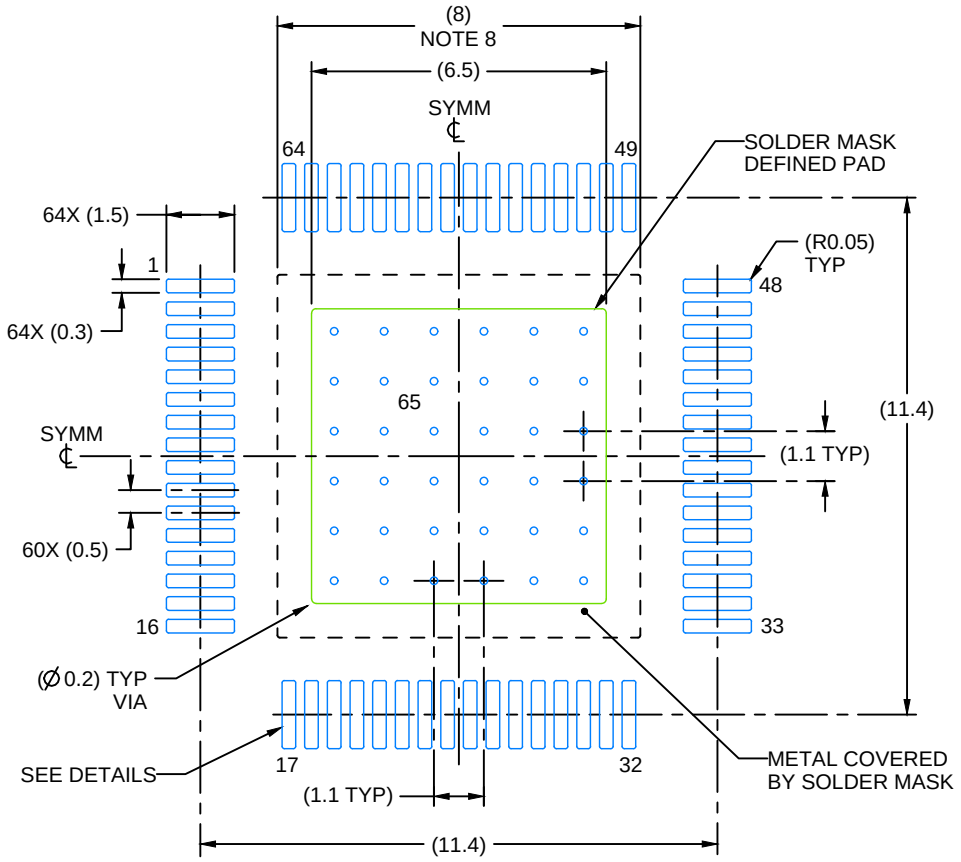
PLASTIC QUAD FLATPACK



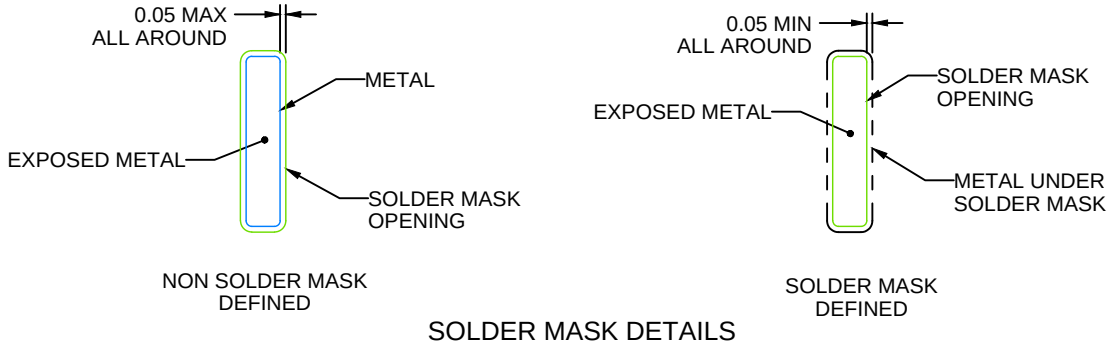

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X




NON SOLDER MASK
DEFINED

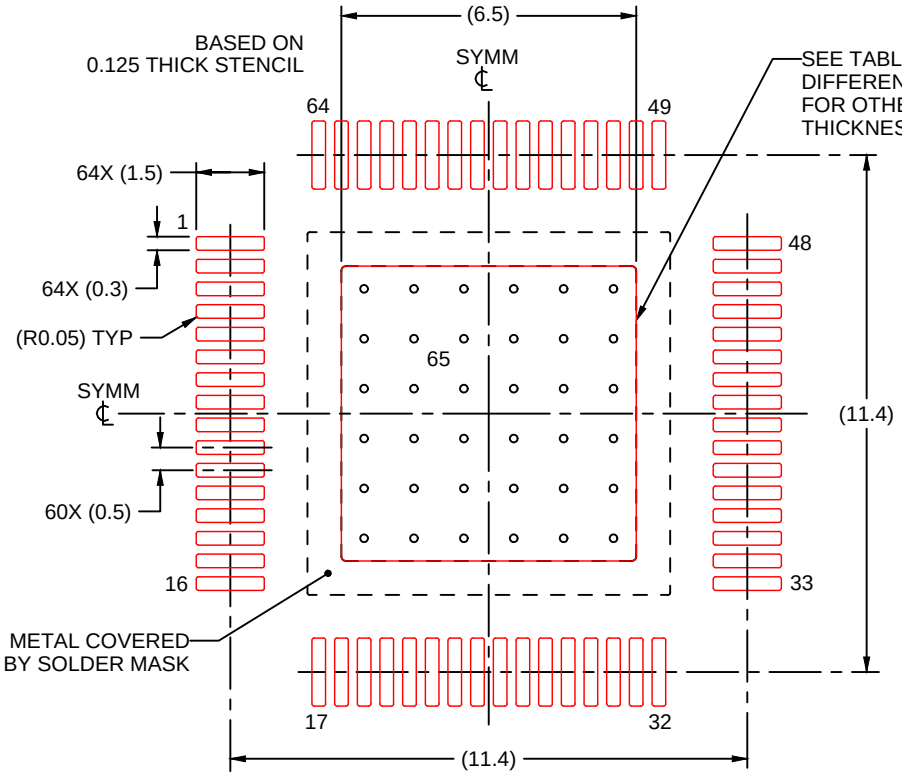
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4226412/A 11/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 7.27 X 7.27 |
| 0.125 | 6.5 X 6.5 (SHOWN) |
| 0.15 | 5.93 X 5.93 |
| 0.175 | 5.49 X 5.49 |

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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